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UNIVERSITÉ DE MONTRÉAL

DYNAMIC AVERAGED MODELS OF VSC-BASED HVDC SYSTEMS FOR ELECTROMAGNETIC TRANSIENT PROGRAMS

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FOR ELECTROMAGNETIC TRANSIENT PROGRAMS

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RÉSUMÉ

Les systèmes d'haute tension à courant continu (HTCC) basés sur technologies de convertisseur de source de tension (CST) offrent des prometteur opportunités dans une variété de domaines au sein de l'industrie des systèmes de puissance en raison de leurs avantages reconnus par rapport aux systèmes HTCC classiques basés à convertisseurs de commutation de ligne (CCL). La technologie CST-HTCC combine des convertisseurs de puissance, basé sur des IGBT (Insulated Gate Bipolar Transistor), avec des liens au courant continus pour transmettre la puissance dans l'ordre de milliers de mégawatts. En plus de contrôler le flux d'énergie entre deux réseaux à courant alternatif, les systèmes CST-HTCC peuvent fournir de réseaux faibles et même des réseaux passifs. Les systèmes CST-HTCC présentent une réponse dynamique plus rapide grâce à la méthode de modulation de largeur d'impulsions (MLI) en comparaison avec l'opération de commutation de fréquence fondamentale des systèmes HTCC traditionnels.

Représentation détaillée des systèmes CST-HTCC dans les programmes d'Électromagnétique Transitoire (EMT) comprend la modélisation des valves IGBT et doit normalement utiliser de pas d'intégration petit pour représenter avec précision les événements de commutation rapides. Les simulations et les calculs informatiques introduits par les modèles détaillés compliquent l'étude des événements en régime permanent et transitoire mettant en évidence la nécessité de développer des modèles plus efficaces qui assurent un comportement similaire de la réponse dynamique.

L'objectif de cette thèse est de développer des modèles moyennés qui reproduit avec précision le comportement statique et dynamique, en plus les transitoires des systèmes CST-HTCC dans des programmes de type EMT. Ces modèles simplifiés représentent la valeur moyenne des réponses des dispositifs de commutation, convertisseurs, et des contrôles à l'aide de techniques de valeur moyenne, de sources contrôlées et des fonctions de commutation. Cette thèse contribue également à l'élaboration de modèles CST détaillés utilisés pour valider les modèles moyenne proposés. Les modèles détaillés développés comprennent convertisseur avec topologies à deux et à trois niveaux et la plus récente topologie du convertisseur modulaire multiniveaux (CMM). Comparaison des différentes topologies de convertisseur approprié pour VSC-HVDC transmission, y compris leurs avantages et leurs limitations, sont également discutés.

Un système de commande robuste est élaboré sur la base de réglage vectorielle qui permet le contrôle simultané et indépendant de la puissance active et réactive à chaque terminal CST. Les techniques de modulation disponibles sont aussi présentées et comparés en termes de qualité et performance. L'approche de modélisation et des modèles développés sont validés pour une interconnexion CST-HTCC point-a-point réel entre la France et l'Espagne et pour un système multiterminal au courant continue (SMCC) utilisé pour intégrer de grandes quantités d'énergie éolienne offshore.

ABSTRACT

High Voltage Direct Current (HVDC) systems based on Voltage-sourced Converter (VSC) technologies present a bright opportunity in a variety of fields within the power system industry due to their recognized advantages in comparison to conventional line-commutated converter (LCC) based HVDC systems. VSC-HVDC technology combines power converters, based on IGBTs (Insulated Gate Bipolar Transistors), with dc links to transmit power in the order of thousands of megawatts. In addition to controlling power flow between two ac networks, VSC-HVDC systems can supply weak and even passive networks. VSC-HVDC systems present a faster dynamic response thanks to its Pulse-width Modulation (PWM) control in comparison with the fundamental switching frequency operation of traditional HVDC systems.

Detailed representation of VSC-HVDC systems in Electro Magnetic Transient (EMT) programs includes the modeling of IGBT valves and must normally use small integration time-steps to accurately represent fast switching events. Computational burden introduced by such a detailed models complicates the study of steady-state and transient events highlighting the need to develop more efficient models that provide similar behavior and dynamic response.

The objective of this thesis is to develop, test and validate averaged models to accurately replicate the steady-state, dynamic and transient behavior of VSC-based HVDC systems in EMT-type programs. These simplified models represent the average response of switching devices and converters by using averaging techniques involving controlled sources and switching functions. The work also contributes to the development of detailed VSC models used to validate the proposed average models. The detailed models developed include two- and three-level converter topologies and the most recent Modular Multilevel Converter (MMC) topology. Comparison of different converter topologies suitable to VSC-HVDC transmission, including their advantages and limitations, are also discussed.

A control system is implemented based on vector control which permits independent control both active and reactive power (and/or voltage) at each VSC terminal. Available modulation techniques are presented and compared in terms of performance and power quality. The modeling approach and models accuracy are validated, and their computing performance compared, for four test cases including an actual point-to-point VSC-HVDC interconnection between France

and Spain and a multi-terminal VSC-based (MTDC) system used to integrate large amounts of offshore wind generation.

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LIST OF NOTATIONS

(1.1)	Equation 1.1
[1]	Reference 1
2L	Two levels
3L	Three levels

LIST OF ABBREVIATIONS

A	Amperes
ac	Alternating Current
AVM	Average-value Model
BCA	Balancing Control Algorithm
CCSC	Circulating Current Suppression Control
CP	Constant Parameter Model
CSC	Current Source Converter
dc	Direct Current
DLL	Dynamic Link Library
DM	Detailed Model
DSP	Digital Signal Processor
EMT	Electromagnetic Transients
EMTP-RV	Electromagnetic Transients Program, Restructured Version
FACTS	Flexible ac Transmission Systems
FD	Frequency Dependent Line Model
GTO	Gate Turn-off Thyristor
HV	High Voltage
FC	Flying Capacitor
HM	Hybrid Multilevel
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
kV	kilo-Volt
LVRT	Low-voltage Ride Through
LCC	Line Commutated Converter
MMC	Modular Multi-level Converter
MTDC	Multi-terminal Direct Current
MV	Medium Voltage
MVA	Mega Volt-Ampere
MVAR	Mega Volt-Ampere Reactive

LIST OF ABBREVIATIONS

MW	Mega Watts
NPC	Neutral-point Diode-clamped
PI	Proportional Integral Control
PLL	Phase-locked Loop
POI	Point of Interconnection
pu	Per Unit
SCL	Short-circuit Level
SM	Sub-module
TD	Time Domain
THD	Total Harmonic Distortion
VCO	Voltage Controlled Oscillator
VSC	Voltage-sourced Converter
WB	Wideband Line or Cable Model

LIST OF APPENDICES

CHAPTER 1 INTRODUCTION

This work presents the development of dynamic averaged models for the accurate and efficient representation of VSC-based HVDC systems technology in EMT programs. The models developed are compared against their detailed representation for validation purposes. The comparison is performed for different VSC-HVDC configurations, converter topologies and applications. This work also presents a detailed description of different VSC-based technologies to introduce researchers into this field. All models developed during this work, including converters topologies, control systems, algorithms, and test cases were developed in the electromagnetic transient software EMTP-RV [1].

1.1 Motivation

Detailed modeling of HVDC systems include the representation of thousands IGBT switches and must normally use small numerical integration time-steps to accurately represent fast switching events. The computational burden introduced by such models highlights the need to develop simplified models that provide similar dynamic and transient behavior. These simplified models are known as mean- or average-value models (AVMs) and their objective is to replicate the average response of switching devices and converters by using simplified functions and controlled sources [2]-[5]. A different AVM concept is the switching function which intends to mimic the high frequency pattern of VSCs allowing the representation of high frequency harmonics [6]-[8]. AVMs have been successfully developed for low power applications in the aerospace and aircraft industry [9], [10] and for wind generation technologies [11]-[13]. However, it is a new trend in high power systems with few applications presented to date including traditional two and three-level VSC-HVDC models in EMT programs [14]-[16]. Reference [17] develops an efficient methodology for simulating MMC systems in EMT-type programs, but it does not model a detailed MMC including a large number of levels and integrated into a large scale transmission system.

The development of accurate and efficient averaged models in EMT programs enables the use of VSC-HVDC technologies integrated into a large grid which corresponds to the main motivation of this research work.

1.2 Contributions of the Thesis

The main objective of this thesis is to overcome the existing computing limitations associated with the detailed modeling of VSC-based HVDC system integrated to large grids. This thesis contributes to the comparison of existing models as well as the development of new averaged models for different VSC technologies. The proposed models are computationally efficient and accurate for the modeling of dynamic and transient events in power systems. The main contributions of this thesis include:

- Providing a comprehensive literature review and description of the available VSC-based HVDC technologies, their main component, applications, and comparison with conventional LCC-based HVDC technologies.
- Providing comprehensive review and description of the available averaging modeling techniques and methods currently used in power electronic applications as well as exploring their applicability to VSC-based HVDC technologies.
- Developing detailed two- and three-level VSC-based HVDC models for different applications in EMTP-RV. These models include converter's IGBT switches, control and protection systems. They are built with the purpose of validating the proposed averaged models.
- Developing detailed MMC-based HVDC models for different applications in EMTP-RV. The models include converter's IGBT switches, control and protection systems. They are built with the purpose of validating the proposed averaged models. These detailed MMC-based models are the first and only full model benchmark available for model validation and for the use in the studies where averaged models may not be suitable.
- Developing efficient averaged models for different VSC-HVDC systems that accurately represent the dynamic and transient behavior of this technology when integrated into large grids. Identifying advantages and limitations of the developed models and their suitability to represent different events in power systems.
- Building test cases in EMTP-RV to demonstrate accuracy and performance of the developed models. Test cases include applications such as point-to-point HVDC

terminals, asynchronous HVDC interconnections, and MTDC systems to integrate offshore wind generation.

- Comparing different VSC-based technologies and assessing their impact on harmonic content, controllability and fault ride-trough capabilities.
- Identifying advantages and limitations of the developed averaged models and studying their suitability to model different events in power systems.

1.3 Methodology

The methodology proposed involves developing detailed models (DMs) in EMTP-RV that accurately represent the actual behavior of VSC-HVDC technologies. These DMs are used to validate the proposed AVMs for different test cases and scenarios. The validation criteria involves comparing systems response to different disturbances such as ac faults, dc faults, changes on power and voltage order set points, power inversion test and other dynamic and transient tests. An initialization technique is proposed to properly set the initial conditions for the time-domain simulation from the multiphase load-flow module of EMTP-RV. The model validation includes the comparison of different variables in time-domain and the comparison of the harmonic content of voltages and currents. The simulation times for different time-steps will be used as a parameter to compare the computing performance and efficiency of the proposed models.

1.4 Thesis Outline

The work presented in this thesis is divided into the following chapters:

- Chapter 1: Introduction.
- Chapter 2: VSC-HVDC Technology: Describes the existing VSC-based HVDC technologies, main components and applications.
- Chapter 3: Detailed VSC-HVDC Models: Develops detailed models for VSC-based technologies to be used in the validation of the proposed AVMs.
- Chapter 4: Average-value Models for VSC-HVDC Systems: Presents the available methodologies for averaging of power converters used in HV and LV applications, and

develops new averaged models for different VSC-based technologies applied to HVDC transmission. It also presents available simplified methods for efficient modeling of VSC-HVDC systems.

- Chapter 5: Dynamic Performance of Averaged Models: Performs a comparison and validation of the averaged models developed against their detailed representation for different VSC-HVDC applications. It also presents the advantages and limitations of the proposed models.
- Chapter 6: Conclusions.

The thesis is complemented with appendices (B to E) that include all relevant data required to replicate the proposed models and test cases as well as block diagrams showing the models design developed in EMTP-RV. Appendix A provides a summary list with the correspondence between the figures in this thesis and their respective EMTP-RV files (test cases).

CHAPTER 2 VSC-HVDC TECHNOLOGY

This chapter starts with a brief introduction to HVDC systems followed by a description of the currently available VSC technologies applied to HVDC transmission including main system components, converter topologies, modulation techniques, and control and protection systems.

2.1 Technology Background

Three-phase alternating current (ac) has been the dominant solution for high-power long-distance transmission since the 19th century. The highest commercial voltage level, initially adopted in 1968, is 765kV. Even though few facilities have been built and are operated at higher voltages (1,000kV and 1,200kV), 765kV remains as the highest commercial transmission voltage currently in operation. In ac transmission systems however, the maximum transfer capability may be limited by not only thermal, but also stability and reliability constraints. In order to increase transfer capability, reduce losses and improve stability margins in long transmission lines, series and shunt compensation may be required forcing the use of costly switching substations or building parallel lines. Transfer capability limitations are particularly true for ac transmission involving underground (or submarine) cables where shunt compensation is required causing stability problems in some cases [18].

The development of HVDC transmission technology in 1954 introduced a bright opportunity for long distance transmission due to its superb capabilities and advantages in comparison to ac technologies. Some of the advantages of traditional HVDC over ac transmission are the reduced line losses and cost for comparable distance and capacity. It enables the use of HV cable connections and asynchronous interconnections, and also allows controllability of power flows and voltage which helps improving system stability. Other advantages are the isolation from disturbances of two interconnected systems and the limitation of fault currents and short-circuit levels.

Early development of power electronics for HVDC technologies back in 1939 considered the use of Current Source Converters (CSC) based on mercury-arc valves as it was found to be the most suitable technology to handle large currents. The appearance of the thyristor semiconductor in 1950 had an enormous impact on static-converter technology and it started to

be used in HVDC transmission by mid-1970s. Ever since, LCC technology based on thyristor valves has dominated the HVDC industry.

From 1990 onwards, the VSC technology became economically viable thanks to the development of self-commutated high-power switches, such as GTOs and IGBTs, and the computing power of Digital Signal Processors (DSPs) to generate the firing patterns. HVDC markets involving long-distance high-power transmission are still dominated by traditional thyristor-based HVDC technology, but it is expected that VSC-based technology will replace traditional CSC technology in future due to the fast development of high-power semiconductor, controls systems and protection schemes [19].

VSC-HVDC systems have the capability to rapidly control both active and reactive power independently of each other to keep the voltage and frequency stable. This gives total flexibility regarding the location of the power converters in the system including ac networks having a very low Short-circuit Level (SCL). In contrast to LCC technology, the polarity of the dc link voltage remains the same with the dc current being reversed to change the direction of power flow which eliminates the issue of commutation failures. In addition, VSC-HVDC systems enable black start and emergency support, stabilization of ac grids, fast reverse power flow control, multi-terminal dc implementation, and eliminate the need of ac filters and the use of grounding electrodes due to bipolar operation [20].

Different VSC topologies have been developed in the past 20 years. However, only two have been successfully implemented in HVDC applications: two-level (2L) and multilevel neutral-point diode-clamped (NPC), also known as three-level (3L) [20], [21]. Recent trends on multilevel converters for HVDC include modular multilevel converter (MMC) topology which connects 2L converter modules in cascade to achieve the desired ac voltage [22]-[24]. VSC-HVDC technologies are currently offered by three manufacturers ABB [25], Siemens [26] and Alstom Grid [27].

2.2 VSC-HVDC System Overview

Figure 2.1 shows a high-level representation of a VSC-HVDC terminal for 2L (or 3L) converter topology. A three-phase transformer, with its secondary winding connected in delta to block the zero-sequence voltages generated by the VSC, is used to interface the converter with

the ac system. A series reactor (L) is added between the converter and the transformer for control of active and reactive powers and low-pass filtering of the PWM pattern. It is also used to limit the short-circuit currents. The primary objective of the dc side capacitor (C) is to provide a low impedance path for the turned-off current, to reduce harmonic ripple on the dc voltage (filter) and also to serve as an energy storage device. The control system uses a vector-type control that includes a Phase Locked-loop (PLL), an outer controller and an inner controller. VSCs based on 2L and 3L topologies typically use high-frequency (greater than 1,000Hz) PWM or space-vector modulation [28], [29].

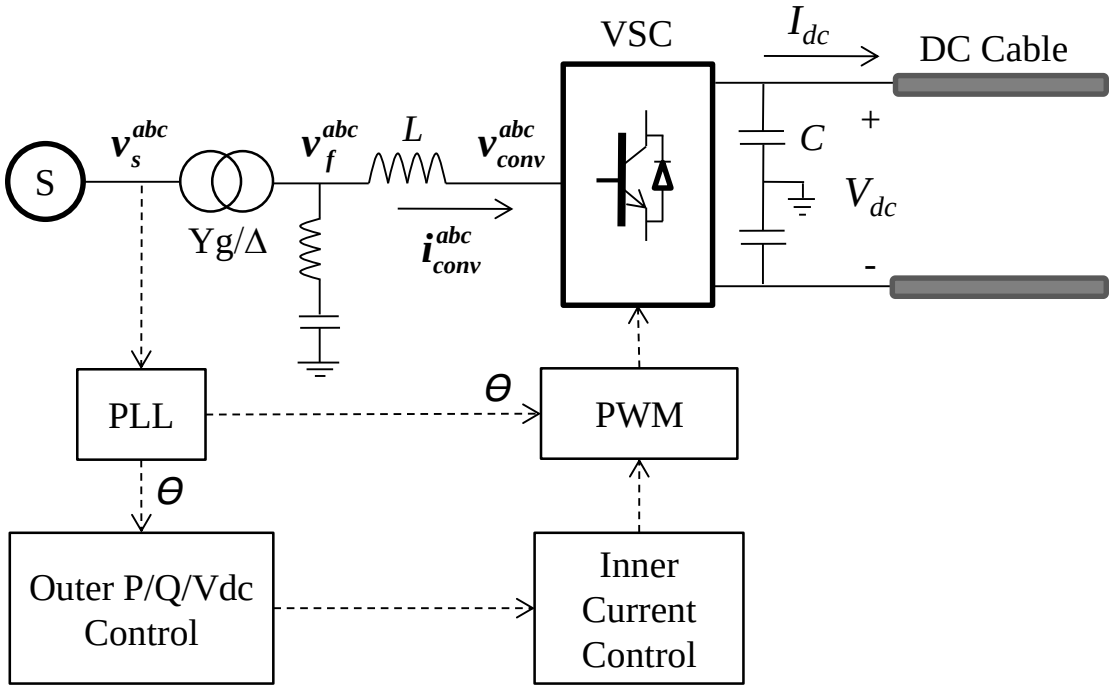


Figure 2.1: 2L (or 3L) VSC-HVDC terminal

New VSC technologies are based on multilevel configurations where 2L sub-modules (SMs) are connected in cascade to form a MMC. The overall configuration of a MMC terminal is presented in Figure 2.2. MMC topologies use a smaller switching frequency helping to reduce converter losses. In addition, filter requirements are eliminated by using a significant number of levels per phase. Scalability to higher voltages is easily achieved and reliability improved by increasing the number of SMs per multivalve arm [30]. The dc capacitors are now included in each SM and the series reactors, used to control the power flow and circulating currents, are

embedded in the converter's phase arms. A Balancing Control Algorithm (BCA) is required to control arm currents and the dc voltage on each SM capacitor [40].

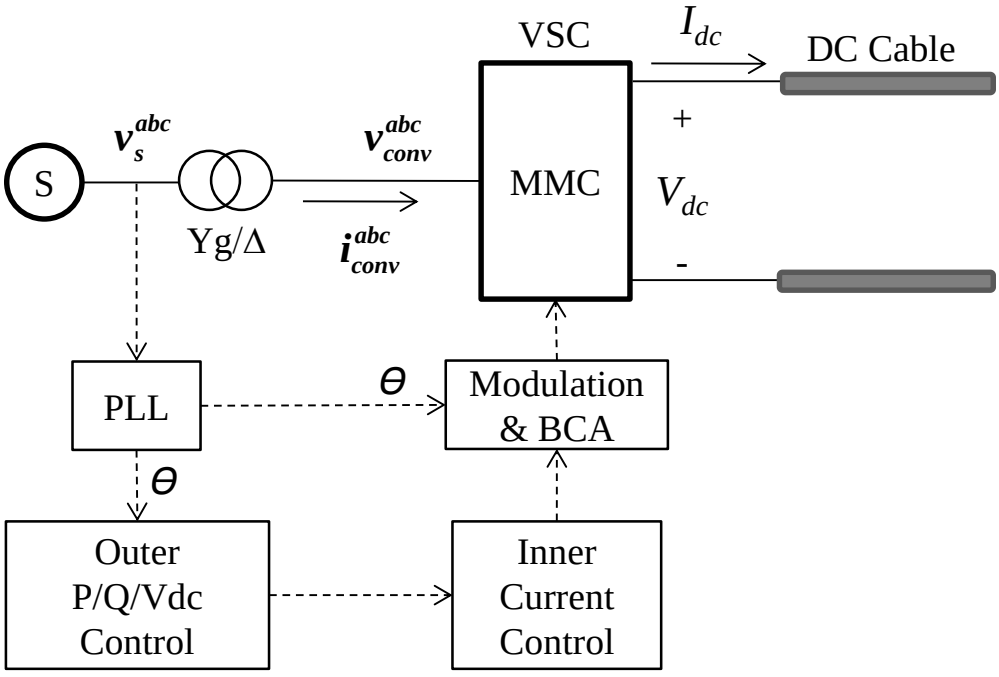


Figure 2.2: MCC VSC-HVDC terminal

2.3 VSC Topologies

VSCs are based on state-of-the-art IGBT semiconductor switches with turn-on/turn-off capabilities and operate at high or low frequencies depending on the topology and modulation technique. The focus of this thesis covers 2L, 3L-NPC and MMC topologies. Other multilevel topologies used in HV and MV applications, such as Flexible ac Transmission Systems (FACTS), are also discussed in this section.

2.3.1 Two-level Converter

The 2L topology has been used in a wide range of power levels including VSC-HVDC transmission. The basic configuration of a three-phase 2L converter is presented in Figure 2.3. Actual systems use packs units grouping several IGBTs switches in series each capable of handling currents between 1-2kA and voltages up to approximately 3kVdc [25]. Features taken into account when designing and specifying IGBT switches are high blocking voltage and turn-off current, low conduction and switching losses, short turn-on and turn-off times, suitable for

series connection, high dv/dt and di/dt withstand capability, good thermal characteristics, and low failure rates [21].

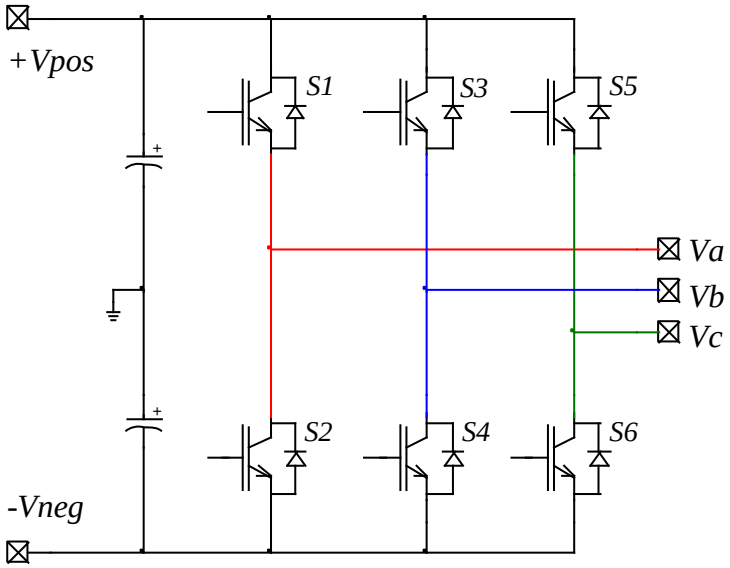


Figure 2.3: 2L Converter topology

The voltage pattern generated by a 2L converter oscillates between +*Vpos* and -*Vneg* (two voltage levels) at a predefined switching frequency. Figure 2.4 shows the 2L converter output and the dominant 50Hz component for a switching frequency ratio of 27 (1,350Hz). The sinusoidal carrier-based PWM produces a voltage waveform with a dominant component plus significant high-order harmonics which are eliminated by means of tuned filter and high-order damped filters.

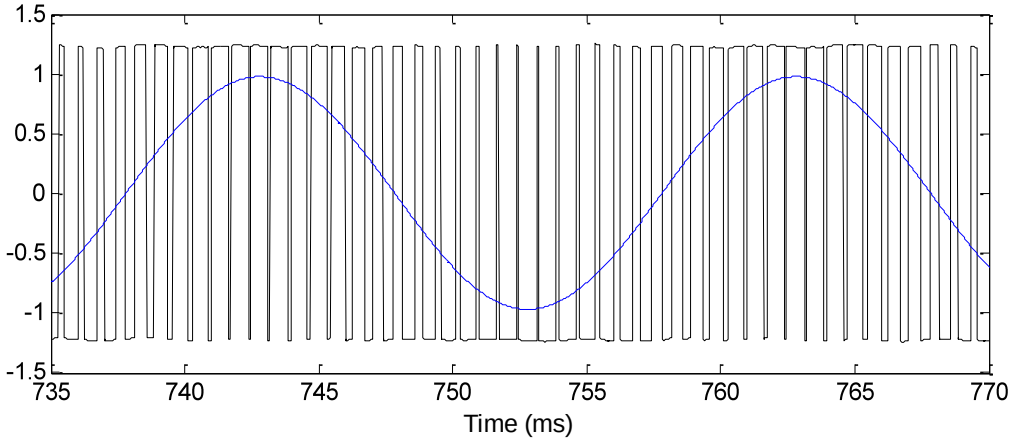


Figure 2.4: 2L Converter voltage (pu) (blue: 50 Hz component, black: converter output)

Although a VSC feeds fundamental ac current into the system, the converter voltage output is in reality a rectangular waveform. The ac system components connected to the VSC would be exposed to very large step changes in voltage with dv/dt levels up to l00kV/μs. This waveform is unacceptable for direct connection to an ac networks and, if a converter transformer is employed, high-frequency filters are generally used to limit the transformer's exposure to high dv/dt levels. The advantages of the 2L topology are simpley circuitry, small dc capacitors and footprint, and the same duty is required for all the IGBTs. The main disadvantages are the large blocking voltage required for the IGBTs, crude waveforms forcing the need of filters and high converter losses due to the high switching frequency [21].

2.3.2 Multilevel Converters

Several multilevel converter topologies have been developed in the past for different HV and MV applications. Most typical multilevel configurations are diode-clamped (NPC), flying capacitor (FC) and hybrid multilevel (HM) converters [31]-[33]. Each configuration may contain several levels, but three-levels have been used in HVDC applications and particularly the NPC topology. A brief description of each of them is provided in this section with emphasis in 3L-NPC topology.

2.3.2.1 Neutral Point Diode-clamped Converter

The configuration of a three-phase 3L-NPC converter is presented in Figure 2.5. The voltage pattern generated by a 3L converter has three levels 0, *+Vpos* and *-Vneg* oscillating at the switching frequency. Taking phase *a* in Figure 2.5, when IGBTs *S11* and *S12* are turned ON, the output is connected to *+Vpos* and when *S12* and *S21* are ON, the output is connected to ground. When *S21* and *S22* are ON, the output is connected to *-Vneg*. Clamp diodes provide the connection to the neutral point (or ground). From the switching states, it can be deduced that IGBTs *S12* and *S21* are ON for most of the cycle, resulting in greater conduction loss than *S11* and *S22*, but less switching loss. The dc bus capacitors are connected in series and establish the mid-point neutral voltage (ground in the case of Figure 2.5). In NPC inverters, maintaining the voltage balance between the capacitors is important for the proper operation of the NPC topology.

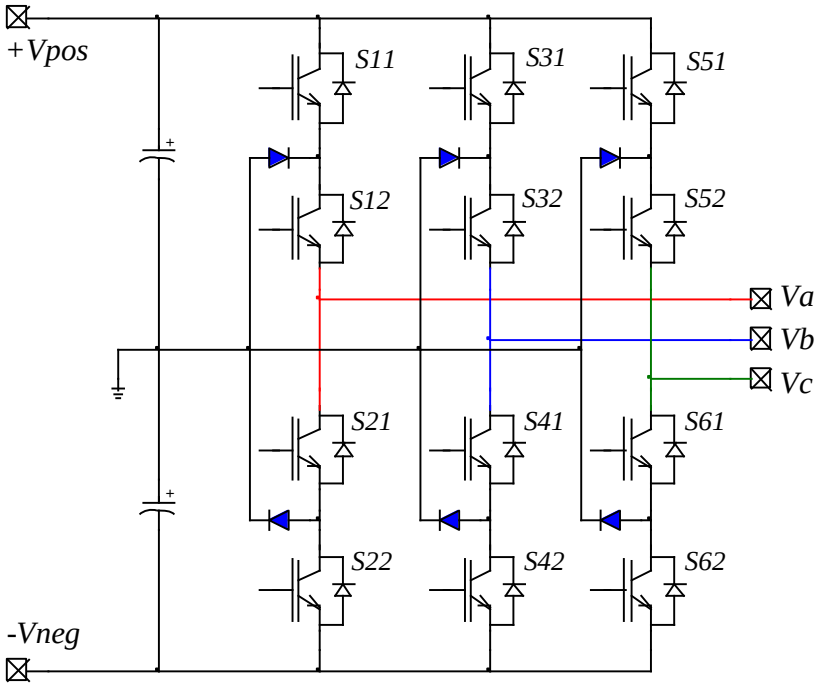


Figure 2.5: 3L NPC converter topology

Figure 2.6 shows the 3L converter output and the dominant 50 Hz component for a switching frequency ratio of 27 (1,350Hz). Similar to the 2L topology, PWM produces a voltage waveform with a fundamental component plus high-order harmonics which are eliminated by means of tuned and high-order damped filters.

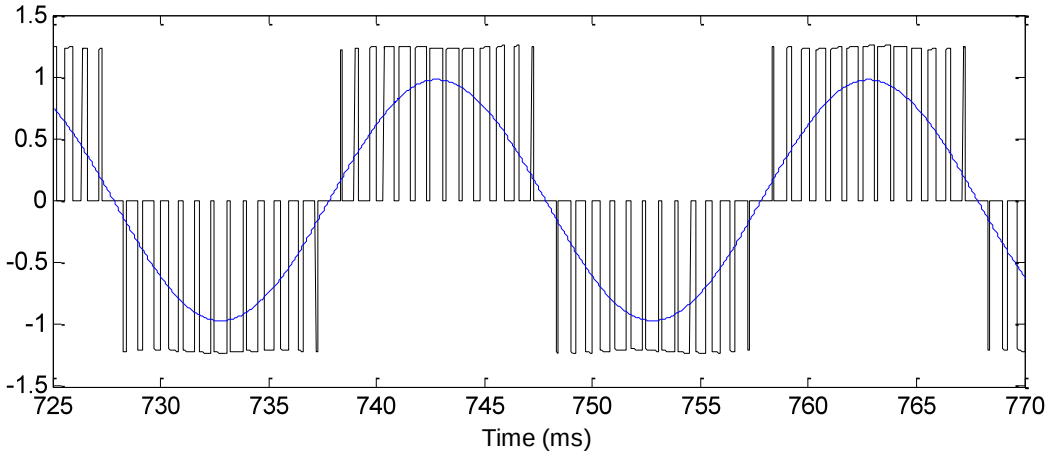


Figure 2.6: 3L Converter voltage (pu) (blue: 50Hz component, black: converter output)

The switching sequence required to generate the voltage pattern is described in reference [31]. The advantages of the 3L-NPC topology are reasonably small dc capacitors needed, lower switch

blocking voltages, small footprint, improved basic ac waveform and relatively low converter switching losses. Among the disadvantages is the inherent difficulty in keeping dc capacitor voltages constant, complex circuitry for large number of levels, the number of added diodes increases rapidly with the number of levels and semiconductor switches have different duties [21].

2.3.2.2 Flying Capacitor Converter

The configuration of a three-phase 3L FC converter is presented in Figure 2.7. Similar to the 3L NPC converter, the voltage pattern generated by a 3L FC converter has three levels 0, +*Vpos* and -*Vneg* oscillating at the switching frequency. The switching sequence required to generate the voltage pattern is also described in reference [31].

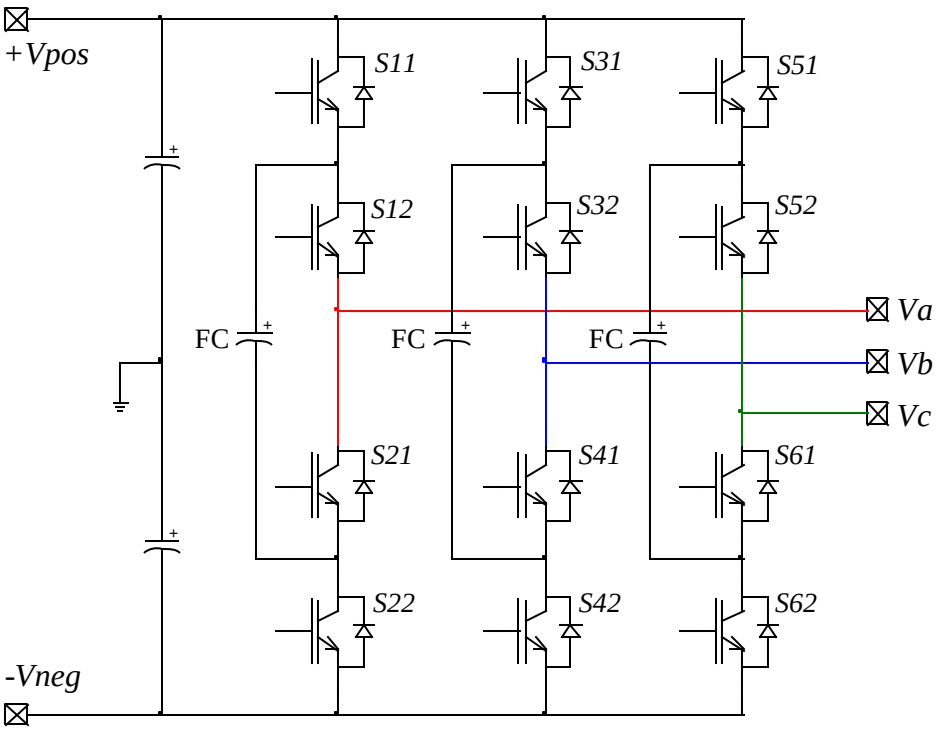


Figure 2.7: 3L FC converter topology

This topology has no additional diodes, but has additional dc capacitors known as floating (or flying) capacitors. For a three-phase unit, the main dc capacitors are shared by the three phases, but the FC are equal but independent for each phase and are connected to the mid-point connection of the upper and lower diodes on each phase leg. During normal operation, the mean

voltages of the FCs for each phase are charged at *+Vpos*, where the voltage of the main dc bus voltage is *Vdc* (*Vpos*+*Vneg*). As a result, the voltage across each IGBT switch is only half of the dc-link voltage *Vdc*. Taking phase *a* in Figure 2.7, when IGBTs *S11* and *S12* are turned ON, the output is connected to *+Vpos* and when *S11* and *S21* are ON, the output is zero (*-Vpos*+*Vpos*). When *S21* and *S22* are ON, the output is connected to *-Vneg*. States *S11* ON and *S22* ON, as well as *S12* and *S21* ON, are forbidden to avoid shorten the capacitors.

The advantages of the 3L FC topology are similar to the 3L NPC with the difference that all switches have the same duty. With the volume of capacitors largely proportional to the square of their nominal voltages, the disadvantage of this topology is the large footprint incurred by the floating capacitors [21].

2.3.2.3 Hybrid Multilevel Configurations

The generalized structure of a single-phase multilevel inverter with *n m*-level SMs (or cells) connected in series is shown in Figure 2.8.

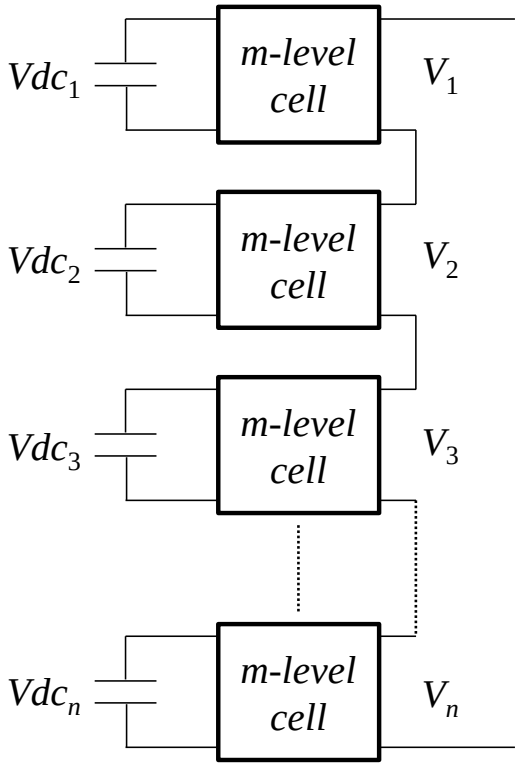
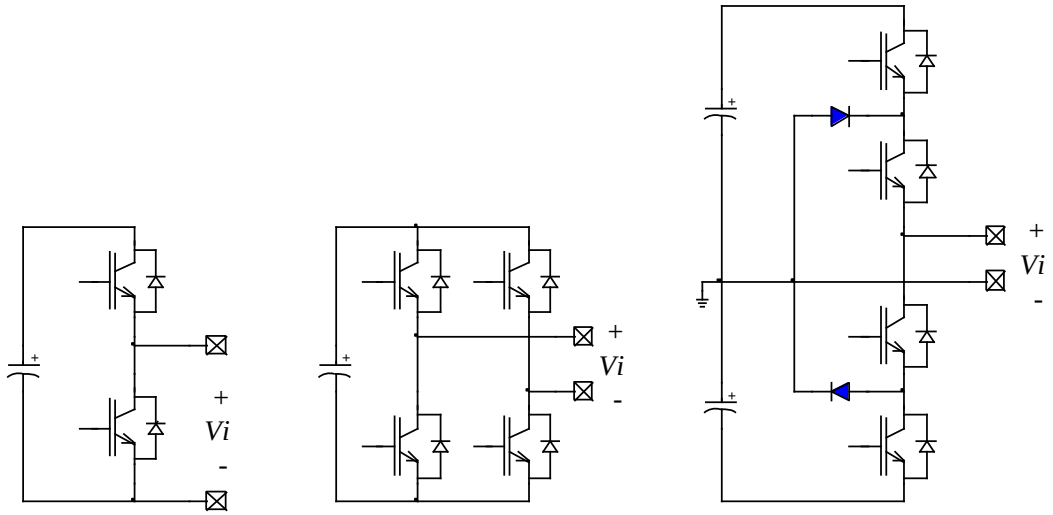


Figure 2.8: Generalized topology of a multilevel converter

A phase-to-neutral voltage waveform is obtained by adding up the output voltages of each cell V_n. It is considered that the output voltage of each cell represents equally spaced levels, where the voltage step between two adjacent levels is a function of Vdc_n. Several topologies of single-phase cells, such as those presented in Figure 2.9, can be connected in series (or cascade) to obtain multilevel waveforms. Full-bridge cells (Figure 2.9b) are usually employed in FATCS devices (STATCOM) because they use a smaller dc bus voltage level, and they present a smaller number of components than half-bridge cells with the same number of levels. On the other hand, full-bridge cells cannot synthesize voltage waveforms with an even number of levels. Although each configuration has its advantages and disadvantages, the unified analysis presented hereinafter does not depend on the arrangement adopted to obtain a given number of levels [32]. A hybrid configuration will combine different level cells in series or different modulation techniques. A multilevel configuration currently used for VSC-HVDC connects two-level cells (Figure 2.9a) in series to form the desired ac voltage configuration and is known as modular multilevel converters (MMC) [23]. As opposed to full-bridge cells, which can generate three *Vi* voltage levels (+*Vdc*, 0 and –*Vdc*), half-bridge cells can only generate two levels (+*Vdc* and –*Vdc*, or +*Vdc* and 0). Half-bridge tree-level cells (Figure 2.9c) can also produce three levels, but they require additional diodes (clamp diodes) which make this topology more onerous for multi-level converter applications.



(a) (b) (c)

Figure 2.9: Sub-modules a) Two-level cell, b) Full-bridge (H-bridge) cell, c) Half-bridge tree-level cell

2.3.3 Modular Multilevel Converters

The MMC topology is a new configuration developed for VSC-based HVDC applications. It connects two-level SMs in series to generate the ac voltage output. Figure 2.10 shows a single-phase MMC configuration including Nu SMs on the upper arm and Nl SMs on the lower arm. Each SM contains two IGBT switches and a capacitor.

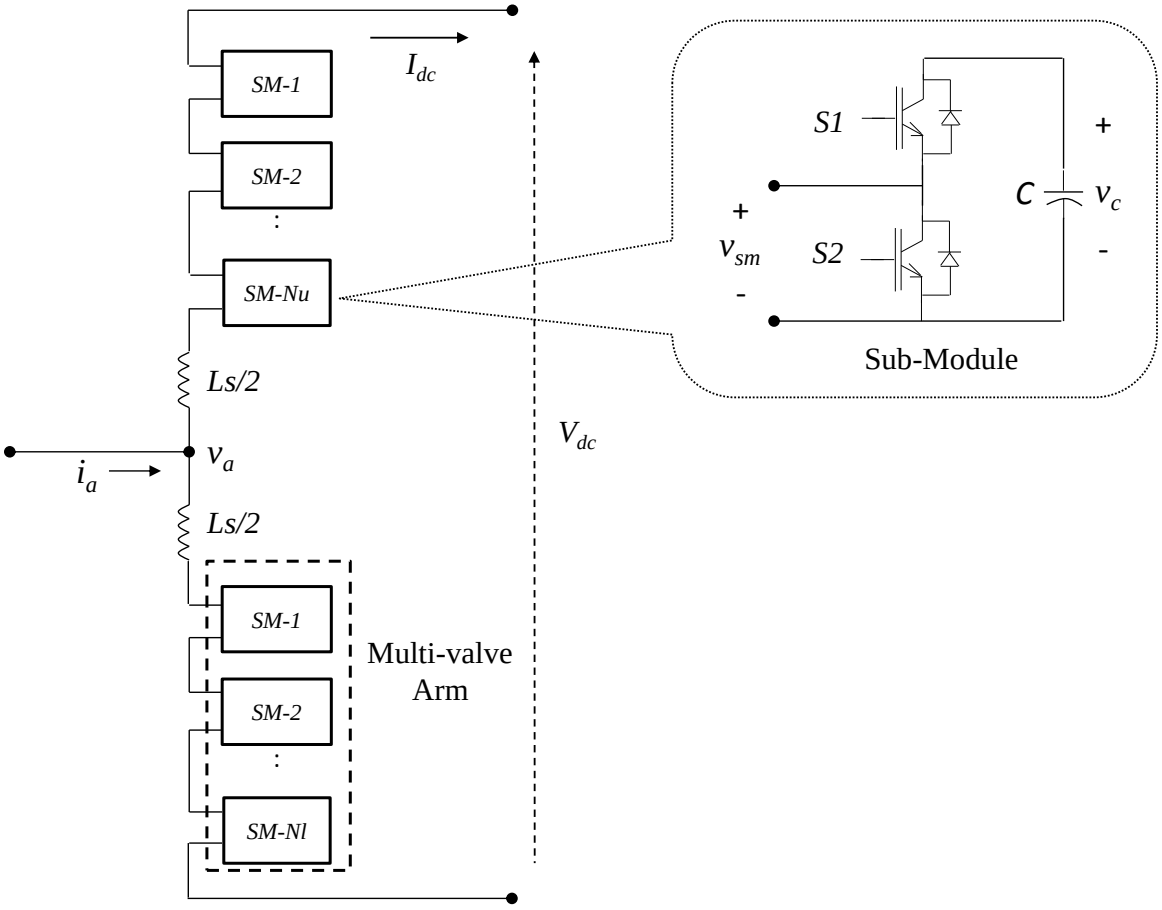


Figure 2.10: Single-phase MMC configuration

Regardless of the sign of the arm current, the voltage v_{sm} of each SM can be switched to either 0 or to the capacitor voltage v_c. By switching a number of SMs in the upper and lower arms, the voltages V_{dc} and v_a are controlled. The voltage on the capacitors are periodically measured with a typical sampling-rate in the millisecond-range and, according to their voltage value, they are sorted by software. In case of positive arm current (entering into the SM), the required number of SMs with the lowest voltages are switched on (*S1*=ON, and *S2*=OFF) and the selected capacitors are charged. When the current in the corresponding arm is negative (going out of the SM), the

number of SMs with highest voltages are switched on. By using this method, continuous balancing of the capacitor voltages is guaranteed. The MMC configuration typically includes redundant SMs, meaning a defective SM can be replaced by a redundant SM in the arm by control action without mechanical switching. This results in an increased safety and availability for this configuration [34].

The converter reactor L_S has two key functions:

- Three-phase MMCs connect the multi-valve arms in parallel on the dc side. As the generated dc voltages on each arm cannot be exactly the same, balancing currents will appear between the individual phase arms. The converter reactors help damping these balancing currents to a very low level and make them controllable by means of appropriate methods.
- The reactors substantially reduce the effects of faults arising inside or outside the converter. As a result, unlike in previous 2L and 3L VSC topologies, current rise rates of only a few tens of amperes per microsecond are encountered even during critical faults such as a short circuit between the dc terminals of the converter. These faults are swiftly detected and, due to the low current rise rates, the IGBTs can be turned off at absolutely uncritical current levels.

The voltage pattern generated by a MMC is a staircase waveform where each step corresponds the SM voltage (or capacitor voltage) v_c. Figure 2.11 shows the ac voltage waveform for a detailed 21-level MMC (20 SMs per multi-valve arm).

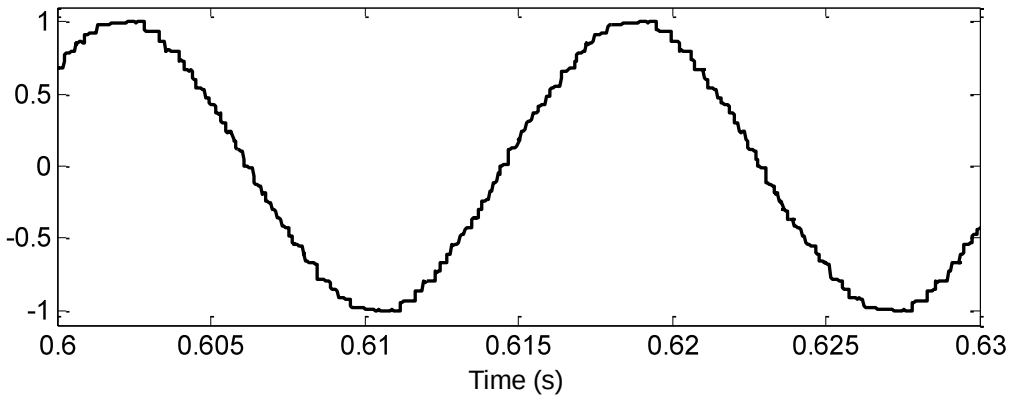


Figure 2.11: AC voltage (pu) for a 21-level MMC

It can be noted that the higher the number of SMs, the lower the harmonic content and the need for filtering. An actual MMC-based HVDC systems of 400MW will include 200 SMs per multi-valve arm on each phase. A larger system in the range of 1,000MW will contain 400 SMs per multi-valve arm forming what is known as a 401-level MMC. These large systems will not require any filter on the ac side of the converter as the voltage output will be almost a perfect sinusoidal waveform as it will be demonstrated later on. The typical dc voltage for an actual 201- and 401-level MMC is ± 200kV and ± 320kV, respectively [30], [34].

A detailed description of a three-phase MMC topology and its control system is provided in section 3.2 of this thesis.

2.4 Filtering Requirements

VSCs based on two- and three-level topologies are usually operated using sinusoidal PWM technique to control the fundamental frequency and the modulation index of the ac voltage. As previously shown in Figure 2.4 and Figure 2.6, the converter's voltage output includes a fundamental frequency plus high frequency components. Elimination of harmonics in VSCs is achieved by the use of ac filters. The series reactor will also help to filter the harmonic content. A typical VSC-HVDC scheme will include a couple of tuned filters plus a high frequency filter. The filters are tuned at the switching frequency and twice the switching frequency. The transformer connection is delta on the secondary side (converter side) in order to remove third-order harmonics. Depending on the filter performance requirements, the filters size will vary between 10-30% of the rated converter's capacity [20]. The requirements for 2L and 3L VSC filter are as follows:

$$D_h = \frac{U_h}{U_1} \approx 1.0\% \tag{2.1}$$

$$THD = \sqrt{\sum_h D_h^2} \approx 1.5\% - 2.5\%, \tag{2.2}$$

where D_h is the individual voltage harmonic distortion and *THD* is the Total Harmonic Distortion measured at the Point of Interconnection of the VSC-HVDC system. These are voltage quality performance measures. There is also a telephone influence factor (TIF) that is used as an indication of the expected telephone interference. Filters are also added on the dc side along with

smoothing reactors where the converter capacitor is installed in order to suppress harmonics. Cables on the dc side may run close to telephone lines causing interference, therefore, additional filtering may be required to minimize telephone interference from dc cables.

The high dv/dt in the switching valves may cause a high frequency noise which should be prevented from propagation to the rest of the system and outside the converter facilities. Mitigations measures are implemented at the valve level by using dumping circuits, but radio interference (RI) filter capacitors and reactors connected between the ac bus and earth are typically used.

MMC-based VSC-HVDC systems using a large number of levels (above 100) do not require ac filters to improve voltage quality as the converter output will be an almost perfect sinusoidal waveform. Harmonic content analyses for different converter levels will be studied in a further section of this report.

2.5 DC Link

The dc link in 2L and 3L VSCs is formed by the storage capacitors and the dc cable or overhead line, respectively. The primary objective of the dc side capacitor is to provide a low-inductance path for the turned-off currents and also to serve as an energy storage device. The capacitor also reduces the harmonics ripple on the direct voltage. Disturbances in the system (e.g. ac faults) will cause dc voltage variations. The ability to limit these voltage variations depends on the size of the dc side capacitor. A storage capacitor provides the corresponding VSC with a smooth dc voltage of a fixed polarity. To achieve maximum use of the power semiconductors of the VSC, the capacitor needs to be connected to the converter by a low inductive path. The size of the capacity is chosen according to the maximum dc voltage ripple tolerated [20]. It should be noted that a dc capacitor is not required in MMC configurations as the storage capacitor is now embedded in the converter's SM. This particularity will reduce the stress on the IGBT switches due to dv/dt variations.

A VSC-HVDC system cannot change voltage polarity. Power reversal is achieved by changing the direction of dc current instead. This enables the use of extruded dc cables, which are an attractive alternative to self-contained oil filled or mass impregnated paper insulated cables as used for conventional thyristor-based HVDC systems. The cable length is not limited as it would

be in case of ac transmission systems. VSC-HVDC systems use land or submarine polymer cables similar to XLPE ac cables, but with a modified polymeric insulation. Cable data for dc cables can be found in [20].

For the purpose of this thesis, the dc cables used in EMTP-RV are modeled using a wideband frequency dependent cable model [35] in order to study both dynamic and transient events on the dc side of the VSC-HVDC link.

2.6 Control System

A high level overview of the control system for a 2L (or 3L) and a MMC-based VSC was presented in section 2.2. The basic control scheme uses a vector control (Figure 2.1) which includes an outer controller that generates the current references in the $dq0$ synchronous rotating frame to the inner controller [36], [37]. The purpose of the inner current controller (or ac current controller) is to allow the (active and reactive) current through the series reactor and the transformer to be controlled. The synchronous frame rotates at the frequency obtained from the PLL which synchronizes the converters voltage with the ac voltage. The inputs to the PLL are the ac voltages of the three-phases at the Point of Interconnection (POI). The current references to the inner controller are obtained from the outer controller (or current-order controller) whose inputs are the active and reactive reference power, or the rms voltage on the converter filter. The dc voltage is also controlled through the outer controller by a current reference order. A voltage-dependent current order limiter provides control to keep the ac filter voltage within its upper and lower limits. The tap changer of the converter transformer is controlled to keep the voltage modulation ratio (m_v) within acceptable limits. The frequency can be controlled in cases where VSC-HVDC system is supplying a passive (no sources or active elements) network [38]. The reactive power control includes an ac voltage override block intended to maintain the ac voltage within acceptable pre-defined limits. The active power control, in turn, includes a dc voltage limiter that overrides the active power control in order to maintain the dc voltage within an acceptable range.

Multilevel (three levels or higher) converters present the problem of having the neutral-point voltage subject to fluctuations due to the irregular charging and discharging cycle of the upper and lower dc capacitors. This unbalance may cause excessive overvoltages on the

switching devices and on the dc capacitors. The dc-voltage regulation method used in this thesis controls the zero-sequence current and adds a zero-sequence signal to the voltage reference of the PWM [39]. MMCs on the other hand, need to balance the second-harmonic circulating currents generated by unbalances in the phase arms as well as the dc capacitor voltage at each SM. This is achieved by using a circulating current suppression control (CCSC) and a balancing control algorithm (BCA), respectively [30]. More details on the origin and mitigation of voltage and current unbalances generated in MMCs are provided in sections 3.2.1.1 and 3.2.1.2, respectively.

Under unbalanced network conditions or grid disturbances, voltage ripple is introduced into the dc link. To mitigate this effect, a control strategy that decouples positive and negative sequence inner-current loops can be implemented. This control strategy improves the dynamic response of the VSC-HVDC system as shown in [44]. The following chapter provides a more detailed description of the control system developed and used in this thesis for different VSC topologies.

2.7 Protection System

The main purpose of the protection system is to promptly remove the VSC components from service in the event of a fault. The main protection device in a VSC-HVDC system is the ac breaker which disconnects the converter and transformer from the grid removing dc current and voltage. Depending on the type of fault and converter technology, the clearing actions may go from transient currents limitation by temporary blocking the valves and control pulses to permanent blocking of the VSC and ac breaker tripping. The transient current limiter stops sending pulses to the IGBTs of the faulted phase or all three phases when overvoltage protection is enabled and is re-established once the fault is cleared. A permanent blocking, whereas, will send a turn-off signal to all the IGBT switches and they will stop conducting.

VSC-HVDC systems based on MMC technology include, in addition to the ac breaker, a press-pack thyristor on each SM in parallel to $S2$ (Figure 2.10) which is used to protect the anti-parallel diodes exposed to high currents from dc faults. Once a dc fault is detected and the IGBTs are blocked, the fast-recovery free-wheeling diodes, which have low surge current withstand capability, are exposed to damaging currents for a few cycles. The thyristor is fired during the fault allowing most of the current to flow through the thyristors and not through the diodes until the ac breaker opens [24]. Press-pack thyristors have a high capability to withstand surge currents

which make them useful in conventional LCC-HVDC applications and their use in VSC-HVDC applications will make this technology suitable for applications involving overhead transmission lines.

2.8 VSC-HVDC Applications

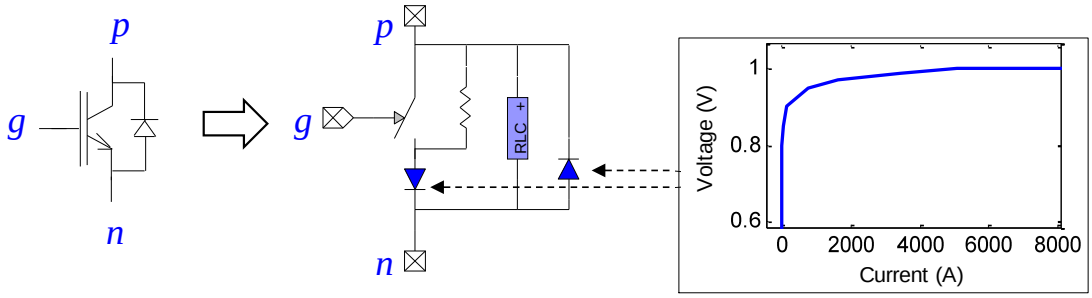
VSC-HVDC systems have the advantage of independently controlling active and reactive power and voltage which make this technology suitable for a number of applications including grid performance and operations support. Examples of applications include parallel interconnection of ac and dc systems where VSC-HVDC link can help damping oscillations in the ac systems [20]. The advantage of this technology for system restoration is considerable in terms of voltage and frequency stability during black start. VSC-HVDC will enable applications requiring asynchronous connections between two systems either back-to-back or by means of dc transmission links. This advantage increases when the connection requires the use of underground or submarine cables such as in VSC-based MTDC systems used to integrate offshore wind generation [45]-[48]. Future in-feed to dense urban cities are an attractive application of VSC-HVDC systems due to their capability to use cable systems and also to control voltage and frequency at the VSCs [38].

CHAPTER 3 DETAILED VSC-HVDC MODELS

This chapter describes the detailed VSC-HVDC models (and mathematical formulation) developed in EMTP-RV for the validation of the proposed AVMs. It starts with the first generation of VSC technologies based on 2L and 3L converters to continue with the latest generation based on MMC technology.

3.1 Two- and Three-level Converter Models

In the detailed two- and three-level converter topologies, described in sections 2.3.1 and 2.3.2, the IGBT switches are modeled using an ideal controlled switch, two non-ideal (series and anti-parallel) diodes and a snubber circuit, as shown in Figure 3.1a. The non-ideal diodes are modeled with nonlinear resistances using the classical V-I curve of a diode whose characteristic can be adjusted according to manufacturer data (Figure 3.1b). This model offers several advantages as it can accurately replicate the nonlinear behavior of switching events accounting for both switching and conduction losses. Six and twelve IGBT valves were modeled for the two- and three-level converters, respectively. Therefore, the RLC snubber circuit must be calibrated to account for losses in the case of an actual VSC system where several IGBTs are connected in series and parallel in order to withstand the design voltage and current.



(a) (b)

Figure 3.1: a) IGBT valve representation, b) Diode V-I curve

It should be noted that partial differential equations could be used to develop a lumped circuit for the IGBT valve. In [61], a complex IGBT sub-circuit is proposed and compared against a finite element model. This complex representation can accurately represent switching losses; however, they require extremely small time-steps (nanoseconds) as the switching event occurs over a very

short period of time. These types of models are not usually used for power system simulations due to excessive computing time requirements and are outside the scope of this thesis.

3.1.1 Control System

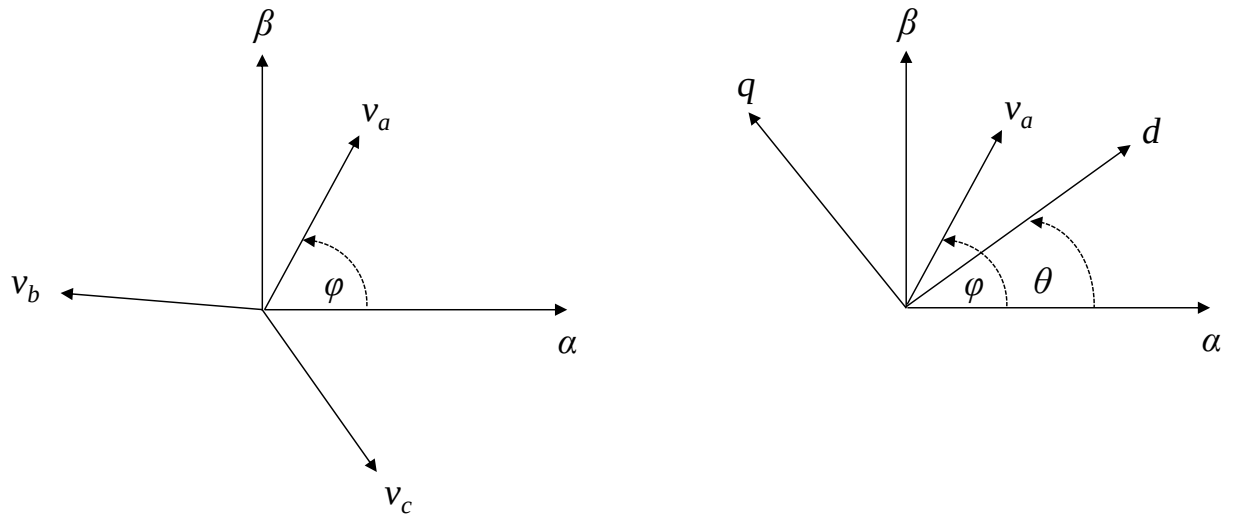
Two- and three-level based VSCs use the same control system approach which is known as vector control [36]. The method calculates a voltage time area across the equivalent reactor L (or voltage drop) which is required to change the current from present value to the reference value. The vector control operates in the synchronous rotating *dq*0-frame and its main components are the phase-locked loop (PLL), inner and the outer control blocks. The inner controller regulates the converter ac voltage (and current over the series reactor) that will be used to generate the modulated switching pattern and the outer controller regulates the current references needed to control the main VSC parameters such as power flow, ac voltage and dc voltage. Using vector control, the active and reactive power (or voltage) can be independently controlled by regulating the currents in the *dq*0-frame [36].

3.1.1.1 Synchronous *dq*0 Reference frame

The use of a rotating *dq*0-frame allows decoupled control of active and reactive power flows. A set of three-phase voltages in the *abc*-frame can be transformed into two-dimensional $\alpha\beta$ complex frame by the Clark transformation [49].

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{3}{2}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}, \tag{3.1}$$

where v_a, v_b, and v_c are the three-phase voltages in the *abc* frame, and v_α and v_β are the corresponding voltages in the $\alpha\beta$ frame (Figure 3.2a). The $\alpha\beta - dq0$ transformation is given by the Park transformation [49] using the reference frame in Figure 3.2b.



(a) (b)

Figure 3.2: Reference frames: (a) Stationary $\alpha\beta$ and (b) rotating $dq0$

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{3.2}$$

The angle θ is the transformation angle and is equal to ωt, where ω is electrical frequency in rad/s of the ac system under consideration. The direct ($\boldsymbol{T}$) and inverse ($\boldsymbol{T}^{-1}$) $abc-dq0$ transformation matrices are defined as follows:

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \boldsymbol{T} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos(\theta - 2\pi/3) & \cos(\theta + 2\pi/3) \\ -\sin(\theta) & -\sin(\theta - 2\pi/3) & -\sin(\theta + 2\pi/3) \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{3.3}$$

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \boldsymbol{T}^{-1} \begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ \cos(\theta - 2\pi/3) & -\sin(\theta - 2\pi/3) \\ \cos(\theta + 2\pi/3) & -\sin(\theta + 2\pi/3) \end{bmatrix} \begin{bmatrix} V_d \\ V_q \end{bmatrix} \tag{3.4}$$

3.1.1.2 Phase-Locked Loop

When a VSC terminal is connected to an active ac system, the frequency and phase must be detected at a pre-defined reference point in order to synchronize the converter and control system accordingly. This action is performed by the PLL circuit which synchronizes a local oscillator with a sinusoidal reference input coming from the system's ac voltage. This ensures that the local oscillator is at the same frequency and in phase with the reference voltage input.

The local oscillator is a voltage controlled oscillator (VCO). The block diagram of the PLL is shown in Figure 3.3, where V_q is the *q*-axis voltage coming from the $abc-dq0$ transformation of the voltage reference and ω_o is base system frequency. The component V_q is selected as it is proportional to $\sin(\theta)$ and $\sin(\theta)\approx\theta$ for small values of the angle θ.

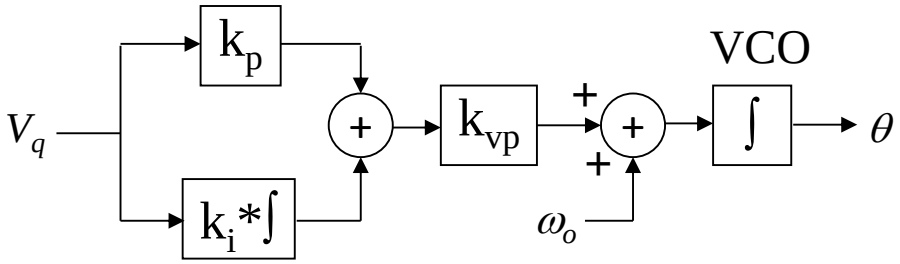


Figure 3.3: Phase-locked loop block diagram

When the converter is connected to a passive system, such as a load connection or a wind farm, the frequency is fixed to ω_o by the PLL and only the frequency oscillator is required to generate the angle θ. This control approach will be used to implement a voltage/frequency VSC controller for MTDC systems integrating offshore wind generation.

3.1.1.3 Inner Control in the *dq*0 frame

The voltage drop equation of the reactance L in Figure 2.1 is computed as follows:

$$\boldsymbol{v}_f^{abc}(t)-\boldsymbol{v}_{conv}^{abc}(t)=R\boldsymbol{i}_{conv}^{abc}(t)+L\frac{d\boldsymbol{i}_{conv}^{abc}(t)}{dt} \tag{3.5}$$

where vectors $\boldsymbol{v}_{conv}^{abc}$ and $\boldsymbol{v}_f^{abc}$ are the converter and filter's instantaneous voltages for the three phases abc. The vector $\boldsymbol{i}_{conv}^{abc}$ represents the three instantaneous line currents through the reactance *L*. It is assumed that the reactance *L* has a small resistance represented by *R*. If the voltage drop equation in (3.5) of is transformed into the $dq0$ frame (using matrix $\boldsymbol{T}$), the following equations are derived:

$$V_{conv,d}=V_{f,d}-L\frac{dI_{conv,d}}{dt}-RI_{conv,d}+\omega LI_{conv,q} \tag{3.6}$$

$$V_{conv,q} = V_{f,q} - L\frac{dI_{conv,q}}{dt} - RI_{conv,q} - \omega LI_{conv,d} \tag{3.7}$$

where $V_{conv,d}$ and $V_{conv,q}$ are the direct- and quadrature-axis representation of the converter's voltage, and $V_{f,d}$ and $V_{f,q}$ are the direct- and quadrature-axis representation of the voltage at the converter's filter. Likewise, $I_{conv,d}$ and $I_{conv,d}$ represent the current through the inductance L in the $dq0$ reference frame.

These equations are the base of the inner control loop for a balanced network. The active (P_{ac}) and reactive (Q_{ac}) power equations on the ac side of the converter are derived from the $dq0$ axis components for voltage (v_f^{abc}) and current (i_{conv}^{abc}) as follows:

$$P_{ac} + jQ_{ac} = \frac{3}{2}\begin{bmatrix} V_{f,d} \\ jV_{f,d} \end{bmatrix} \times \begin{bmatrix} I_{conv,d} & jI_{conv,d} \end{bmatrix} \tag{3.8}$$

$$P_{ac} = \frac{3}{2}(V_{f,d}I_{conv,d} + V_{f,q}I_{conv,q}) \tag{3.9}$$

$$Q_{ac} = \frac{3}{2}(V_{f,d}I_{conv,q} - V_{f,q}I_{conv,d}) \tag{3.10}$$

The power on the dc (P_{dc}) side is given by:

$$P_{dc} = V_{dc}I_{dc} \tag{3.11}$$

where V_{dc} and I_{dc} are the dc-side converter's voltage and current, respectively. Assuming there is no zero-sequence component (due to the transformer converter's delta connection), a three-phase voltages (vector $\boldsymbol{v}_{abc}$) can be decomposed into positive- (vector $\boldsymbol{v}_{abc}^{+}$) and negative-sequence (vector $\boldsymbol{v}_{abc}^{-}$) components when the network is unbalanced [44], [51].

$$\boldsymbol{v}_{abc}(t) = \boldsymbol{v}_{abc}^{+}(t) + \boldsymbol{v}_{abc}^{-}(t) \tag{3.12}$$

Applying the $\boldsymbol{T}$ matrix transformation with the corresponding rotating angle (θ for positive sequence and $-\theta$ for negative sequence), the positive- and negative-sequence components are derived in the $dq0$ rotating frame:

$$\boldsymbol{V}_{\boldsymbol{dq}}^{+} = \boldsymbol{T}(\theta)\boldsymbol{v}_{\boldsymbol{abc}}^{+} \tag{3.13}$$

$$\boldsymbol{V}_{\boldsymbol{dq}}^{-} = \boldsymbol{T}(-\theta)\boldsymbol{v}_{\boldsymbol{abc}}^{-} \tag{3.14}$$

where $\boldsymbol{V}_{\boldsymbol{dq}}^{+}$ and $\boldsymbol{V}_{\boldsymbol{dq}}^{-}$ are the positive- and negative-sequence voltage vectors for direct- and quadrature-axis components in the *dq*0 reference frame. The angle θ is derived from a generic PLL from the *dq*0 transformation applied to the phase voltage vector $\boldsymbol{v}_{\boldsymbol{abc}}(t)$. However, a filter must be added to remove the second harmonic ripple generated by the negative sequence component on the ac voltage.

If this same formulation is applied to the voltage drop equation in (3.5), we obtain the new *dq*0-frame equations [51]:

$$V_{conv,d}^{+} = V_{f,d}^{+} - L\frac{dI_{conv,d}^{+}}{dt} - RI_{conv,d}^{+} + \omega LI_{conv,q}^{+} \tag{3.15}$$

$$V_{conv,q}^{+} = V_{f,q}^{+} - L\frac{dI_{conv,q}^{+}}{dt} - RI_{conv,q}^{+} - \omega LI_{conv,d}^{+} \tag{3.16}$$

$$V_{conv,d}^{-} = V_{f,d}^{-} - L\frac{dI_{conv,d}^{-}}{dt} - RI_{conv,d}^{-} - \omega LI_{conv,q}^{-} \tag{3.17}$$

$$V_{conv,q}^{-} = V_{f,q}^{-} - L\frac{dI_{conv,q}^{-}}{dt} - RI_{conv,q}^{-} + \omega LI_{conv,d}^{-} \tag{3.18}$$

$$P_{ac} = P + P^{'}\sin(2\omega t) + P^{''}\cos(2\omega t) \tag{3.19}$$

$$Q_{ac} = Q \tag{3.20}$$

where *P*, *P'*, *P''* and *Q* are defined as follows:

$$\begin{bmatrix} P \\ Q \\ P^{'} \\ P^{''} \end{bmatrix} = \frac{3}{2}\begin{bmatrix} V_{f,d}^{+} & V_{f,q}^{+} & V_{f,d}^{-} & V_{f,q}^{-} \\ -V_{f,q}^{+} & V_{f,d}^{+} & V_{f,q}^{-} & V_{f,d}^{-} \\ V_{f,q}^{-} & -V_{f,d}^{-} & -V_{f,q}^{+} & V_{f,d}^{+} \\ V_{f,d}^{-} & V_{f,q}^{-} & V_{f,d}^{+} & V_{f,q}^{+} \end{bmatrix}\begin{bmatrix} I_{conv,d}^{+} \\ I_{conv,q}^{+} \\ I_{conv,d}^{-} \\ I_{conv,q}^{-} \end{bmatrix} \tag{3.21}$$

Neglecting the second order terms and the reactor resistance in equations (3.15) to (3.18) a proportional-integral (PI) controller can be designed as follows:

$$V_{conv,d}^{+} = V_{f,d}^{+} - \left[k_p^{+}(I_{conv,d}^{+*} - I_{conv,d}^{+}) + k_i^{+} \int (I_{conv,d}^{+*} - I_{conv,d}^{+})dt \right] + \omega L I_{conv,q}^{+} \quad (3.22)$$

$$V_{conv,q}^{+} = V_{f,q}^{+} - \left[k_p^{+}(I_{conv,q}^{+*} - I_{conv,q}^{+}) + k_i^{+} \int (I_{conv,q}^{+*} - I_{conv,q}^{+})dt \right] - \omega L I_{conv,d}^{+} \quad (3.23)$$

$$V_{conv,d}^{-} = V_{f,d}^{-} - \left[k_p^{-}(I_{conv,d}^{-*} - I_{conv,d}^{-}) + k_i^{-} \int (I_{conv,d}^{-*} - I_{conv,d}^{-})dt \right] - \omega L I_{conv,q}^{-} \quad (3.24)$$

$$V_{conv,q}^{-} = V_{f,q}^{-} - \left[k_p^{-}(I_{conv,q}^{-*} - I_{conv,q}^{-}) + k_i^{-} \int (I_{conv,q}^{-*} - I_{conv,q}^{-})dt \right] + \omega L I_{conv,d}^{-} \quad (3.25)$$

Where k_p^{+}, k_p^{-} are proportional gains and k_i^{+}, k_i^{-} are the integral gains of the controller. The control block representing the inner controller for unbalanced networks is shown in Figure 3.4.

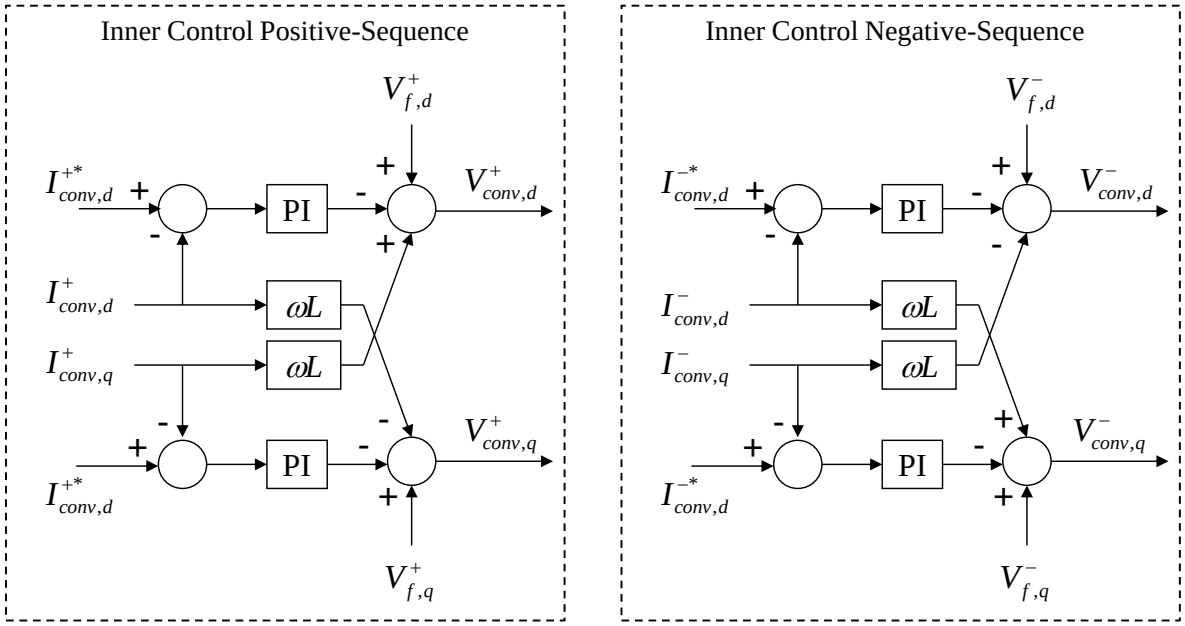


Figure 3.4: Positive- and negative-sequence inner controllers

3.1.1.4 Outer Control in the *dq*0 frame

The maximum number of controllable variables in a VSC terminal depends on the available degrees of freedom. In a decoupled *dq*0 reference frame, two variables can be independently controlled on each terminal. This approach allows implementing several types of control strategies depending on the type of grid (passive or active), ac connection (weak or strong), and application (point-to-point, multi-terminal system, offshore wind integration, etc.). The typical control strategies implemented in VSC-HVDC systems are described hereafter.

(a) *Constant ac Voltage and Frequency Control – Vac / freq*

When a VSC terminal is connected to a passive network, the ac voltage at POI should be kept constant. The PLL is phase locked at the required system frequency (50 or 60 Hz). The control block for the *Vac / freq* controller is presented in Figure 3.5.

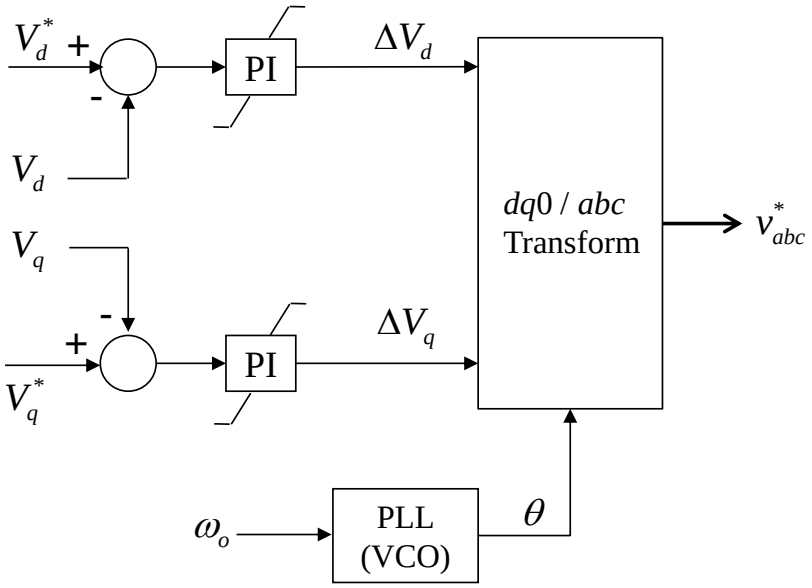


Figure 3.5: Constant voltage and frequency controller

For this specific *Vac / freq* controller, the reference voltages V_d^* and V_q^* will typically take the value of 1 and 0, respectively (for a *d*-axis voltage alignment), in order to keep the nominal voltage (1.0pu) at the VSC's POI. The voltage error is passed thought a PI controller/limiter and then the output sent to the $dq0-abc$ transformation block to generate the three phase voltage references ($\boldsymbol{v}_{\boldsymbol{abc}}^*$).

(b) *Constant Active Power and Reactive Control – P / Q*

The constant active and reactive power control is typically applied when the VSC terminal is connected to a stiff ac grid where active and reactive powers need to be independently controlled. The active power control is achieved by controlling the *d*-axis current reference $I_{conv,d}^*$ and the reactive power by controlling the *q*-axis current reference $I_{conv,q}^*$, both going into the inner

controller shown in Figure 3.4. If the ac voltage is aligned to the *d*-axis reference, then $V_{f,q}$ will be zero, and equations 3.9 and 3.10 can be rewritten as:

$$P_{ac} = \frac{3}{2} V_{f,d} I_{conv,d} \tag{3.26}$$

$$Q_{ac} = \frac{3}{2} V_{f,d} I_{conv,q} \tag{3.27}$$

$$I_{conv,d} = \frac{2P_{ac}}{3V_{f,d}} \tag{3.28}$$

$$I_{conv,q} = \frac{2Q_{ac}}{3V_{f,d}} \tag{3.29}$$

If P_{ac}^{*} and Q_{ac}^{*} are the desired (reference) active and reactive powers respectively, an accurate control of the active and reactive power is achieved by a combination of a feedback loop and an open loop control as follows.

$$I_{conv,d}^{*} = \frac{P_{ac}^{*}}{V_{f,d}} + (k_p + \frac{k_i}{s})(P_{ac}^{*} - P_{ac}) \tag{3.30}$$

$$I_{conv,q}^{*} = \frac{Q_{ac}^{*}}{V_{f,d}} + (k_p + \frac{k_i}{s})(Q_{ac}^{*} - Q_{ac}) \tag{3.31}$$

Where k_p and k_i are the proportional and integral gains of the controller, respectively. An output limiter and an error passing feedback to the integral controller are included to improve the response of the controller and to avoid output divergence as shown in Figure 3.6.

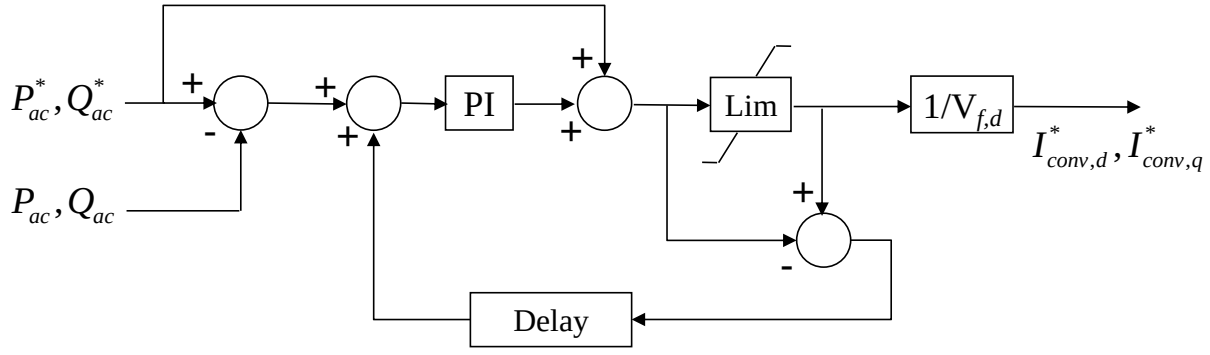


Figure 3.6: Active and reactive outer power controller

If there is no requirement for power factor control, the reference power reference Q_{ac}^{*} can be assigned a value of zero (unity power factor). A current limiter is added at the output of the outer controller in order to limit the current references ($I_{conv,d}^{*}, I_{conv,q}^{*}$) and meet the VSC's overload capability specifications. Figure 3.7 shows the current limiter control block implemented. A maximum converter current (I_{conv}) is specified for the converter which sets the direct fix limit of the *d*-axis current. Typically, a value between 1.1-1.2pu is chosen for I_{conv}. The *q*-axis current limiter ($I_{\max,q}$) is a dynamic limiter and is calculated as a function of the active power operating point and the converter capacity (I_{conv}) in order to satisfy the relation $\sqrt{I_{conv\_l,d}{}^{2} + I_{conv\_l,q}{}^{2}} \le I_{conv}$ and limit the maximum converter current output at all times.

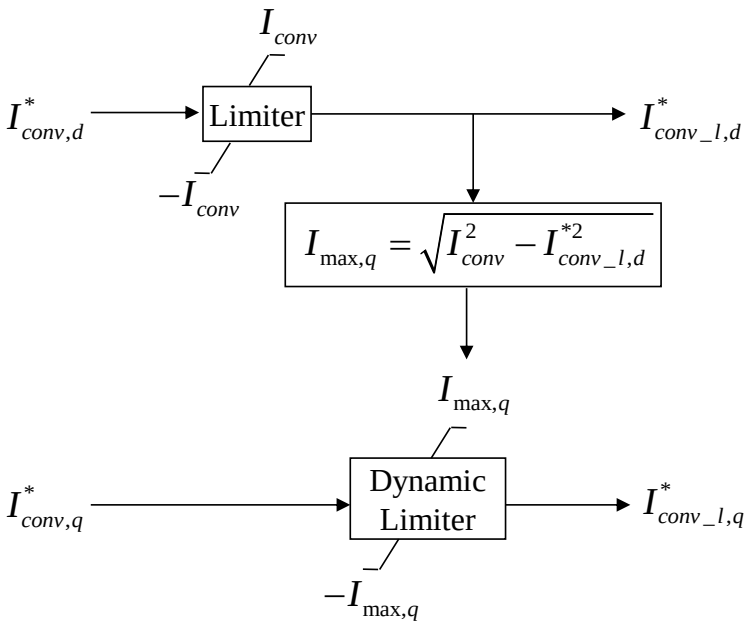


Figure 3.7: Active and reactive current limiter

(c) *Constant Active Power and ac Voltage Control – P / Vac*

Constant active power and voltage control is used when the VSC terminal is connected to a weak grid while constant active power is needed. The ac voltage is controlled by regulating the reactive power in the converter. The active power control is the same developed in b), whereas the ac voltage control is achieved by a PI regulator that calculates the voltage error and sends it to the

reactive power reference signal (Figure 3.8). The voltage reference is defined by V_{ac}^{*} and the regulating range for the ac voltage will depend on the operating conditions (active power flow) and overload capability of the VSC defined in the current limiter and specified by the IGBT's overload capability.

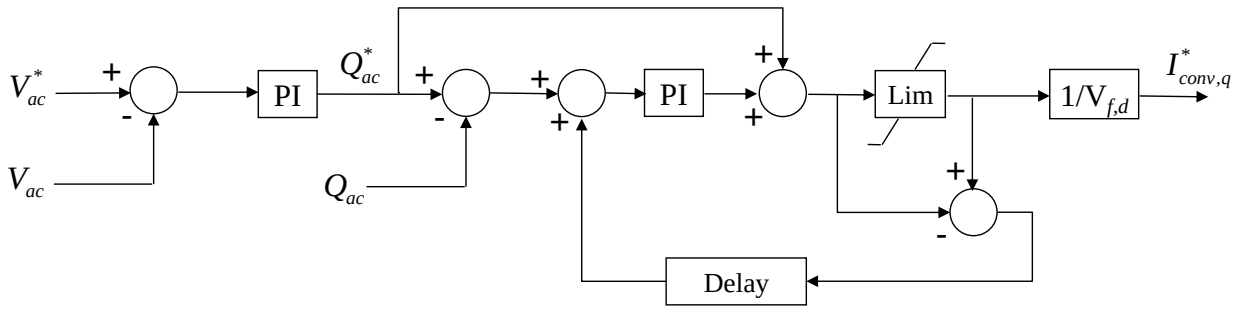


Figure 3.8: AC voltage controller

The measured input voltage V_{ac} is the positive sequence voltage estimated as follows:

$$V_{ac} = \sqrt{v_{\alpha}^{\ 2} + v_{\beta}^{\ 2}} \tag{3.32}$$

The voltage error determines the reactive power reference Q_{ac}^{*} that should achieved by regulating the control signal $I_{conv,q}^{*}$. The control is derived from equation (3.31), similar to Figure 3.6, but it includes a voltage regulator which output defines the reference reactive power Q_{ac}^{*}.

(d) *Constant dc Voltage and Reactive Power Control – Vdc / Q*

The dc voltage and reactive power control is implemented when the VSC terminal is connected to a stiff network and is required to regulate dc voltage. The reactive power control is the same described in b). Using the power balance equation between the ac and dc sides of the converter ($P_{ac} = P_{dc}$), we have:

$$V_{dc} I_{dc} = \frac{3}{2} V_{f,d} I_{conv,d} \tag{3.33}$$

$$I_{conv,d} = \frac{2 V_{dc} I_{dc}}{3 V_{f,d}} \tag{3.34}$$

Therefore, the dc voltage control can be achieved by a PI regulator as follows:

$$I^*_{conv,d} = (k_p + \frac{k_i}{s})(V^*_{dc} - V_{dc}) \tag{3.35}$$

The controller block diagram is presented in Figure 3.9.

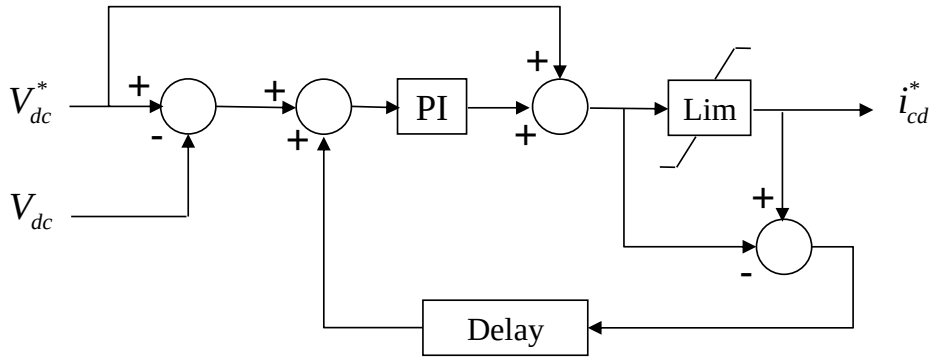


Figure 3.9: DC voltage controller

The dc voltage regulator will maintain the dc voltage by controlling $I^*_{conv,d}$ achieving active power flow balancing between ac and dc sides of the converter. The *q*-axis component will then be able to control reactive power and/or voltage. The voltage limits are defined such that the ac voltage is maintained between the maximum continuous operating voltages (typically ±10% of the nominal value depending on manufacturer specification).

(e) *Constant dc Voltage and ac Voltage Control – Vdc / Vac*

The constant dc and ac voltage controller is used when VSC terminal is connected to a weak grid and is required to maintain a constant dc voltage. The ac and dc voltage controllers are modeled in the same way as presented in Figure 3.8 and Figure 3.9, respectively. In order to maintain the ac voltage within acceptable limits and to increase the robustness of the controller, the reactive power control includes an ac voltage override limiter that acts on the $I^*_{conv,q}$ signal. Similarly, to maintain the dc voltage within pre-defined limits, a dc voltage override limiter is added to the active power controller that acts over the $I^*_{conv,d}$ signal.

(f) *DC Voltage Droop Control – Vdc _ Droop*

Droop control is typically used in MTDC systems to improve the reliability of a system conformed by several VSCs in case of outages of terminals controlling the dc voltage. The droop

control assigns a slope (*Vdc-Pdc* characteristic of Figure 3.10) to the dc voltage error signal and adds it to the power reference in the active power controller (Figure 3.6) [49].

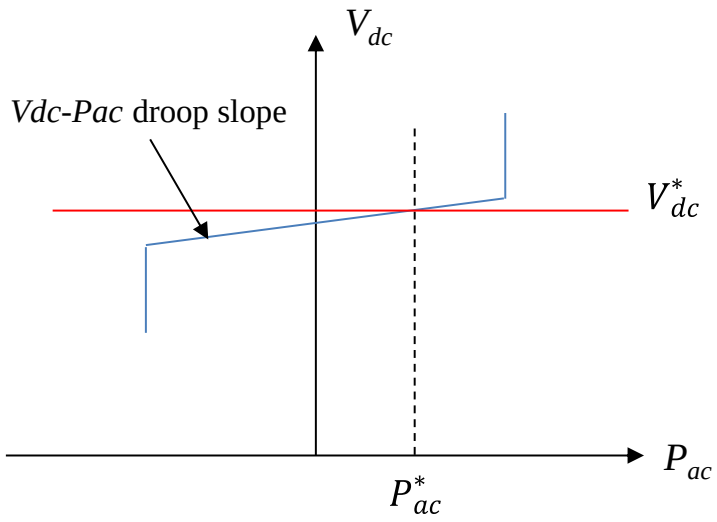


Figure 3.10 *Vdc-Pac* converter droop characteristic

The new dc voltage is calculated as follows:

$$V_{dc} = V_{dc}^{*} - Slope * P_{ac} \tag{3.36}$$

Thus, a power error is introduced in the power controller:

$$\Delta P_{ac} = \frac{1}{slope}(V_{dc}^{*} - V_{dc}) = KP(V_{dc}^{*} - V_{dc}) \tag{3.37}$$

where *slope*=1/*KP*.

The dc voltage droop control block is presented in Figure 3.11.

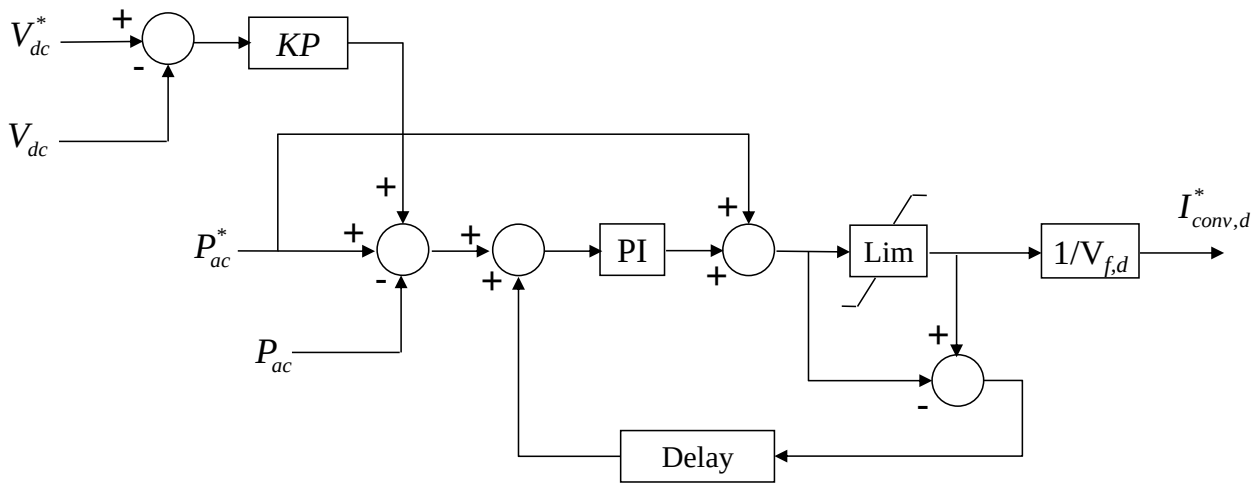


Figure 3.11: Active power controller with dc voltage droop control

(g) *Frequency Droop Control – Freq _ Droop*

Active ac systems include synchronous generators with natural frequency droop characteristics with respect to power. They also implement frequency droop control which is useful for frequency oscillations damping and compensation for power unbalance occurring at some point in the system. VSCs can also be set to contribute to the aggregate frequency droop and frequency modulation characteristics. The frequency droop control can be realized as shown in Figure 3.12 [50].

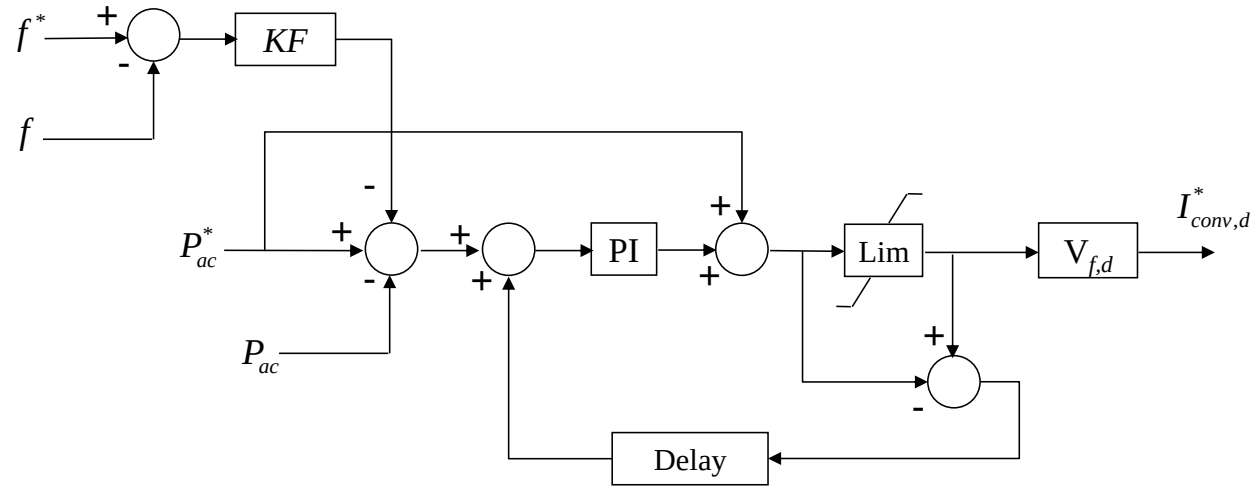


Figure 3.12: Active power controller with frequency droop control

This control works similar to the *Vdc* droop control of Figure 3.11, but using frequency error as input instead of dc voltage. This control is equivalent to droop control on synchronous generators allowing the converter to contribute to frequency regulation during load changes in case there is enough reserve margins in the converter.

The new frequency is calculated as follows:

$$f = f^* - Slope * P_{ac} \tag{3.38}$$

Thus, a power error is introduced in the power controller:

$$\Delta P_{ac} = \frac{1}{slope}(f^* - f) = KF(f^* - f) \tag{3.39}$$

where *slope*=1/*KF*.

3.1.2 Modulation Technique

Several modulation techniques have been developed for two- and three-level VSCs. Among the most typical are the carrier-based pulse-width modulation (PWM) [29] and the space vector modulation (SVM) [52] techniques. The modulation approach used in this thesis, and described in this section, is the carrier-based PWM technique which is the preferred method for VSC-HVDC applications. The SVM technique was not implemented in the detailed VSC model as this technique is more suitable for low and medium voltage applications.

Carrier based PWM is the most widely used method for pulse-width modulation in 2L and 3L converters. The method employs individual carrier modulators in each of the three phases. The reference voltage vector ($\boldsymbol{v}^*_{abc}$) contains the three sinusoidal voltages in steady-state that are generated by the inner controller (Figure 3.4). The vector $\boldsymbol{v}^*_{abc}$ forms a symmetrical three-phase system that is compared with a high-frequency triangular carrier signal v_{cr} which is common to the three individual phases (See Figure 3.13 and Figure 3.14 for 2L and 3L converters, respectively).

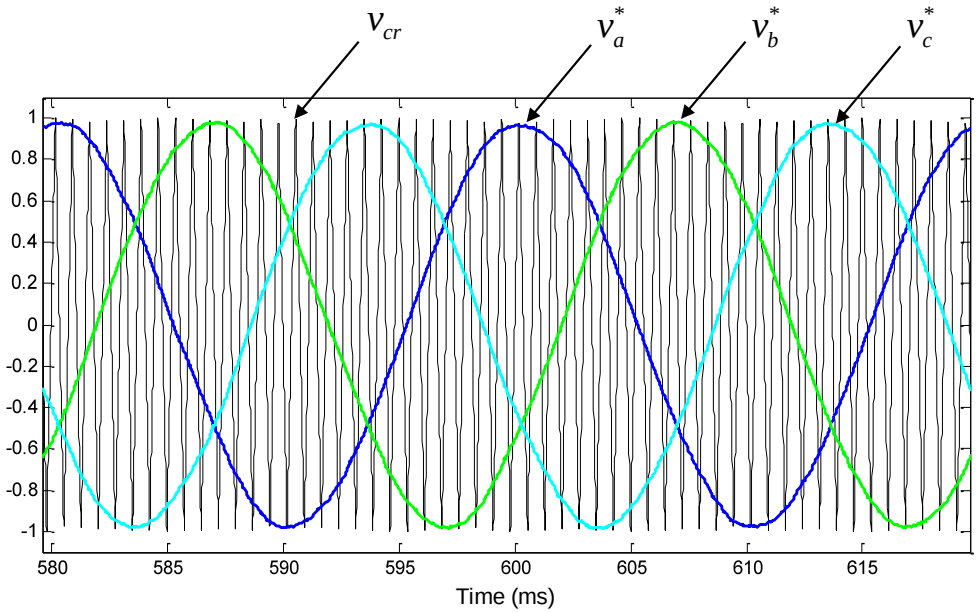


Figure 3.13: Voltage references and PWM triangular carrier waveforms for a 2L VSC

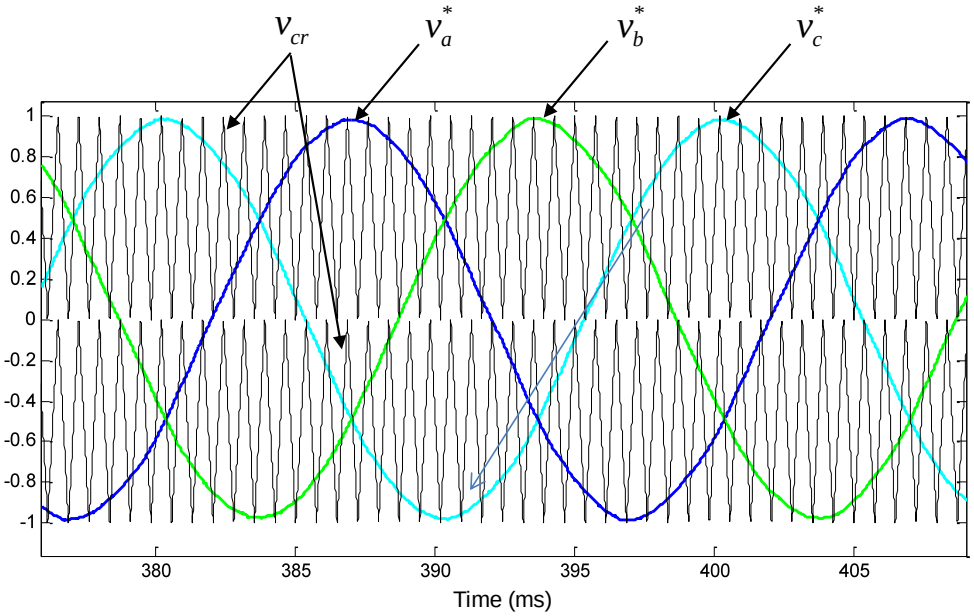


Figure 3.14: Voltage references and PWM triangular carrier waveforms for a 3L VSC

The switching frequency f_{sw}, which is multiple of the fundamental system frequency f_1, allows fast modulation and efficient elimination of low frequency harmonics. The output of the comparator block between the carrier and reference voltages is a digital signal whose value is 1

when the reference is greater than the triangular carrier and 0 when the reference voltage is smaller than the carrier signal. The comparator output corresponds to the switching pattern (pulse trigger) of the IGBT valves which is shown in Figure 2.4 and Figure 2.6 for 2L and 3L converters, respectively.

The reference signal or control signal is used to modulate the valve's duty ratio and has the frequency of the fundamental ac system voltage. The output voltage of the VSC will not be a perfect sinusoidal waveform and will contain harmonic content. The amplitude of the fundamental modulated waveform is defined by the voltage modulation ratio m_{v_a} (for phase a) which is determined as follows:

$$m_{v\_i} = \frac{\hat{v}_i}{\hat{v}_{cr}}, \quad i = a,b,c \tag{3.40}$$

where $\hat{v}_i$ is the peak value of the fundamental converter voltage and $\hat{v}_{cr}$ is the peak value of the triangular carrier. Therefore, the converter ac voltage is defined as:

$$v_i = m_{v\_i} \cdot F_i(t) \cdot \frac{V_{dc}}{2}, \quad i = a,b,c \tag{3.41}$$

With $F_i(t)$ being the sinusoidal control or reference function for phase *i* coming from the $dq0-abc$ transformation, and V_{dc} is the dc voltage.

The harmonic content on the ac voltage of 2L VSCs appears as sidebands frequencies centered around the switching frequency and its multiples, that is, around harmonics f_{sw}, $2f_{sw}$, $3f_{sw}$, and so on. In theory, the frequencies at which voltage harmonic occurs in 2L converters are [38]:

$$f_h = jf_{sw} \pm kf_1, \quad j = 1,2,3...\infty \tag{3.42}$$

For odd values of *j*, the harmonics exist only for even values of *k*; and for even values of *j*, harmonics exist only for odd values of *k*.

In the case of 3L VSCs, harmonics appears as sidebands frequencies centered around two times the switching frequency ($2f_{sw}$) and the multiples of $2f_{sw}$.

$$f_h = j(2f_{sw}) \pm kf_1, \quad j = 1,2,3...\infty \tag{3.43}$$

3.2 Modular Multilevel Converter Model

The last generation of VSCs is known as modular multilevel converter topology (MMC). This topology, briefly described in section 2.3.3, aggregates multiple two-level SMs in series to generate the desired ac voltage output. The detailed MMC model developed as part of this thesis is depicted in Figure 3.15. The DM, developed for validation purposes, is inspired on a real MMC-HVDC system planned to interconnect the 400 kV systems of France and Spain. The MMC is based on the preliminary design of this interconnection that will include two independent symmetric monopolar MMC-HVDC links each one containing two MMC terminals with a rated transmission capacity of 1,059MVA and a dc voltage of ±320kV. It is expected that this project will be the most powerful MMC-HVDC link in operation by 2013.

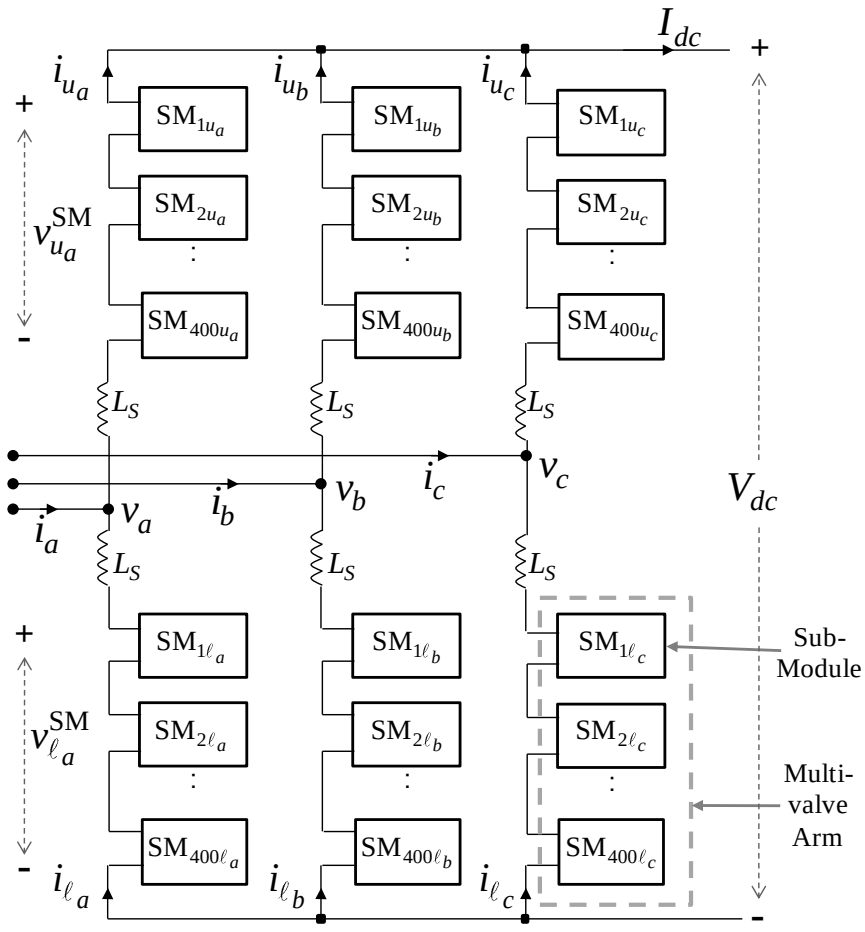


Figure 3.15: Detailed MMC topology

The MMC design considers 800 SMs per phase (400 SMs per multi-valve arm). Figure 3.15 shows the MMC topology where each SM (Figure 3.16) contains a capacitor *C* and two IGBT switches (S1 and S2).

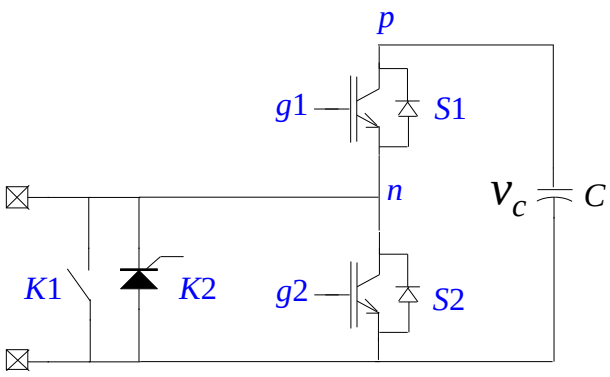


Figure 3.16: MMC sub-module

At any instant during normal operation, only one of the two switches (S1 or S2) is ON. As a result, when the switch S1 is ON (S2 is OFF) the voltage of the *i*th SM is v_C and when the switch S2 is ON (S1 is OFF) the SM voltage is zero. The arm reactor L_S helps controlling and balancing circulating currents in the phase arms, and also limiting fault currents [24]. It has a value of 15% on the system impedance base. The IGBT switches are modeled using an ideal controlled switch, two non-ideal (series and anti-parallel) diodes and a snubber circuit (Figure 3.1a).

The non-ideal diodes are modeled as nonlinear resistances using the classical diode function. The switch K1 in Figure 3.16 is a high-speed bypass switch used to increase safety and reliability of the MMC in case of SM failure [22]. K2 is a press-pack thyristor used to protect the MMC semiconductors and cables from high fault currents. The detailed model developed in this thesis includes 4,800 ideal switches and 9,600 non-ideal diodes per MMC. This number excludes the press-pack thyristors used for protection which are triggered only during dc faults. The ideal switches K1 were not modeled.

The capacitor *C* is selected with a value such that the ripple of the SM voltages is kept within a range of ±10%. To achieve this, the energy stored in each SM should be in the range of 30-40 kJ/MVA [53]. The SM capacitance C is then estimated as follows:

$$C = \left(2\, S\, E_{MMC}\right) / \left(6\, N_{arm}\, v_C^2\right) \tag{3.44}$$

Where E_{MMC} is the energy per MVA stored on each MMC, *S* is the nominal capacity of the MMC (1,059MVA), N_{arm} is the number of SMs per multi-valve arm (400) and v_C is the nominal value for the SM capacitor (1.6kV in our case). For a stored energy of 30kJ/MVA, the resulting capacitor value is 10 mF. The converter transformer is a 1,059MVA, 400/333kV three-phase transformer with its secondary winding connected in delta to block the zero-sequence voltages generated by the MMC. The converter transformer impedance $Z_T = j\omega L_T$ is 18%.

The MMC-HVDC system includes two 70km underground transmission cables. The 320kV single-core cables are modeled using a wideband frequency-dependent model [35].

In addition to serve as reference to validate averaged models, the DM offers several advantages such as increased accuracy of sub-module modeling (nonlinearities, switching losses, etc.), capability to account for special switching states and direct representation of unbalanced conditions and internal faults within the converters.

3.2.1 Control System

The control system employed by MMC-based HVDC systems is very similar to the vector control used by two- and three-level converters described in section 3.1.1. It includes the inner and outer controllers as well as the PLL. The voltage time area across the transformer/converter equivalent reactor is now computed as $L_T + L_S/2$, where L_S is the arm reactor and L_T is the transformer reactor. In addition to the vector control, the MMC includes a dc voltage balancing control algorithm (BCA) intended to balance the capacitor voltage v_C on each SM. Voltage unbalances between the arm phases of the MMC introduce circulating currents containing a second harmonic component which not only distorts the arm currents, but also increases the ripple of SM voltages, thus impacting the rating of SM capacitors and switches. Therefore, a circulating current suppression control (CCSC) must be implemented to eliminate the second harmonic current distortion. The BCA and CCSC controls are described in the next sections.

3.2.1.1 Balancing Control Algorithm

The capacitor voltage on each SM must be balanced and kept the same during normal operation. To achieve this, the SMs voltage v_C must be monitored and the capacitors switched ON and OFF based on the BCA. The BCA proposed in [40] measures the capacitor voltages at

any instant and sorts them before selecting the upper and lower SM to switch ON. Reference [41] proposes a different BCA where an SM is switched ON and OFF any time the reference signal crosses one of the triangular signals from the PS-PWM. An alternative BCA, that uses an individual PI control for each SM, is proposed in [54], but adding individual PI controllers to each SM significantly increases the simulation time as the number of levels increases.

The detailed MMC model developed in this thesis employs an improved version of the BCA presented in [40]. In this case, the number of SMs to be switched ON is determined from two time-dependent switching functions $N_{up}(t)$ and $N_{low}(t)$ that are defined by the modulation control strategy. The combination $N_{up}(t)+N_{low}(t)$ gives the total number of SMs per multi-valve arm (400 in our case). There are several switching combinations for a specified number of SMs in the upper and lower arms. Therefore, the capacitor voltage values, and also the direction of the arm currents, are used to select $N_{up}(t)$ and $N_{low}(t)$ at each time.

To achieve the SM voltage balancing on each arm, the SM capacitor voltages are measured and sorted in descending order as follows:

- If the upper (or lower) arm current is positive, the SMs with the lowest voltages are selected and switched on. Consequently, the corresponding SM capacitors are charged and their voltages increased.
- If the upper (or lower) arm current is negative, the SMs with the highest voltages are selected and switched on. Consequently, the corresponding SM capacitors are discharged and their voltages decreased.

Regardless of the direction of the upper (or lower) arm currents, if a SM is disconnected (switched-off), the corresponding capacitor will be bypassed and its voltage will remain unchanged.

The BCA procedure, presented in Figure 3.17, was programmed and tested in Matlab (FORTRAN code) and then converted into a Dynamic Link Library (DLL) that can be read by EMTP-RV engine at each time step. It should be noted that the DLL inputs are the measured SM capacitor voltages and arm currents and the outputs are the switching functions including the state (ON/OFF) of each SM. In order to improve the efficiency of the balancing algorithm, a trigger control that activates the BCA only when $N_{up}(t)$ or $N_{low}(t)$ changes is included. This

avoids switching the SMs at each solution time point unnecessarily reducing the stress and switching losses in the IGBT valves.

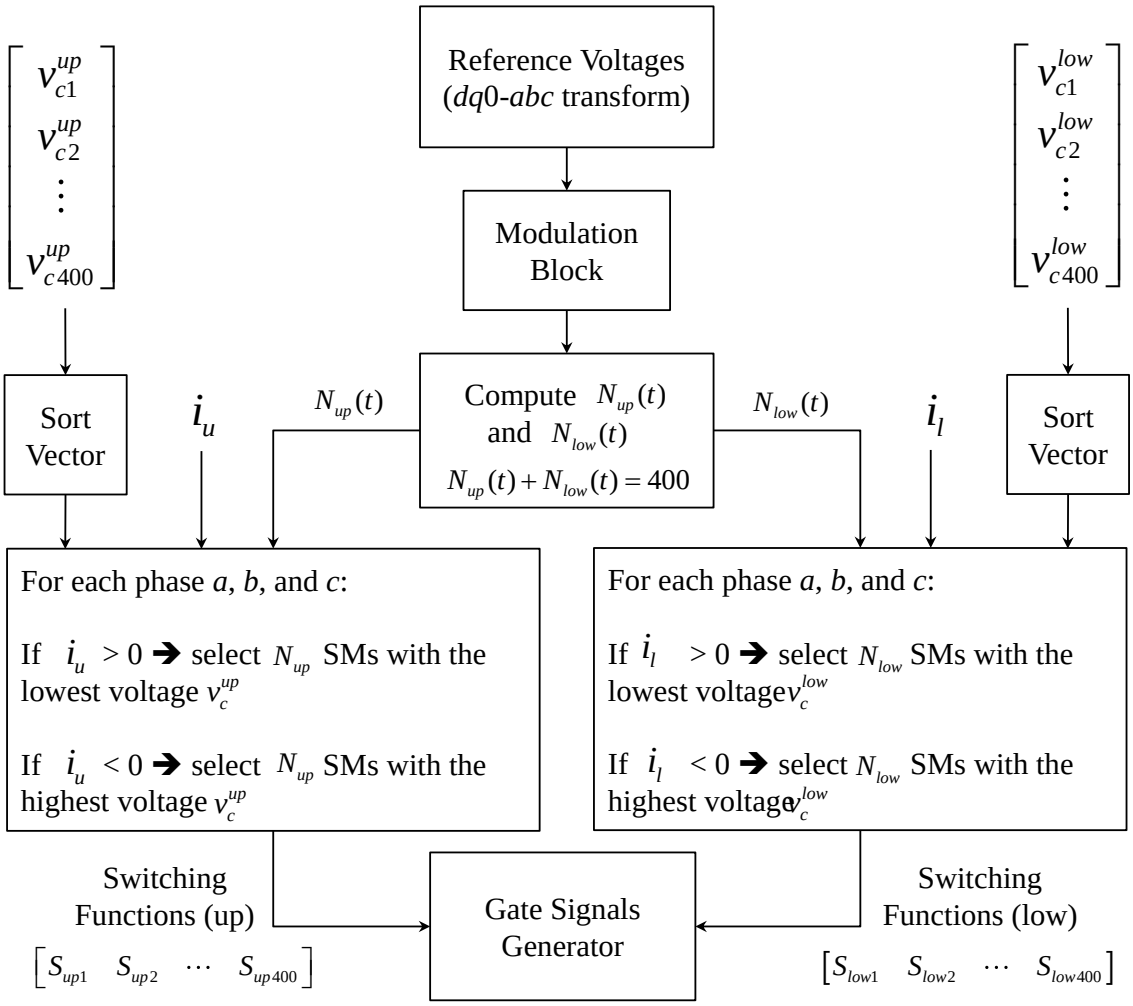


Figure 3.17: BCA procedure

3.2.1.2 Circulating Current Suppression

The second harmonic component of the circulating currents can be eliminated by using an active control over the modulated voltage [55], [56] or by adding a parallel capacitor (resonant filter) between the mid-points of the upper and lower arm inductances on each phase [53]. The DM developed here employs the circulating current suppression control (CCSC) proposed in [56]. The circulating currents flow through the three phase arms of the converter without affecting the AC-side voltages and currents. It has been proved in [57] that the circulating currents in the MMC are generated by the voltage differences among each phase arm, and they

appear in the form of negative sequence with the frequency being twice the fundamental. These second harmonic currents increase the *rms* values of the arm currents resulting in higher converter power losses. The circulating current on each phase is superimposed to a dc current component that provides the actual dc/ac power transfer. As a result, the upper/lower arms difference current consists of two terms: a dc component equal to one-third of the total dc current and an ac component corresponding to the second harmonic circulating current. For each phase *j* (with $j = a,b,c$), the upper and lower arm currents are computed as [30]:

$$i_{u_j} = \frac{i_j}{2} + \frac{I_{dc}}{3} + i_{z_j} \tag{3.45}$$

$$i_{\ell_j} = -\frac{i_j}{2} + \frac{I_{dc}}{3} + i_{zj} \tag{3.46}$$

$$i_a + i_b + i_c = 0 \tag{3.47}$$

$$i_{za} + i_{zb} + i_{zc} = 0 \tag{3.48}$$

Therefore, the circulating current (ac second harmonic) is given by:

$$i_{zj} = \frac{i_{u_j} + i_{\ell_j}}{2} - \frac{I_{dc}}{3} \tag{3.49}$$

Where i_{zj} ($j = a,b,c$) are as follows [56]:

$$i_{za} = I_{2f} \sin(2\omega_0 t + \varphi_0) \tag{3.50}$$

$$i_{zb} = I_{2f} \sin(2\omega_0 t - \frac{2\pi}{3} + \varphi_0) \tag{3.51}$$

$$i_{zc} = I_{2f} \sin(2\omega_0 t + \frac{2\pi}{3} + \varphi_0) \tag{3.52}$$

The CCSC is achieved by adding a voltage control signal to the MMC voltage reference output (from the inner controller). The voltage control signal comes from a new inner control intended to eliminate the second harmonic component in the *dq*0 reference frame. The proposed CCSC structure is presented in Figure 3.18. The difference current for each phase is calculated by adding the respective upper and lower arm currents (i_{u_j} and i_{l_j}). They are then transformed to the

double line-frequency (negative-sequence) $dq0$ rotational frame (i_{zd} and i_{zq}). Both the reference values of the second harmonic component (i_{zd}^{*} and i_{zq}^{*}) are set to zero to eliminate the circulating currents. The voltage control signals are obtained using PI controllers with cross-coupling compensation. Finally, the three reference values are calculated by the inverse $dq0-abc$ transformation and added to the MMC reference voltages from the main inner controller in Figure 3.4.

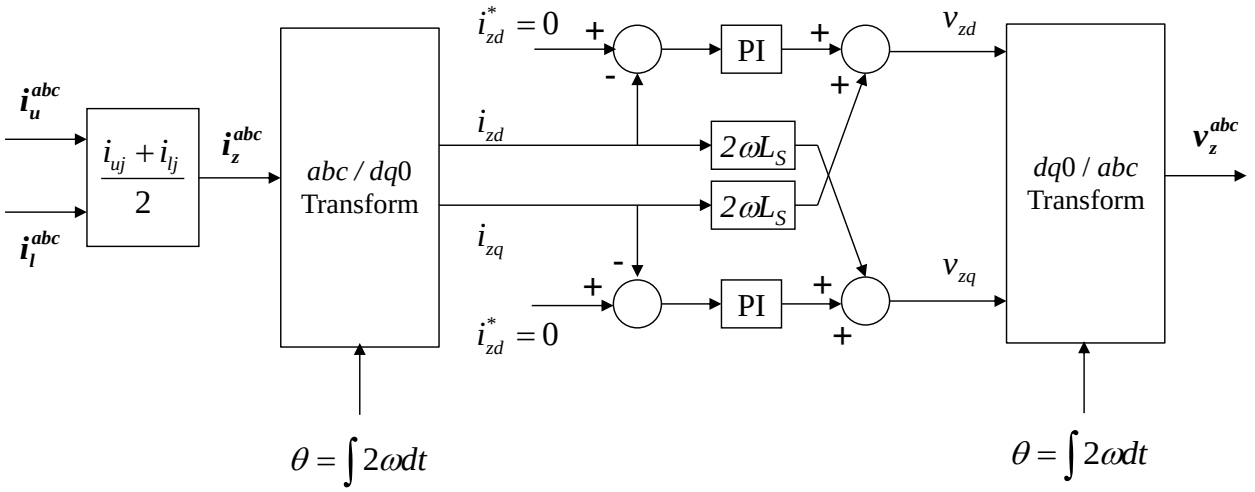
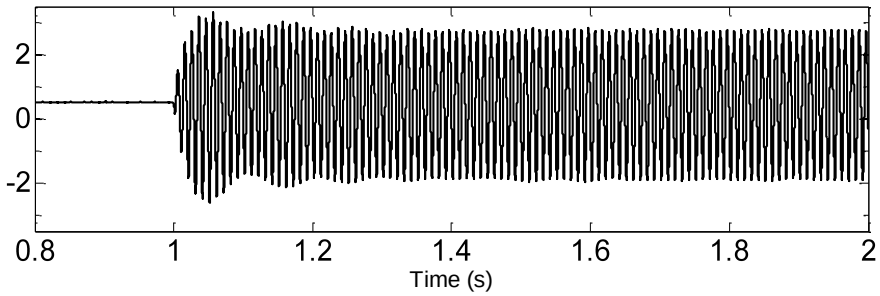
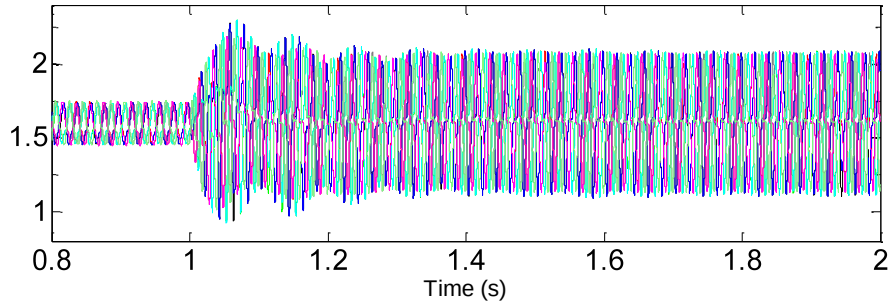


Figure 3.18: CCS control block

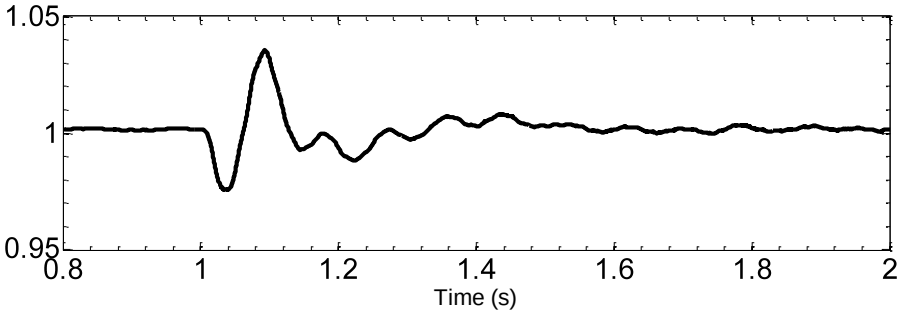
Figure 3.19a-d shows the effect of the CCSC on the circulating current and on SM voltage ripples (showing several SMs) before and after the control removal at t=1s . It is observed that the CCSC eliminates the ac (2nd harmonic) component of the circulating current and also decreases the capacitors voltage ripple from 30% to 8%.



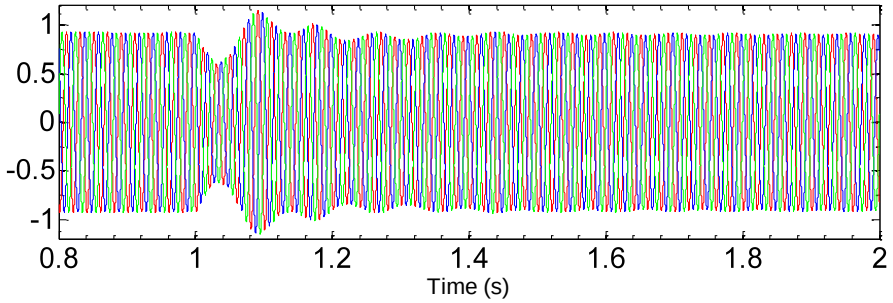
(a) Circulating current (kA)



(b) SM voltage ripples (kV)



(c) Converter dc voltage (pu)



(d) Converter ac currents (pu), phase-*a* (red), phase-*b* (blue), phase-*c* (green)

Figure 3.19: CCSC for a 401-Level MMC, CCSC is removed at t=1s

3.2.2 Modulation Technique

Traditional modulation techniques for MMCs include Phase-Disposition Modulation (PD-PWM) [40], Phase-Shift Modulation (PS-PWM) [41], Space-Vector Modulation (SV-PWM) [23], and the improved Selective Harmonic Elimination method (SHE) [22]. As the number of levels increases in MMCs, PWM and SHE techniques become cumbersome for EMT-type simulations. Therefore, more efficient staircase-type methods, such as the Nearest Level Control (NLC) technique, have been proposed in [42] and [43]. The MMC models developed in this

thesis employs the NLC technique proposed in [42]. The NLC approach, presented in Figure 3.20, determines the reference functions n_{uj}^* and n_{lj}^* for the upper and lower levels respectively from the reference voltage on each phase j (v_j^*). The upper and lower references are then divided by the SM capacitor nominal voltage (v_{c_nom}) and rounded to the nearest (upper or lower) level. The outputs are the time-variant modulated functions N_{uj} and N_{lj} which define the number of SMs to switch ON at each instant on the upper and lower arms, respectively. It should be noted that $N_{uj} + N_{lj} = 400$ at all times.

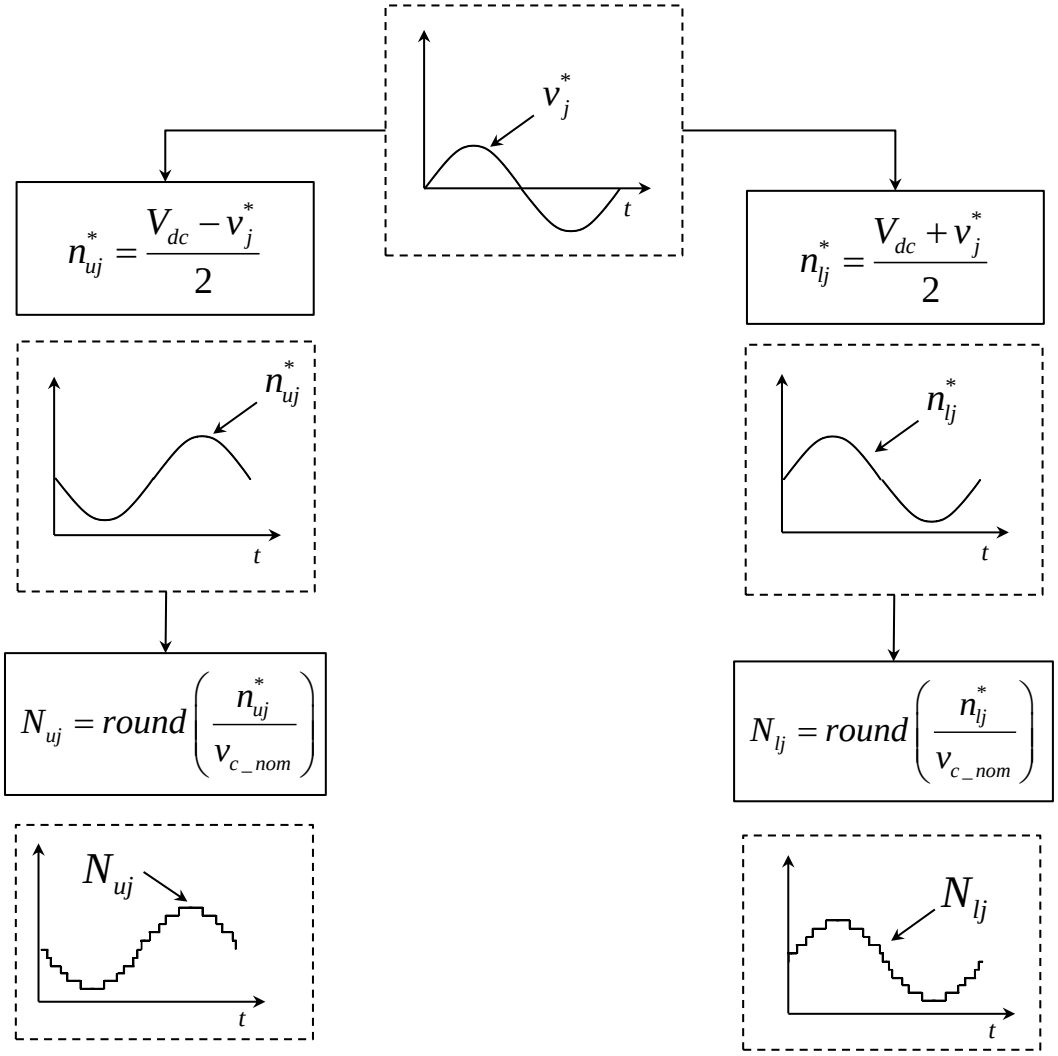


Figure 3.20: NLC modulation control block

3.2.3 Protection System

The main protection device employed by MMC systems is the ac breaker. It will operate to protect the system for during ac and dc disturbances. In the case of dc faults, the press-pack thyristor (K2 in Figure 3.16) is used to protect the converter semiconductors and cables from high fault currents. The anti-parallel free-wheeling diodes used in VSC have a low capacity for withstanding surge current events without damage. This would be the case during a dc fault where the diodes would have to withstand a high fault current without damage until the circuit breaker opens which in most cases is at least three cycles [22]. To avoid this, the fast thyristor switch (K2) is added to bypass the SM allowing the current to flow through the fast thyristor instead of the diodes. Once a dc fault is detected, the MMC is blocked (the IGBT valves are switched off) and the fast thyristor is switched on within a few microseconds (40μs in our proposed model), allowing the fault current to flow from the ac to the dc side systems through the antiparallel free-wheeling diodes for only a short period of time. After a few cycles the main ac breaker is open and the fault cleared. This technology makes the HVDC transmission based on MMCs suitable for overhead transmission lines, an application previously reserved entirely for conventional LCC-HVDC systems.

CHAPTER 4 AVERAGE-VALUE MODELS FOR VSC-HVDC SYSTEMS

The main purpose of developing average-value models is to replicate the average response of switching devices, converters, and control systems by using simplified functions and controlled sources. These models have been successfully developed in the past for low power applications; however, the averaging methodology remains under development for high-voltage high-power systems applications [14]-[17]. This chapter describes the averaging theory, presents existing and proposes new averaging methods applicable to VSC-HVDC systems [16], [28], [30].

4.1 Averaging Theory for Power Converters

In order to understand the theory applicable to averaging modeling in power converters, it is necessary to better understand the converter topologies and sub-modules components. A typical power-electronic based module is composed of a switching device and additional passive elements (such as inductors, capacitors, and resistors) that take part in the energy conversion process. In addition to the input and output power ports, switching modules may also have a control input through which the controllable switches (transistors, thyristors, etc.) are turned on and off according to a specific control strategy and modulation approach [5]. The switching frequency and modulation technique chosen will depend on many factors including the converter's topology, application and type of switches, and may vary in a wide frequency range from several times the fundamental ac frequency (50/60Hz) to hundreds of kHz.

4.1.1 DC-DC Switching Module

A basic IGBT-based DC-DC module is realized using a switched-inductor or switched-capacitor valve as shown in Figure 4.1. Opening and closing the controllable switch (IGBT) using PWM voltage or current control schemes enables energy conversion from the input source side at one dc voltage level to a different level at the output terminal. The energy in each module is first stored in the inductor (or the capacitor) and then released to the output side. Typical switching frequency of the valves may be in the range from tens to hundreds of kHz. For the voltage and/or current ripple to remain within acceptable levels, appropriate filters are designed at the input and output terminals.

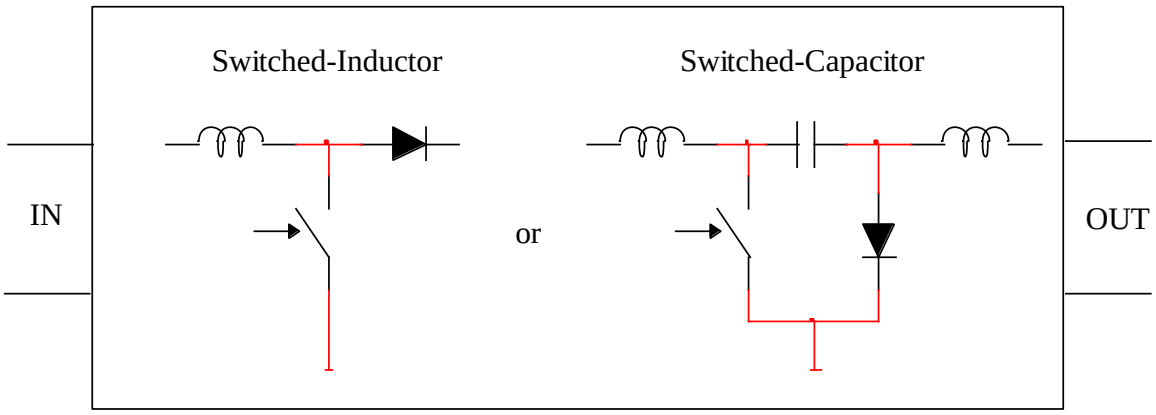


Figure 4.1: Basic switched-inductor and switched-capacitor modules

The instantaneous ON/OFF conducting states of the active (IGBT) and passive (Diode) switches determine the topology of the switching module. When the converter operates in steady state, a sequence of topologies will become repetitive within each switching interval defining a certain switching pattern. This repetitive pattern of topologies, in turn, defines the operating mode of a given switching valve. The prototypical switching interval varies for different converters and is the basis for the averaging window when developing average-value models.

For example, the switched-inductor valve of Figure 4.1 can have three topological states: (i) when the controlled switch is ON and the diode is OFF; (ii) when the switch is OFF and the diode is ON; and (iii) when both switch and diode are OFF. The typical inductor current waveform (i_L) for this switching module is shown in Figure 4.2 for different operational modes [5]. An operational mode can be characterized by a sequence of repeated topologies and is a function of the loading conditions. Changes in load conditions might lead to a change in the topologies and hence the mode of operation. In continuous conduction mode (CCM), each switching interval T_S is divided into two subintervals d_1T_S and d_2T_S (Figure 4.2a) corresponding to the topologies (i) and (ii). The variables d_1 and d_2 are the so-called relative duty cycles, which are defined such that $T_S = d_1T_S + d_2T_S$.

In discontinuous conduction mode (DCM), the switching pattern also includes the third topological state (iii) in which both switches are off and the current stays at zero for the duration of that subinterval as shown in Figure 4.2b. Hence, the switching interval is divided into three

subintervals such that $T_S = d_1 T_S + d_2 T_S + d_3 T_S$. DC-DC converter modules are not used in VSC-based converters; therefore, they are not studied in great detail in this thesis.

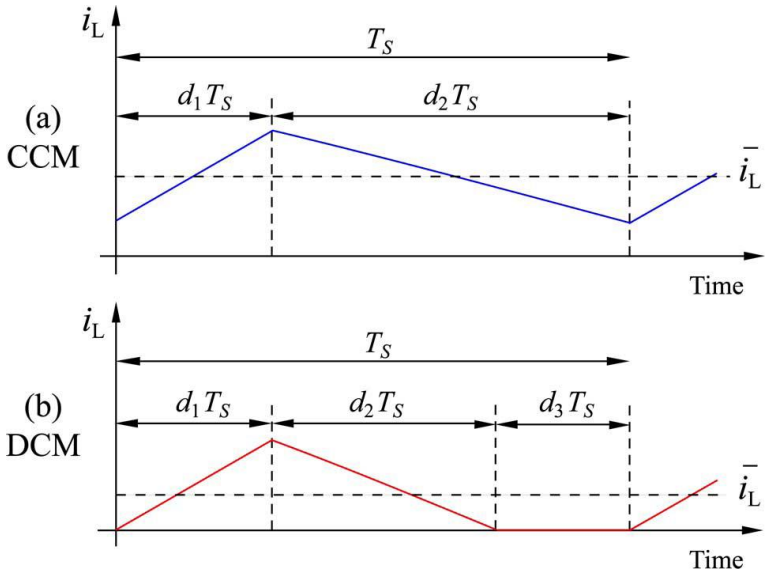


Figure 4.2: Current for switched-inductor module during CCM and DCM operation

4.1.2 AC-DC Switching Module

A three-phase ac-dc IGBT-based converter may be realized using switching modules as presented in Figure 2.3 for a 2L converter. Depending on whether the upper or the lower switches are conducting, each phase terminal can be connected to either the upper or the lower rail, or left floating if none of the switches are conducting. In general, such converter systems provide bi-directional energy flow during steady state and/or transients. Figure 2.5 shows a 3L converter which basic advantage over the two-level converter is the inclusion of the OFF-state allowing lowering the harmonic distortion of the ac voltage. The additional voltage level is obtained using the neutral-point of the two capacitors connected in series. Depending on the state of the switch and the direction of the phase current, each phase can be connected to either the lower rail, the neutral-point, or the upper rail.

In the three-phase 2L and 3L VSCs, the switching frequency is typically much higher than that of LCCs. For high power frequency applications, the switching frequency may be on the order of several kHz. This allows modulating the voltages and/or currents on the ac side with the desired quality that it can approach ideal sinusoidal waveforms. The typical ac voltage and

current waveforms of the PWM VSCs are shown in Figure 4.3 and Figure 4.4 for the 2L and 3L converters, respectively.

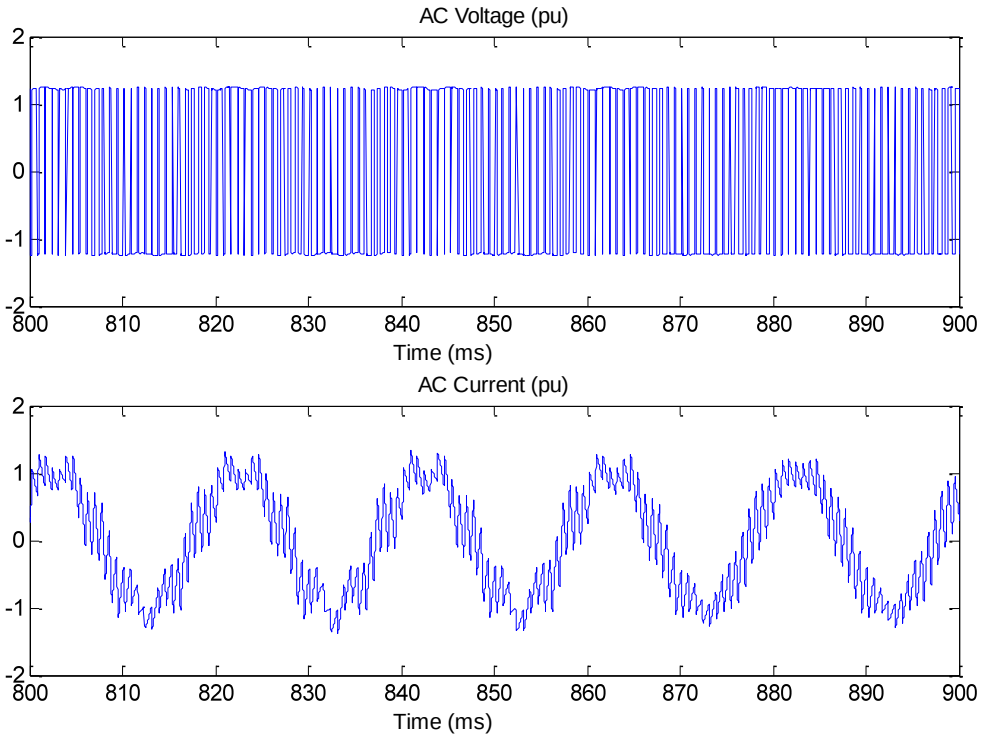


Figure 4.3: Voltage and current waveforms for a 2L VSC

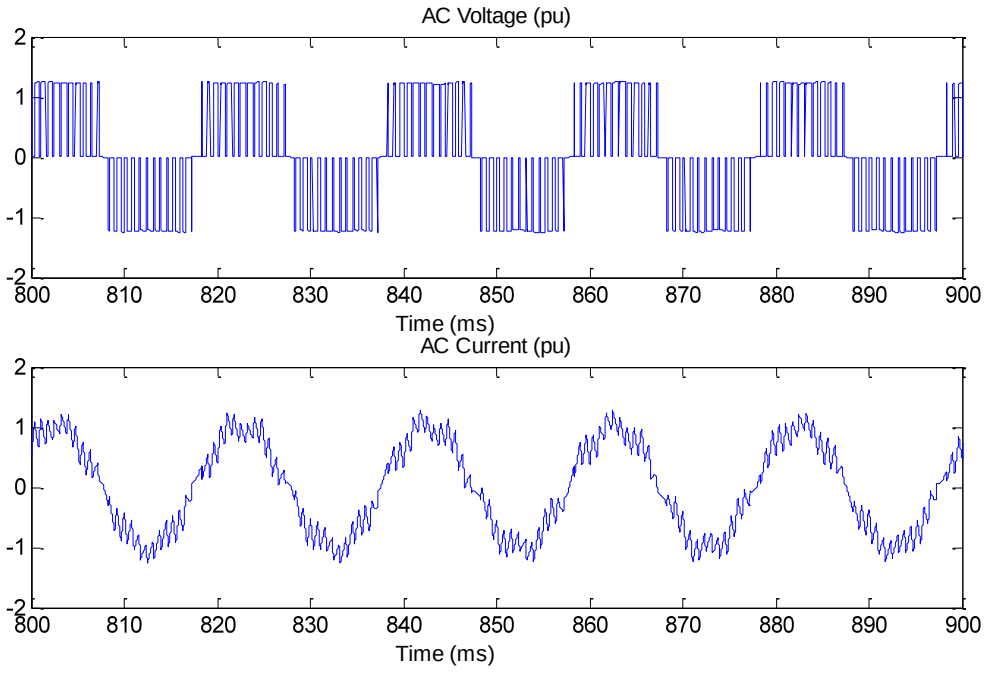


Figure 4.4: Voltage and current waveforms for a 3L VSC

As noted in Figure 4.3, the phase-to-ground voltage takes only two values (positive and negative levels); however, for the 3L converter waveforms depicted in Figure 4.4, the phase-to-ground voltage takes three values (positive, zero, and negative levels).

The switching interval $T_S = 1/f_{sw}$ for the voltage waveform is divided into two subintervals $d_1 T_S$ and $d_2 T_S$ (Figure 4.5) corresponding to the positive and zero status of a 3L VSC. The variables d_1 and d_2 are such that $T_S = d_1 T_S + d_2 T_S$. The relative duty cycles will vary with time and are derived from the intersection between the sinusoidal voltage control reference and the triangular carrier function of the PWM.

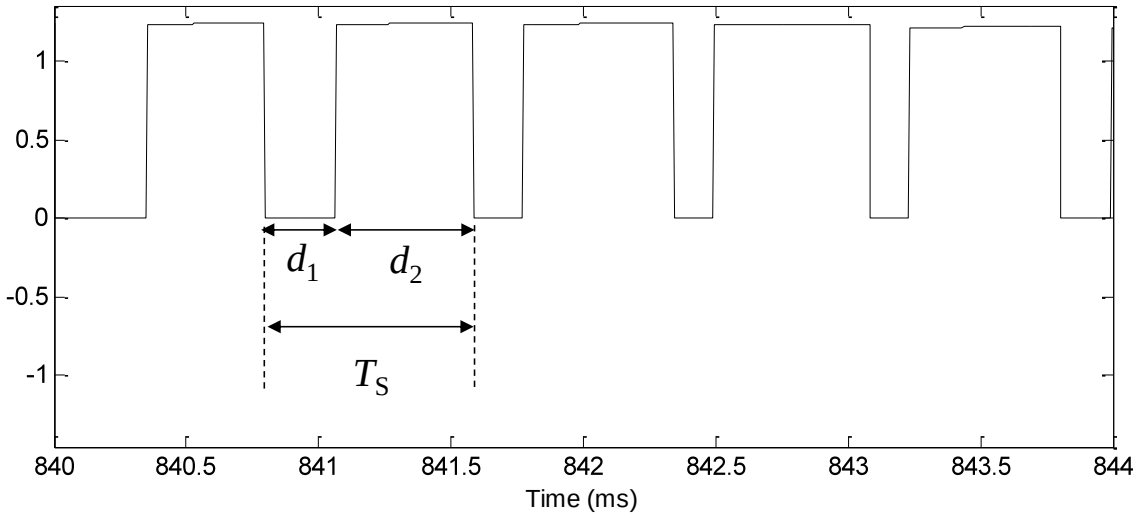


Figure 4.5: Voltage waveform for 3L VSC during steady-state operation

For both 2L and 3L converters, it is observed that the phase current essentially consists of the fundamental sinusoidal component with the superimposed high-frequency switching ripples. The amount of high frequency harmonics and switching intervals in the phase current depends on the PWM strategy and the switching frequency.

4.1.3 Generalized Averaging Theory

The averaging theory used for system studies assumes that the ripple due to valve switching can be neglected. Therefore, instead of looking at the instantaneous values of currents and voltages that contain high frequency ripple, a dynamic average-value that is defined over the length of a switching interval T_S could be used [58]:

$$\overline{f}(t) = \frac{1}{T_S} \int_{t-T_S}^{t} f(s)ds \tag{4.1}$$

where $\overline{f}(t)$ may represent the voltage or current. From the averaged inductor current in the dc-dc converter of Figure 4.2, it can be observed that the duty cycles will be constant in steady state and may also represent slower dynamics of the converter during transients. The input and output voltages are often filtered using large capacitors that in effect do the averaging. The averaged (or filtered) variables are useful for design of controllers and analysis of dynamic interactions of converter circuits [5]. The idea represented by equation (4.1) can be extended such that the resultant averaged model captures also higher-order harmonics and dynamics. This is referred to as the extended or generalized averaging [2], and is especially instrumental in modeling of resonant converters.

The concept of averaging can also be extended to ac-dc PWM converters. However, simple averaging of the ac variables using (4.1) over the switching interval will not yield the desired result. In this case, the ac side variables first have to be transformed using an appropriate synchronously rotating *dq*0 reference frame as described in section 3.1.1.1. The direct and quadrature components of the phase current (and voltage) in steady state are composed of a dc constant term plus a high frequency ripple in the same interval T_S. Since the *dq*0 variables have a dc component that is constant in steady state, they can be used for averaging using equation (4.1) in the same way as the variables in the dc-dc converter. The current on the dc side will also contain some ripple due to the IGBTs switching which often requires the use of large capacitors on the dc link for filtering. This allows the use of the averaging concept defined by (4.1) for dc currents.

In the following sections, average-value methods applicable to VSC-based HVDC systems are proposed. Methodologies to build average-value models for dc-dc converters can be found in [5] and are not included here as they are not part of the scope of this thesis.

4.2 Average-value Models for VSC-HVDC Systems

The objective of average-value models is to replace the switching modules with continuous blocks or functions that represent the averaged behavior of the switching valve within a switching interval. Obtaining the AVMs generally requires detailed analysis of the switching valves and

accurate averaging of the converter waveforms. This section presents existing and new methods and concepts for developing average-value models applicable to ac-dc converters used in VSC-based HVDC systems.

4.2.1 AVMs for Two- and Three-level VSCs

Two AVM methods are presented here for 2L and 3L converters which are the first generation of the VSC-HVDC technology. The first approach is based on *dq*0-frame averaged components [5]. The second method is a new approach using phase components and is based on the use of controlled voltage and current sources to average the instantaneous fundamental behaviour of currents and voltages on each side of the VSC [16].

4.2.1.1 AVM in the *dq*0 Reference Frame

As described earlier, the ac variables must be expressed in an appropriate reference frame in order to convert them to constant dc parameters. Typically, the *dq*0 converter reference frame is used as described in Chapter 3. Depending on the converter topology and application, the dynamic AVM can be structured in the form of equivalent sources circuits as shown in Figure 4.6.

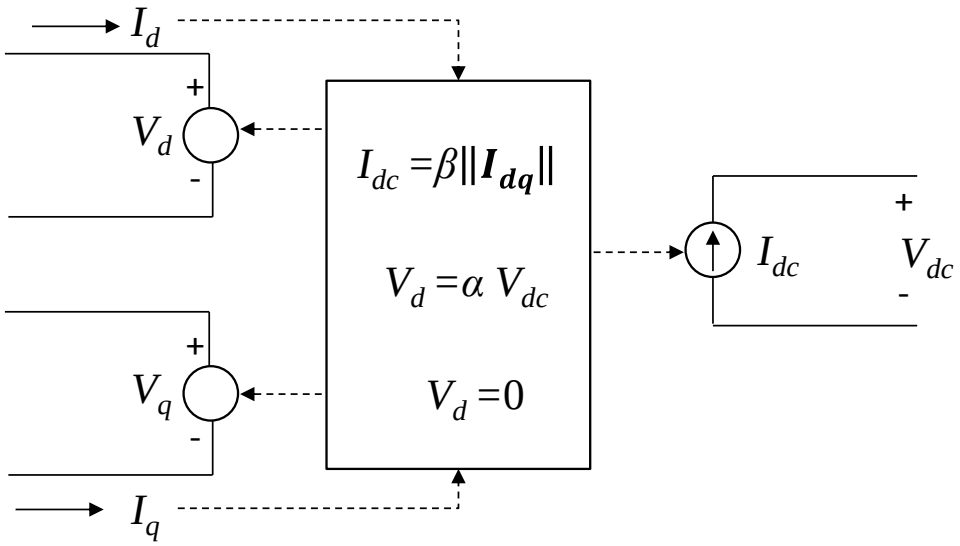


Figure 4.6: VSC AVM using algebraic parametric functions in the *dq*0 frame

Since the switching valves of the two- and three-level converters do not contain any energy storage components, the voltages and currents on the ac side can be related to the dc side

variables through functions that are purely algebraic [5]. In particular, the voltages on the ac and dc side are related as follows:

$$\left\|\boldsymbol{V}_{\boldsymbol{dq}}\right\| = \sqrt{V_d{}^2 + V_q{}^2} = \alpha V_{dc} \tag{4.2}$$

Where α is an algebraic function and $\boldsymbol{V}_{\boldsymbol{dq}}$ the ac converter voltage vector in the *dq*0 reference frame. The dc current can be expressed as:

$$I_{dc} = \beta \left\|\boldsymbol{I}_{\boldsymbol{dq}}\right\| = \beta \sqrt{I_d{}^2 + I_q{}^2} \tag{4.3}$$

where β is another algebraic function and $\boldsymbol{I}_{\boldsymbol{dq}}$ converter current vector in the *dq*0 reference frame. Both α and β depend on the type of inverter and its operating condition. Equations (4.2) and (4.3) can be established by applying the power conservation principle to the converter. In particular, looking at the ac side, the three phase power can be written as:

$$P_{ac} = \frac{3}{2}\left\|\boldsymbol{V}_{\boldsymbol{dq}}\right\| \cdot \left\|\boldsymbol{I}_{\boldsymbol{dq}}\right\| \cos(\phi) \tag{4.4}$$

where ϕ is the power factor angle. Assuming an ideal (lossless) converter, the power calculated on the ac side is equal to the power on the dc link. Therefore, the dc bus current can be derived as:

$$I_{dc} = \frac{P_{ac}}{V_{dc}} = \frac{3}{2}\alpha \cos(\phi) \cdot \left\|\boldsymbol{I}_{\boldsymbol{dq}}\right\| \tag{4.5}$$

Finally, comparing (4.3) and (4.5), β is obtained as:

$$\beta = \frac{3}{2}\alpha \cos(\phi) \tag{4.6}$$

Since the angle ϕ depends on the load, the value of β also depends on loading conditions. The angle may be expressed in terms of the components of the *dq*0 voltages:

$$\phi = \tan^{-1}\left(\frac{V_d}{V_q}\right) - \tan^{-1}\left(\frac{I_d}{I_q}\right) \tag{4.7}$$

The values of the parameters α and β for several commonly-used modulation strategies are summarized in [5]. The average-value model shown in Figure 4.6 assumes that the ac voltage is calculated from the control system (voltage reference out of the PWM) and the dc voltage is available from the dc circuit measurements. The ac side currents become the input of the AVM circuit and are derived from the network model on the ac side. The dc current is calculated as a function of the parameter α and the ac currents in the *dq*0 frame.

Since this model works on the *dq*0 reference frame, their variables are averaged, and therefore, cannot properly model transient events. Besides, losses are not represented in this model.

4.2.1.2 AVM in the Phase Reference Frame

The new proposed phase reference frame AVM includes voltage-controlled sources on the ac side of the VSC and current-controlled sources on the dc side as shown in Figure 4.7. The high-frequency harmonic contents in voltage and current waveforms are not represented as the reference voltage on the ac side of the converter is derived from the *dq*0-*abc* transformation.

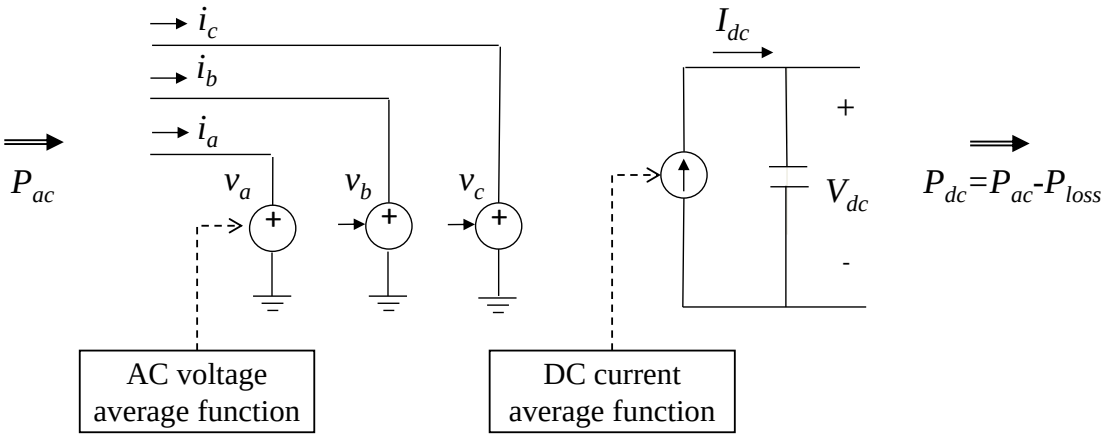


Figure 4.7: AVM model for 2L and 3L VSCs

The amplitude and phase of the voltages are independently controlled in the *dq*0 reference frame. The AVM of the VSC is based on three voltage-controlled sources (v_a, v_b, v_c) on the ac side and a current-controlled source I_{dc} on the dc side. The AVM voltage-controlled sources are represented as follows [16]:

$$v_j = \frac{1}{2} V_{dc}\, m_{v\_j}, \qquad j = a,b,c \tag{4.8}$$

where m_{v_j} corresponds to the voltage modulation function and is obtained from the *dq*0-*abc* transformation of the reference voltages V_d^* and V_q^*. The dc side of the VSC is derived using the principle of power conservation, meaning the power on the ac side must be equal to the power on the dc side plus the converter losses.

$$P_{ac} = P_{dc} + P_{loss} \tag{4.9}$$

Neglecting converter losses, the controlled current I_{dc} on the dc side is computed as follows:

$$v_a\, i_a + v_b\, i_b + v_c\, i_c = V_{dc}\, I_{dc} \tag{4.10}$$

Replacing equation (4.8) in (4.10), we obtain:

$$I_{dc} = \frac{1}{2}\left(m_{v\_a}\, i_a + m_{v\_b}\, i_b + m_{v\_c}\, i_c\right) \tag{4.11}$$

The controls of the VSC remain unchanged in the AVM in order to ensure fast control and accurate dynamic response. The selected converter topology and modulation technique are irrelevant for the proposed AVM as high- or low-frequency modulation will only impact the filtering requirements on the ac side of the VSC, but not the magnitude and phase angle of the fundamental ac components. Converter losses, however, will be impacted by the converter topology and switching frequency, and should be taken into account in the AVM.

The power balance equation (4.9) can be rewritten as:

$$\frac{P_{ac}}{V_{dc}} = \frac{1}{2} \sum_{j=a,b,c} m_{v\_j}\, i_j = I_{dc} + \frac{P_{loss}}{V_{dc}} \tag{4.12}$$

The converter current loss function I_{loss} is defined as:

$$I_{loss} = \frac{P_{loss}}{V_{dc}} = R\frac{I_c^2}{V_{dc}} \tag{4.13}$$

with,

$$I_c = \frac{1}{2} \sum_{j=a,b,c} m_{v\_j}\, i_j \tag{4.14}$$

where R is the equivalent resistance of the converter losses and represents both switching and resistive losses, and I_c is the equivalent dc current including converter losses. The new dc current, excluding converter losses, is then derived from equations (4.12) and (4.14) as follow:

$$I_{dc} = I_c - I_{loss} \tag{4.15}$$

The value of R is selected using the VSC losses from the DM which are close to 2% for 2L and 3L VSCs. It should be noted that a parallel resistance on the dc side of the VSC does not allow modeling current-dependent losses as the latter will depend on the dc voltage only. Therefore, the loss function in (4.13) is preferred to model the VSC losses.

Hereafter, the AVM based on fundamental frequency representation described in this section is named as AM. The detailed models for two- and three-level VSCs are identified as DML2 and DML3, respectively. The accuracy of the AM is observed in Figure 4.8 which compares the ac voltages on the grid (HV) side of a VSC transformer against the 2L and 3L detailed VSC models (DML2 and DML3). The detailed 3L (dashed-dotted black line) and 2L (dashed red line) representations provide an accurate sinusoidal waveform (very lithe harmonic content) after the converter voltage signal is filtered. As anticipated, the AM (solid blue line) only represents the fundamental (50Hz) component of the ac voltage.

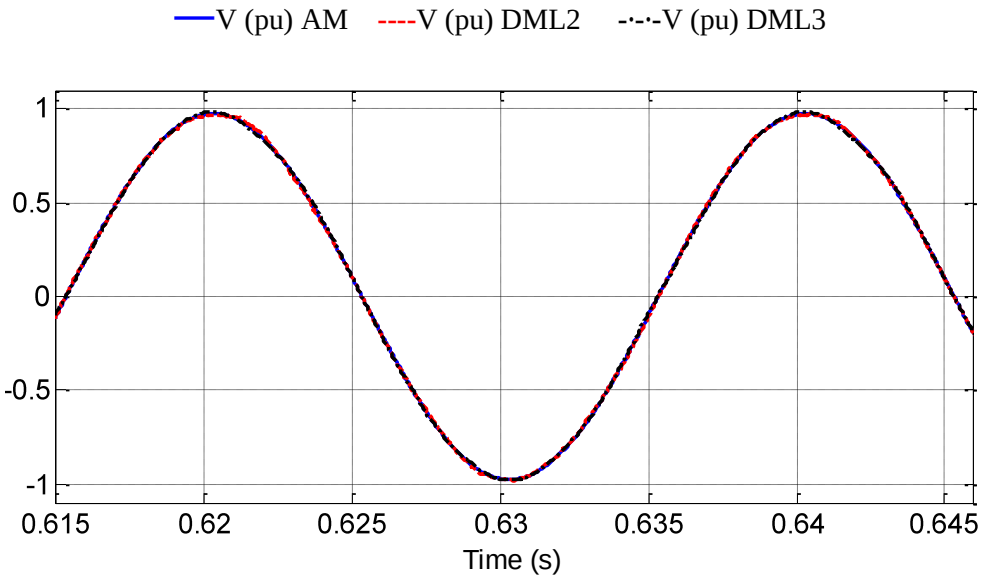


Figure 4.8: VSC voltage waveforms for 2L and 3L converters

4.2.2 Switching Function Models

The concept of switching functions intends to mimic the high frequency pattern of the VSC allowing the representation of high frequency harmonics. This section proposes a new AVM based on switching functions for 2L VSCs (named ASL2) and 3L VSCs (named ASL3). The overall models are similar to the one presented in Figure 4.7, but in this case the controlled ac voltages and dc current contain harmonic distortion generated by the PWM pattern as shown in Figure 4.9 for a 2L VSC (3L VSCs have similar representation).

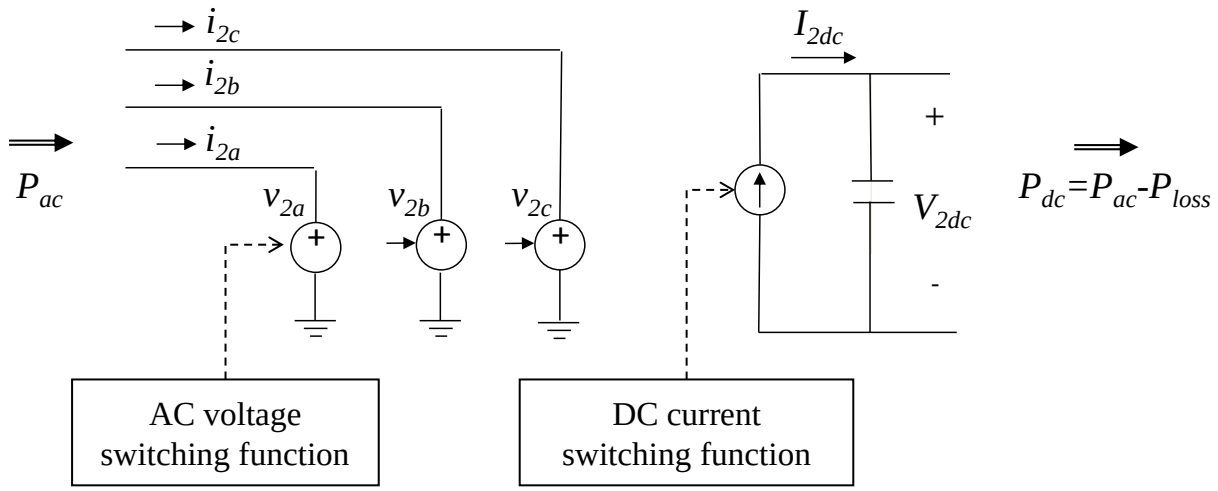


Figure 4.9: Switching function circuit model for a 2L VSCs

4.2.2.1 Switching Functions for Two-level VSCs

The *dq*0-*abc* transformation converts the reference voltage outputs from the inner controller into three voltages references (v_a^*, v_b^*, v_c^*) that are intersected with a triangular carrier waveform to generate the switching pulses. These switching pulses generate voltage waveforms similar to the switching pattern shown in Figure 2.4 and Figure 2.6. Unlike the AM described in section 4.2.1.2, the averaged models based on switching functions represents the high-frequency harmonic content of the converter voltages and currents, thus expanding its range of applications to power quality studies, harmonic analysis and filter design. The switching function concept applied to 2L VSCs was introduced in [7]. The mathematical derivation of the ac converter voltage functions v_{2j} $(j = a,b,c)$ is as follows:

$$v_{2j} = \frac{V_{dc}}{2} SF_{2j} \tag{4.16}$$

$$SF_{2j} = SP_{u_{2j}} - SP_{\ell_{2j}} \tag{4.17}$$

Where SF_{2j} is the switching function of phase j. $SP_{u_{2j}}$ and $SP_{\ell_{2j}}$ are the upper and lower switching pulses (valves $S1$ and $S2$ for phase a in Figure 2.3a) of the 2L converter. SF_{2j} has a pattern similar to the one shown in Figure 2.4, but limited to ± 1. The dc current function for a 2L VSC (I_{2dc}) is calculated as:

$$I_{2dc} = \sum_{j=a,b,c} i_{2j}\, SP_{u_{2j}} \tag{4.18}$$

The accuracy of the AVM based on switching functions is demonstrated in Figure 4.10 for the converter's ac voltage. From the graph, it is observed that the switching function model (ASL2 - solid black line) closely follows the detailed model (DML2 - dashed blue line). The curve AM represents the fundamental voltage (AVM presented in section 4.2.1.2) and is included (plotted) for reference purposes.

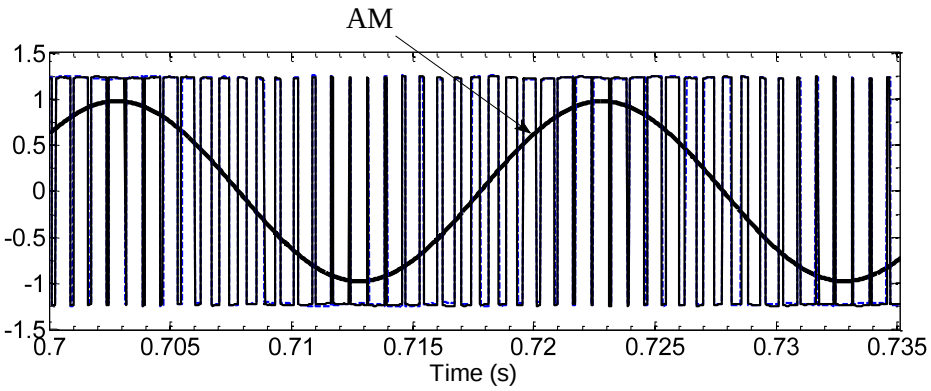


Figure 4.10: 2L converter voltage (pu): DML2 (dashed blue line), ASL2 (solid black line)

4.2.2.2 Switching Functions for Thee-level VSCs

The switching functions for the ac converter's voltage v_{3j} $(j = a,b,c)$ in a 3L VSC are derived as follows:

$$v_{3j} = \frac{V_{dc}}{2} SF_{3j} \tag{4.19}$$

$$SF_{3j} = SP_{u_{3j,1}} SP_{u_{3j,2}} - SP_{\ell_{3j,1}} SP_{\ell_{3j,2}} \tag{4.20}$$

where SF_{3j} is the switching function of phase *j*, $SP_{u_{3j,1}}$ and $SP_{u_{3j,2}}$ are the upper switching pulses for the two upper IGBTs. The lower switching pulses are defined by $SP_{\ell_{3j,1}}$ and $SP_{\ell_{3j,2}}$. SF_{3j} has a pattern similar to the one shown in Figure 2.6, but limited to ± 1. The dc current function for a three-level VSC (I_{3dc}) is given by:

$$I_{3dc} = \sum_{j=a,b,c} i_{3j}\left(SP_{u_{3j,1}} SP_{u_{3j,2}}\right) \tag{4.21}$$

The accuracy of the model is demonstrated in Figure 4.11 for the converter's ac voltage. From the graph, it is observed that the switching function model (ASL3 - solid black line) closely follows the detailed model (DML3 - dashed blue line). The curve AM is included again for reference purposes. The models based on switching functions are shown to be more accurate as they represent the high-frequency switching behavior of the IGBT valves.

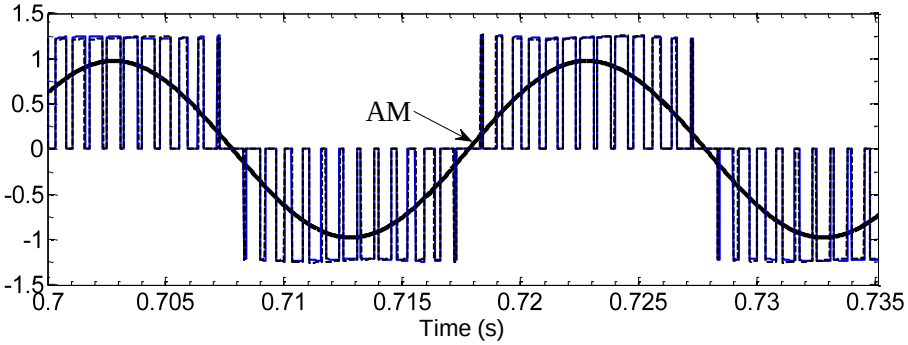


Figure 4.11: 3L converter voltages (pu): DML3 (dashed blue line), ASL3 (solid black line)

4.2.3 AVM for MMCs

Similar to AVMs for 2L and 3L converters, the proposed AVM for MMCs uses voltage- and current-controlled sources. The controlled sources, however, include the harmonic content from the modulation control in the ac voltage waveforms. Similar to the detailed MMC, the reference voltages are the output voltages obtained from the inner vector control where amplitude and phase are controlled independently. Hereafter, the MMC averaged model developed in this section is named as AMM and its equivalent detailed model is named as DMM.

4.2.3.1 AC Side Representation of the AMM

The following equations can be derived from Figure 3.15 for each phase *j* (with $j = a,b,c$) [30]:

$$v_{u_j} = v_{u_j}^{\mathrm{SM}} - L_S \frac{di_{u_j}}{dt} \tag{4.22}$$

$$v_{\ell_j} = v_{\ell_j}^{\mathrm{SM}} - L_S \frac{di_{\ell_j}}{dt} \tag{4.23}$$

$$v_{u_j}^{\mathrm{SM}} = \sum_{k=1}^{N_{arm}} \left(S_{u_{jk}} v_{C_{u_{jk}}} \right) \tag{4.24}$$

$$v_{\ell_j}^{\mathrm{SM}} = \sum_{k=1}^{N_{arm}} \left(S_{\ell_{jk}} v_{C_{\ell_{jk}}} \right) \tag{4.25}$$

$$v_j = -v_{u_j} + \frac{V_{dc}}{2} = v_{\ell_j} - \frac{V_{dc}}{2} \tag{4.26}$$

$$v_{u_j}^{\mathrm{SM}} = -v_j + L_S \frac{di_{u_j}}{dt} + \frac{V_{dc}}{2} \tag{4.27}$$

$$v_{\ell_j}^{\mathrm{SM}} = v_j + L_S \frac{di_{\ell_j}}{dt} + \frac{V_{dc}}{2} \tag{4.28}$$

where v_{u_j} is the total upper arm voltage on each phase *j*, including the voltage of reactor L_S. The voltage $v_{u_j}^{\mathrm{SM}}$ is the total voltage of all upper SMs and is a function of the number of capacitors turned on and the capacitor voltages of each SM ($v_{C_{u_{jk}}}$) as given by equation (4.24). In this equation, the binary function $S_{u_{jk}}$ gives the state of each capacitor. Similar definitions are applicable for the lower arm identified with the subscript ℓ. For arm currents in each phase (see also [40]):

$$i_{u_j} = \frac{i_j}{2} + \frac{I_{dc}}{3} + i_{z_j} \tag{4.29}$$

$$i_{\ell_j} = -\frac{i_j}{2} + \frac{I_{dc}}{3} + i_{z_j} \tag{4.30}$$

where the circulating current (ac second harmonic) is given by:

$$i_{z_j} = \frac{i_{u_j} + i_{\ell_j}}{2} - \frac{I_{dc}}{3} \tag{4.31}$$

and

$$i_{z_a} + i_{z_b} + i_{z_c} = 0 \tag{4.32}$$

Since the AMM assumes perfectly balanced voltages on all capacitors at any time, the second harmonic circulating currents i_{z_j} $(j = a,b,c)$ are zero.

By subtracting (4.27) from (4.28), we obtain:

$$v_j = \frac{L_S}{2}\frac{di_j}{dt} + e_j \tag{4.33}$$

where

$$e_j = \frac{v_{\ell_j}^{\mathrm{SM}} - v_{u_j}^{\mathrm{SM}}}{2} \tag{4.34}$$

Replacing equations (4.29) and (4.34) into (4.27) gives,

$$v_{u_j}^{\mathrm{SM}} = -\left(v_j - \frac{L_S}{2}\frac{di_j}{dt}\right) + \frac{V_{dc}}{2} = -e_j + \frac{V_{dc}}{2} \tag{4.35}$$

By using the same approach for lower arm equations, we obtain:

$$v_{\ell_j}^{\mathrm{SM}} = v_j - \frac{L_S}{2}\frac{di_j}{dt} + \frac{V_{dc}}{2} = e_j + \frac{V_{dc}}{2} \tag{4.36}$$

The ac side representation of the AMM is presented in Figure 4.12 (only phase-*a* control blocks are shown for convenience). The reference voltage $\hat{e}_a$ is generated using the outer and inner controllers described in section 3.1.1. The proposed AMM can support any modulation technique, but only the NLC method is used in this work [30].

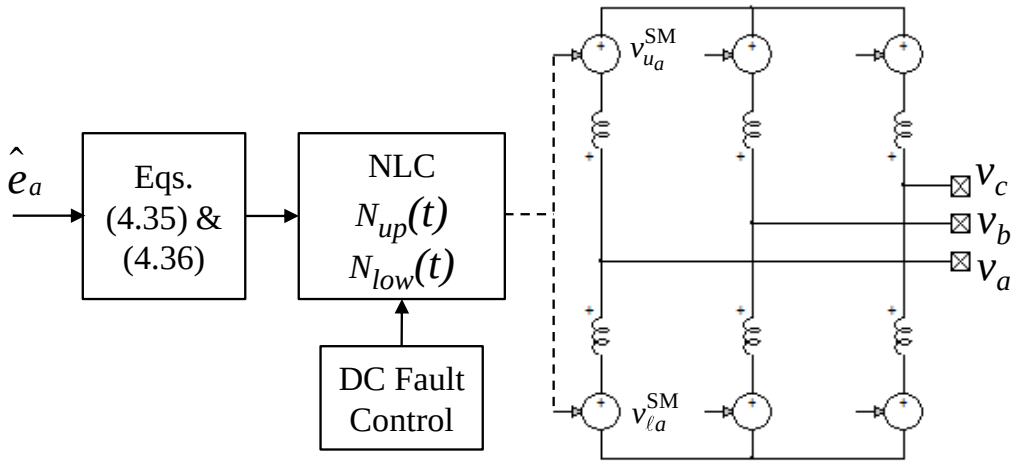


Figure 4.12: AC side representation of the AMM

Figure 4.13 shows the voltage v_a of the AMM for a 21-level MMC using the NLC modulation method. It should be noted that the magnitude and angle of voltage v_a determines the ac current going into (or out of) the MMC.

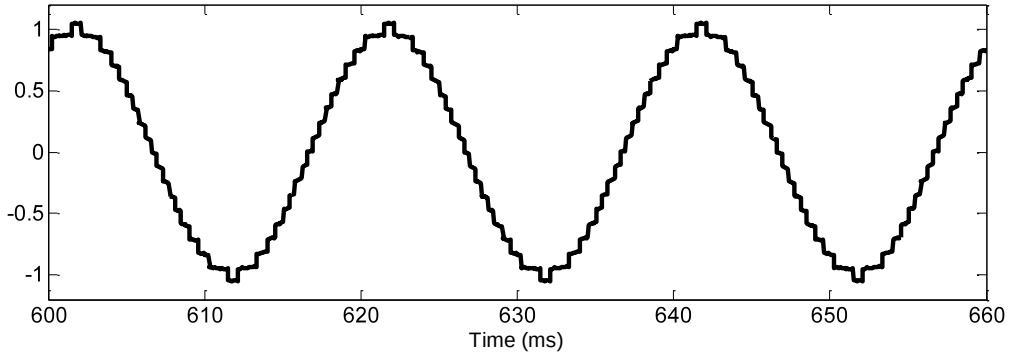


Figure 4.13: AC voltage (pu) for a 21-level AMM

The AMM proposed in this thesis incorporates the harmonic content of the switching evens in the ac waveforms of currents and voltages which significantly improves its accuracy over the previous AM developed for 2L and 3L converters where only the fundamental frequency is represented.

4.2.3.2 DC Side Representation of the AMM

The dc side of the AMM is derived using the principle of power balance (or energy conservation), meaning that the power on the ac side must be equal to the power on the dc side

plus converter losses. The same derivation from equations (4.12) to (4.15) can be applied to MMC AVMs.

$$P_{ac} = \sum_{j=a,b,c} e_j \, i_j = V_{dc} \, I_{dc} + P_{loss} \tag{4.37}$$

$$\frac{P_{ac}}{V_{dc}} = \frac{1}{2} \sum_{j=a,b,c} m_{v\_j} \, i_j = I_{dc} + \frac{P_{loss}}{V_{dc}} \tag{4.38}$$

$$I_{loss} = \frac{P_{loss}}{V_{dc}} = R \frac{I_c^2}{V_{dc}} \tag{4.39}$$

$$I_c = \frac{1}{2} \sum_{j=a,b,c} m_{v\_j} \, i_j \tag{4.40}$$

$$I_{dc} = I_c - I_{loss} \tag{4.41}$$

with,

$$m_{v\_j} = 2 \frac{e_j}{V_{dc}} \tag{4.42}$$

In this case, the reference voltage e_j includes the harmonic content form the NLC modulator. The value of R is selected using the MMC losses from the DMM which are close to 1% for a MMC. The dc side of the AMM is then represented by two current-controlled sources as shown in Figure 4.14.

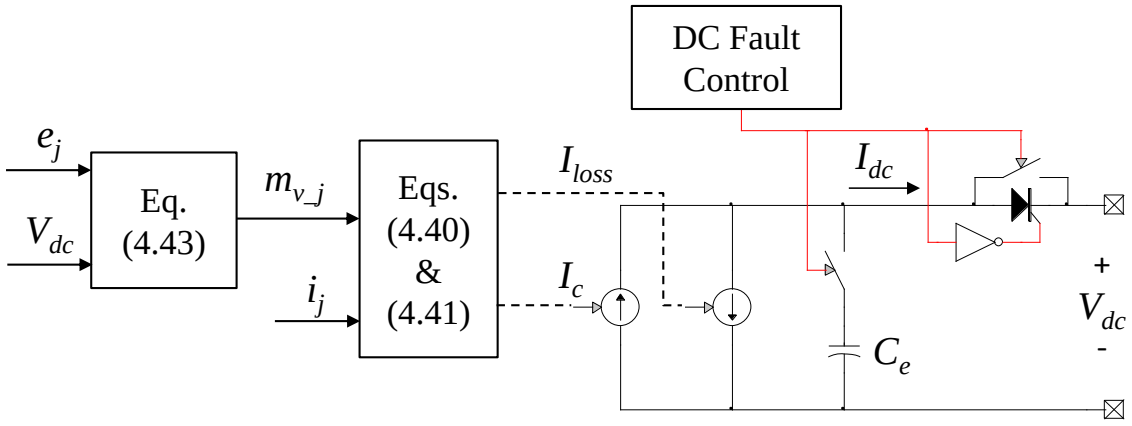


Figure 4.14: DC side representation of the AMM

The capacitor C_e in Figure 4.14 represents the equivalent capacitance of the MMC in the detailed representation. It is derived using the energy conservation principle as follows:

$$E_{\text{MMC}} = 6\frac{1}{2}C\sum_{k=1}^{N_{arm}} v_{C_k}^2 = \frac{1}{2}C_e V_{dc}^2 \tag{4.43}$$

Where E_{MMC} is the total energy stored in the MMC. Assuming all SMs have the same voltage v_C, the equivalent capacitor C_e can be computed from (4.44).

$$C_e = \frac{6C}{N_{arm}} \tag{4.44}$$

It should be noted that the control parameters remain unchanged for the AM in order to ensure fast and accurate dynamic response. During dc faults, all SMs in the detailed MMC are shorted by the thyristor K2 (see Figure 3.16) transforming the MMC into a 6-pulse bridge diode converter. Therefore, the voltage-controlled sources in the AM must be shorted and the dc capacitor C_e disconnected in order to mimic the effect of K2 in the DMM. A series thyristor is added in the dc side representation of the AVM to force the dc current flow direction from ac to dc side.

4.2.4 Simplified Thévenin Equivalent Model for MMCs

A simplified MMC model using Thévenin equivalent circuits for the converter's SMs (named as STM) has been proposed in [17] and is included here for comparison purposes only. In this model, each phase of the MMC is interfaced as a specially designed Thévenin equivalent, thereby greatly reducing the number of nodes. The MMC equations are solved separately in an efficient manner by exploiting its simple topology. Mathematically, the method is exactly equivalent to conducting an EMT-type simulation in the traditional manner, but can be implemented with a reduced computational effort while retaining the accuracy.

Using the trapezoidal integration method [59], the SM's capacitor can be represented as an equivalent voltage source and a resistor as follows:

$$v_c(t) = R_c.i_c(t) + v_{c\_eq}(t - \Delta t) \tag{4.45}$$

where,

$$R_c = \frac{\Delta t}{2C} \tag{4.46}$$

$$V_{c\_eq}(t-\Delta t) = \frac{\Delta t}{2C} i_c(t-\Delta t) + v_c(t-\Delta t) \tag{4.47}$$

The equivalent resistance R_c depends on the SM capacitance C and the simulation time step Δt. The equivalent history voltage $V_{c\_eq}(t-\Delta t)$ is calculated using the capacitor's current and voltage history terms (past time-step).

Additionally, the anti-parallel connection of the IGBT switch and the diodes acts as a bi-directional switch which can be represented by a two-state resistance: ON (small conductive resistive value) and OFF (large open-circuit resistive value).

With the previous capacitor's representation and the resistances representing the bi-directional switches, the equivalent circuit shown in Figure 4.15 can be derived for each SM, where the value of the resistors ($r1$ and $r2$) depends on the switch state (ON/OFF).

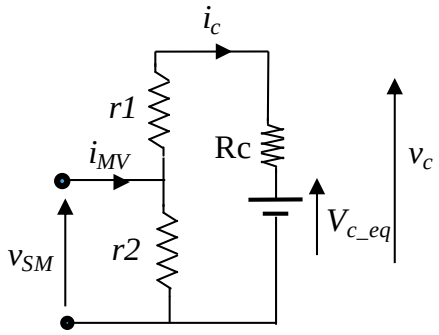


Figure 4.15: Equivalent representation of the SM

Applying Thévenin theorem, the equivalent SM circuit of Figure 4.15 can be further reduced and the voltage v_{SM} calculated as follows:

$$v_{SM}(t) = r_{SM\_eq}.i_{MV}(t) + v_{SM\_eq}(t-\Delta t) \tag{4.48}$$

where i_{MV} is the multi-valve arm current, and

$$r_{SM\_eq}(t) = \frac{r_2(t).\left(r_1(t) + R_c\right)}{r_2(t) + r_1(t) + R_c)} \tag{4.49}$$

$$v_{SM\_eq}(t - \Delta t) = v_{c\_eq}(t - \Delta t).\left(\frac{r_2(t)}{r_2(t) + r_1(t) + R_c}\right) \tag{4.50}$$

The converter's multi-valve arm at each phase can now be modelled as shown in Figure 4.16.

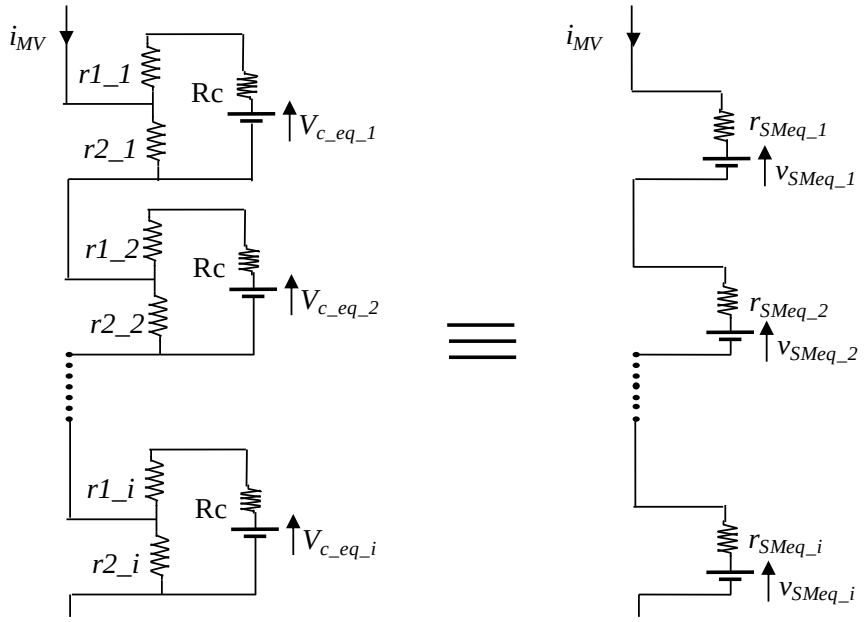


Figure 4.16: Converter's multi-valve arm representation of the MMC

The converter's multi-valve arm circuit can then be reduced and the following equivalent equation derived for the multi-valve arm voltage v_{MV} [17]:

$$v_{MV}(t) = r_{MV\_eq}(t).i_{MV}(t) + v_{MV\_eq}(t - \Delta t) \tag{4.51}$$

where N_{arm} is the number of SMs per multi-valve arm, and

$$r_{MV\_eq}(t) = \left(\sum_{i=1}^{N_{arm}} r_{SM\_eq\_i}(t)\right) \tag{4.52}$$

$$v_{MV\_eq}(t - \Delta t) = \sum_{i=1}^{N_{arm}} v_{SM\_eq\_i}(t - \Delta t) \tag{4.53}$$

4.2.5 Simplified Sub-module Model for MMCs

This model is based on the assumption that the IGBT device and its anti-parallel diodes act as a bi-directional switch represented by a two-state resistance: R_{ON} (small conductive value) and R_{OFF} (large open-circuit value) [60]. Thus, in Figure 4.17 (simplified version of Figure 3.16), R_1 and R_2 depend on gating signals, current direction and capacitor voltage sign. Unlike the Thévenin equivalent model presented in section 4.2.4, the SM capacitor *C* is not reduced using trapezoidal rule, but is explicitly represented. This makes the model less efficient in terms of computing performance as compared to the STM described in the previous section [60]. The equivalent SM circuit is shown in Figure 4.17.

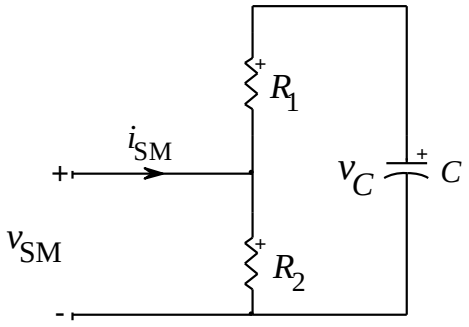
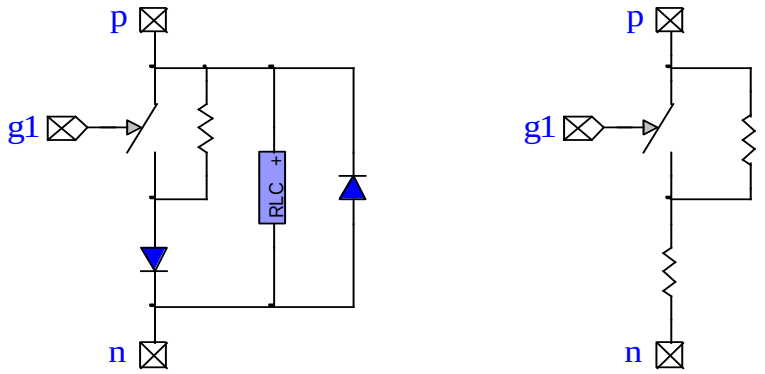


Figure 4.17: SM circuit representation with simplified IGBT model

4.2.6 DM Using a Simplified IGBT Valve

A detailed model including a simplified IGBT valve model can be also used. The model excludes the snubber (RL) circuit of the detailed IGBT valve in Figure 3.1a, and the non-ideal diodes are replaced by small series resistances to represent conduction losses as shown in Figure 4.18b. The model maintains the detailed representation of SM and its accuracy for ac transients, and will improve the computing performance, but not the level of the previous average models. Therefore, this model is not studies further in this work.



(a) (b)

Figure 4.18: IGBT Valve: a) Detailed model with non-linear diodes, b) Simplified model

CHAPTER 5 DYNAMIC PERFORMANCE OF AVERAGED MODELS

Dynamic behavior validation and computing performance comparison of averaged and simplified models are presented in this section. An analysis of advantages and disadvantages (or limitations) is also conducted. Different VSC-HVDC test models are developed for comparison purposes and recommendations on the selection of suitable models for different types of system studies are also provided here. Table 5.1 presents the list of different averaged and detailed VSC models studied in this section.

Table 5.1: Averaged and Detailed VSC Models

Model Name	Model Description
AM	Average model for VSCs based on fundamental frequency
ASL3	Average model for three-level VSCs based on switching functions
DML3	Detailed model for three-level VSCs
AMM	Average model for MMCs
STM	Simplified model for MMCs using Thévenin equivalent circuits
DMM	Detailed model for MMCs

5.1 Dynamic Behavior Validation

Two VSC-based technologies are compared and validated in this section for different transient events using EMTP-RV program. First, conventional 2L and 3L VSC topologies are compared and then, the new MMC-based HVDC technology is studied.

5.1.1 Two- and Three-level AVM VSCs – Test Case 1

A detailed model has been developed in section 3.1 for comparison purposes of 2L and 3L VSC topologies. A point-to-point VSC-HVDC system connecting two asynchronous HV systems is developed here as validation test case (Test Case 1). This case, presented in Figure 5.1, includes two VSC terminals plus a dc link connecting two asynchronous HV systems operating at 500kV (50Hz) and 735kV (60Hz). The nominal power transfer is 1,000MW at a dc voltage of ±400kV. The dc link is represented by a 100 km dc cable using a constant parameter (CP) model. The selected control strategy considers an active/reactive power flow controller on the sending (rectifier VSC-1) side and a dc voltage/reactive power controller on the receiving (inverter VSC-2) side. The two VSCs in the detailed system are modeled using both 2L and 3L NPC converters with a switching frequency ratio of 27. However, as the results are equally valid for both

converter topologies, only the 3L converter model results are presented in this section. The numerical integration time-step used for both models is 10μs.

The 3L VSC AVM compared here corresponds to the phase reference frame AVM developed in section 4.2.1.2 (named as AM). This model is compared against its detailed version (named as DML3) for small and large disturbances. In this section, the solid red line color is used for DML3 waveforms and the solid blue color is used for AM waveforms. All models development and simulations are performed using EMTP-RV (EMTP-RV files "Test Case 1 AM.ecf" and "Test Case 1 DML3.ecf").

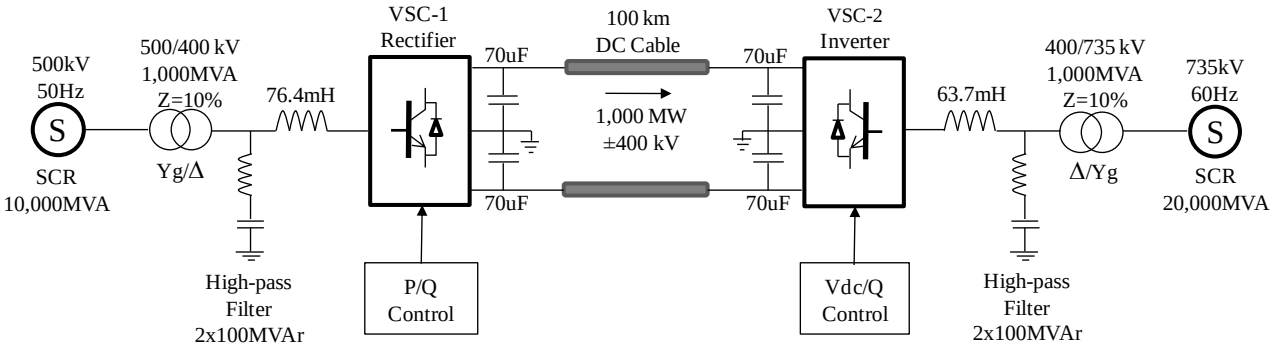


Figure 5.1: Test case 1 - VSC-HVDC transmission system using 3L VSCs

The system data for Test Case 1, including cable configuration and main component parameters, are provided in Appendix B. The overall system configuration and main control blocks of EMTP-RV models are also provided in Appendix B.

5.1.1.1 Active Power Reference Change

A negative variation of 20% is applied to the active power reference set-point on the rectifier converter (VSC-1) after one second of simulation. The active power at each VSC is compared in Figure 5.2 (VSC-1) and Figure 5.3 (VSC-2) for the AM and DML3. The currents and powers are considered positive when entering a VSC. It is observed from these figures that AM accurately follows the behavior of DML3. After 500ms, the system initializes and reaches steady-state for a nominal power flow of 1,000MW (1.0 pu). The active power flow settles down at approximately 400ms after the set-point reduction is applied.

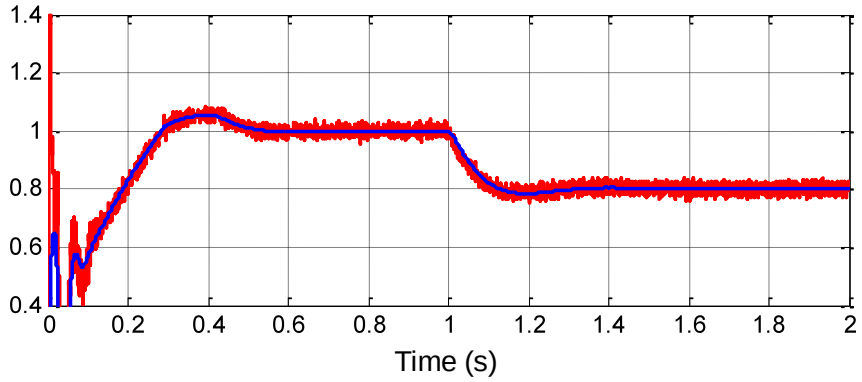


Figure 5.2: Active power (pu) VSC-1 with 20% set-point reduction

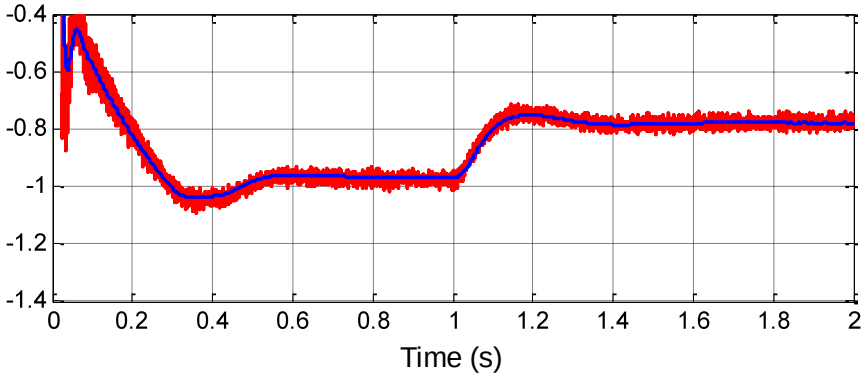


Figure 5.3: Active power (pu) VSC-2 with 20% set-point reduction

5.1.1.2 Reactive Power Reference change

The reactive power reference is initially set to zero at both VSC terminals. After one second of simulation, the reactive power reference is reduced by 10% on VSC-2. Figure 5.4 and Figure 5.5 show that the reactive power can be independently controlled at each VSC terminal. Similar to the active power, AM matches the average behavior of DML3.

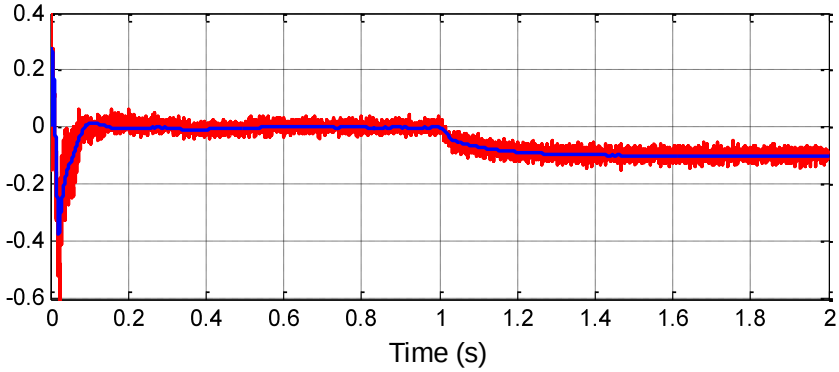


Figure 5.4: Reactive power (pu) VSC-2 with 10% set-point reduction

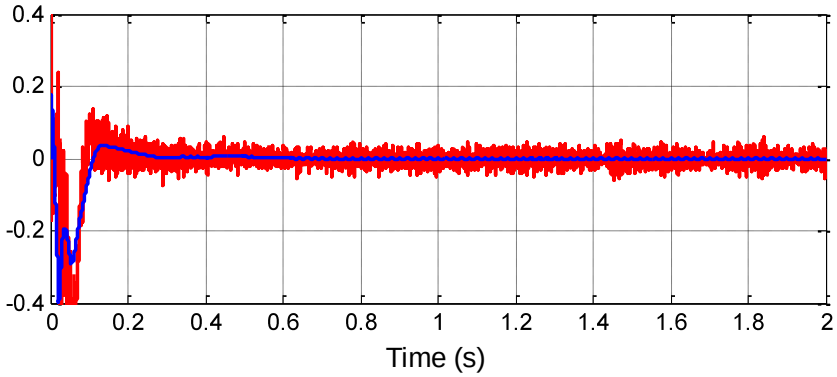


Figure 5.5: Reactive power (pu) VSC-1 with 10% set-point change on VSC-1

5.1.1.3 DC Voltage Reference change

The response to a 10% negative step applied to the dc voltage reference (VSC-2) at t=1s is shown in Figure 5.6. The reference voltage is measured at the low-voltage (delta) side of the converter transformer. The dc voltage control follows the voltage reference for both AM and DML3. Since an independent control is used, the ac voltage on the inverter side is not affected by the dc voltage variation as demonstrated in Figure 5.7.

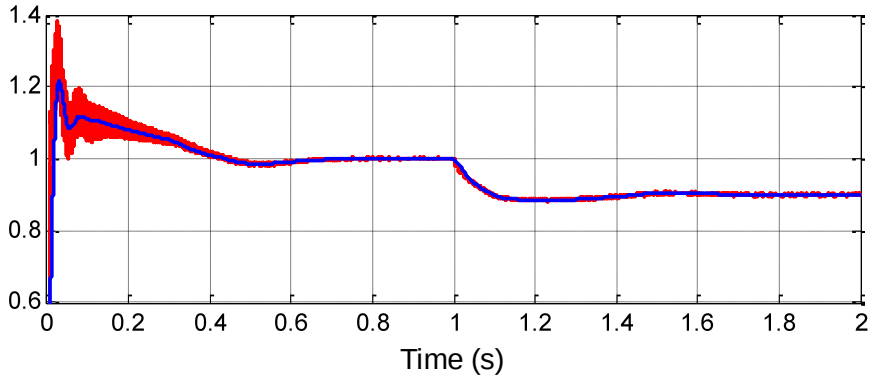


Figure 5.6: DC voltage (pu) Control VSC-2 with 10% set-point change

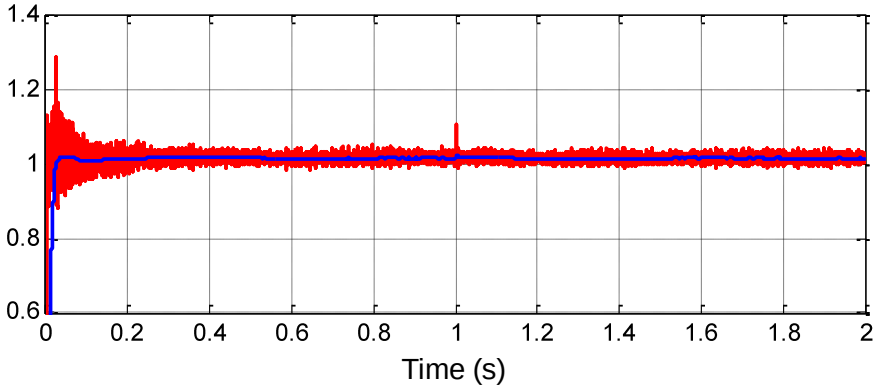


Figure 5.7: AC voltage (pu) VSC-2 with 10% set-point change on VSC-2

5.1.1.4 Three-phase Fault on VSC-2

At $t = 1s$, a three-phase fault is applied for 200ms on the HV side of the 735/400kV converter transformer. The system response including dc voltage, ac voltages and active and reactive powers are presented in Figure 5.8 to Figure 5.12. The dc overvoltage during faults on the ac side is limited to approximately 20% by the dc voltage controller (Figure 5.8). From Figure 5.10, it is observed that the ac voltage on the rectifier side is only slightly affected by the fault on the inverter side of the system, which confirms the assumption of independent voltage control on each VSC terminal. The VSC-HVDC link isolates the two ac systems from any negative impact on the ac voltage due to faults.

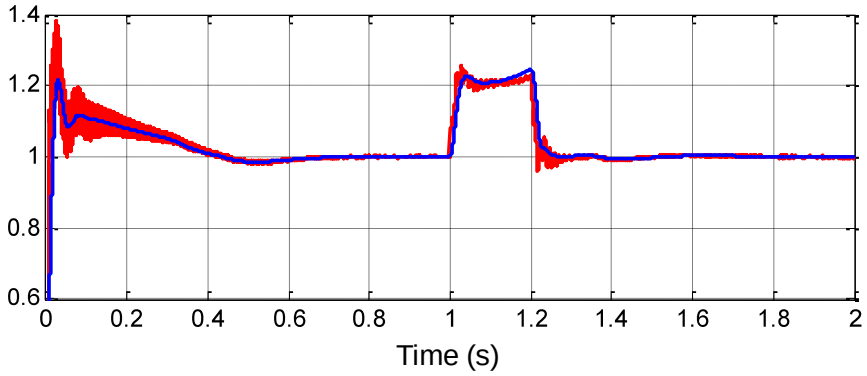


Figure 5.8: DC voltage (pu) VSC-2 - Three-phase fault

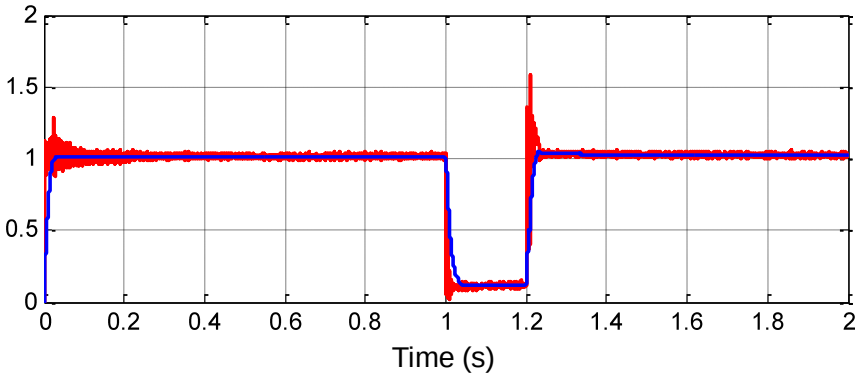


Figure 5.9: AC voltage (pu) VSC-2 - Three-phase fault

The active power is reduced to zero during the fault, and it recovers in 200ms after fault clearing followed by a transient overload of less than 20% (Figure 5.11). This overload is limited by the power control on the rectifier side of the system. The reactive power is invariant during the fault and experiences a short transient right after clearing to slowly recover after approximately one second of simulation (Figure 5.12).

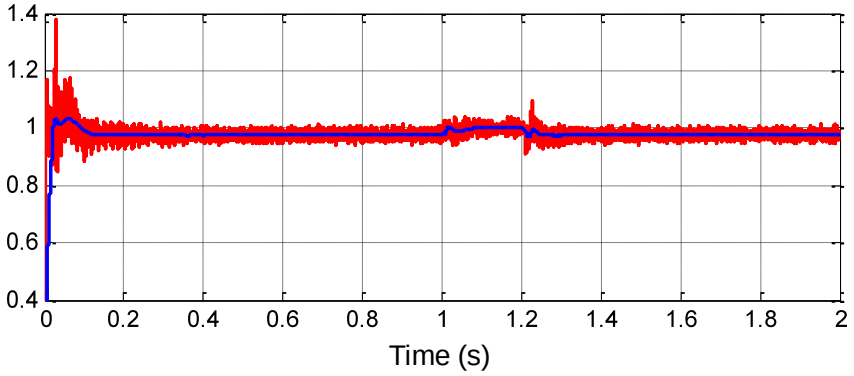


Figure 5.10: AC voltage (pu) VSC-1 - Three-phase fault

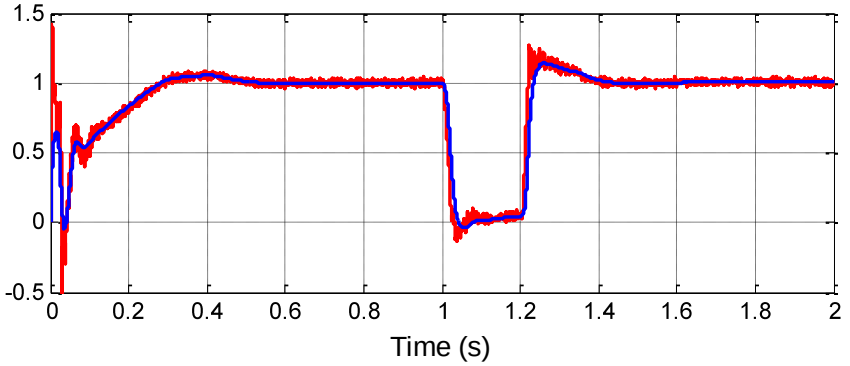


Figure 5.11: Active power (pu) VSC-1 - Three-phase fault

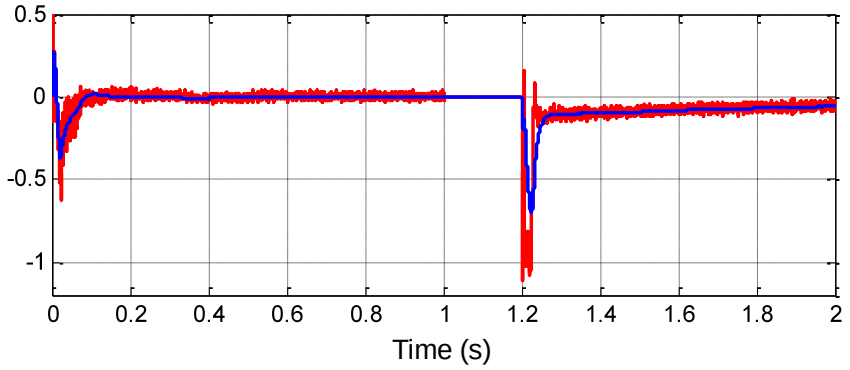


Figure 5.12: Reactive power (pu) VSC-2 - Three-phase fault

5.1.1.5 Reversal of Power Flow

The power reversal test consists of changing the power reference on VSC-1 from full rectifier to full inverter operation. Figure 5.13 shows that the system can suddenly reverse the power flow by reversing the power set-point on VSC-1, without significantly impacting the ac voltage.

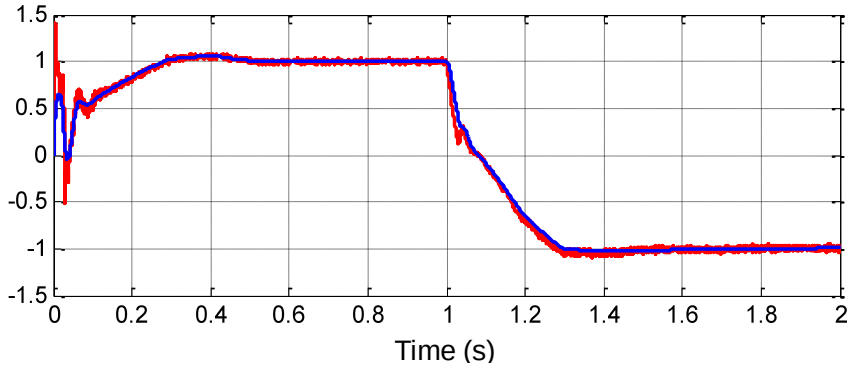


Figure 5.13: Active power (pu) VSC-1 – Power reversal

The controls allow switching the active power from +1.0pu to -1.0pu in only 400ms without significantly altering the ac system voltages (Figure 5.14). It should be noted that the control strategy for each VSC remains unchanged during the power flow inversion.

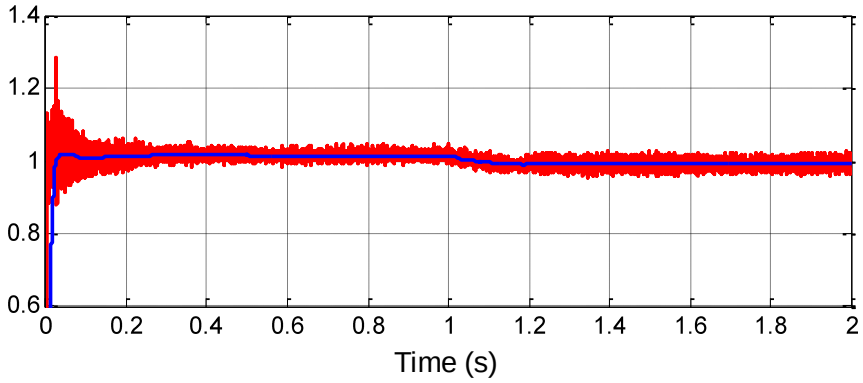


Figure 5.14: AC voltage (pu) VSC-2 – Power reversal

5.1.1.6 DC Fault on VSC-2

DC faults represent a big concern for VSC-HVDC since the anti-parallel diodes conduct as in rectifier bridges to feed the fault. The IGBTs become bypassed and are unable to extinguish the fault current which might damage dc cables and diodes. In order to accurately represent a dc fault, the dc filters must be included in the AM. A dc fault between the positive and negative poles of the inverter VSC-2 (between the cable and the dc capacitors) is simulated at t=1.0s. Although the occurrence likelihood of such a fault is small, it has to be taken into account to specify the cable's maximum current rating. The fault current contribution (in Amps.) going into the cable from VSC-1 and VSC-1 are presented in Figure 5.15 and Figure 5.16, respectively.

The dynamic behavior obtained with the AM (blue) and DML3 (red) models are identical until approximately 3ms after the fault is applied, which is the time where the current is mainly driven by cable and dc capacitors discharge. After this transient period, the dc current accuracy of the AM is lost since this model does not account for the conduction of anti-parallel diodes. The peak current contribution reaches a value of approximately 15 times the nominal current and will vary depending on the size of the dc capacitors and length of the dc cable.

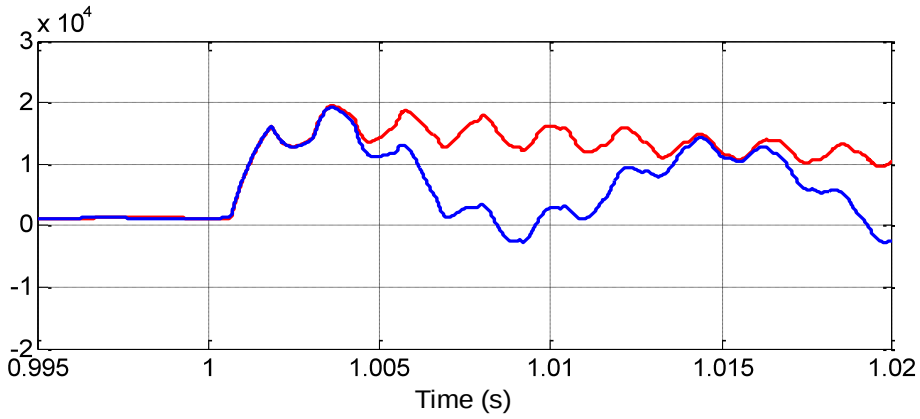


Figure 5.15: DC current contribution (A) from VSC-1 - Pole-to-pole fault

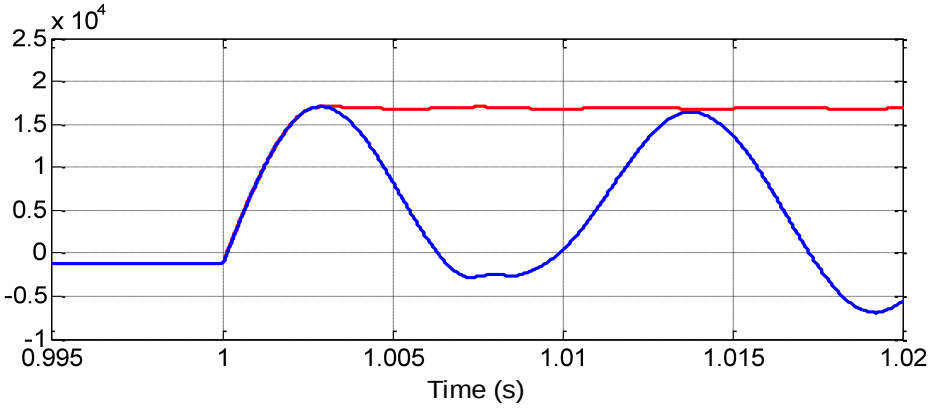


Figure 5.16: DC current contribution (A) from VSC-2 - Pole-to-pole fault

It can be concluded that, even though the AM is accurate to identify maximum stress (peak current) on cables and diodes due to dc faults in some cases, it has limitations to properly represent dc fault conditions during the entire simulation timeframe. Neglecting the effect of anti-parallel diodes makes the accuracy of the model very much dependent on the location and type of faults. Faults close the rectifier converter may present very different results as compared to faults at the inverter terminal. In addition, fault current contribution from the rectifier and inverter sides will be different depending on the fault type and location.

5.1.2 Switching Functions Based Models – Test Case 2

The previous AVM only represents the fundamental component of the ac voltages and currents. Even though the model showed to be accurate, it cannot represent the high frequency harmonics generated by switching pulses in 2L and 3L VSCs. To overcome this limitation, AVMs based on switching pulses were proposed in section 4.2.2. The switching-function-based model for a 3L VSC (named ASL3), is compared here against its detailed representation (named DML3) for a VSC-based MTDC test case (Test Case 2) [28].

The MTDC system, presented in Figure 5.17, includes 5 VSC terminals and is used to integrate 2,000MW of offshore wind generation through a transmission grid of submarine cables modeled with a frequency-dependent (wideband) cable model [35]. The dc voltage is ±320kV and the system is connected to two independent 400kV ac systems (SYS1 and SYS2).

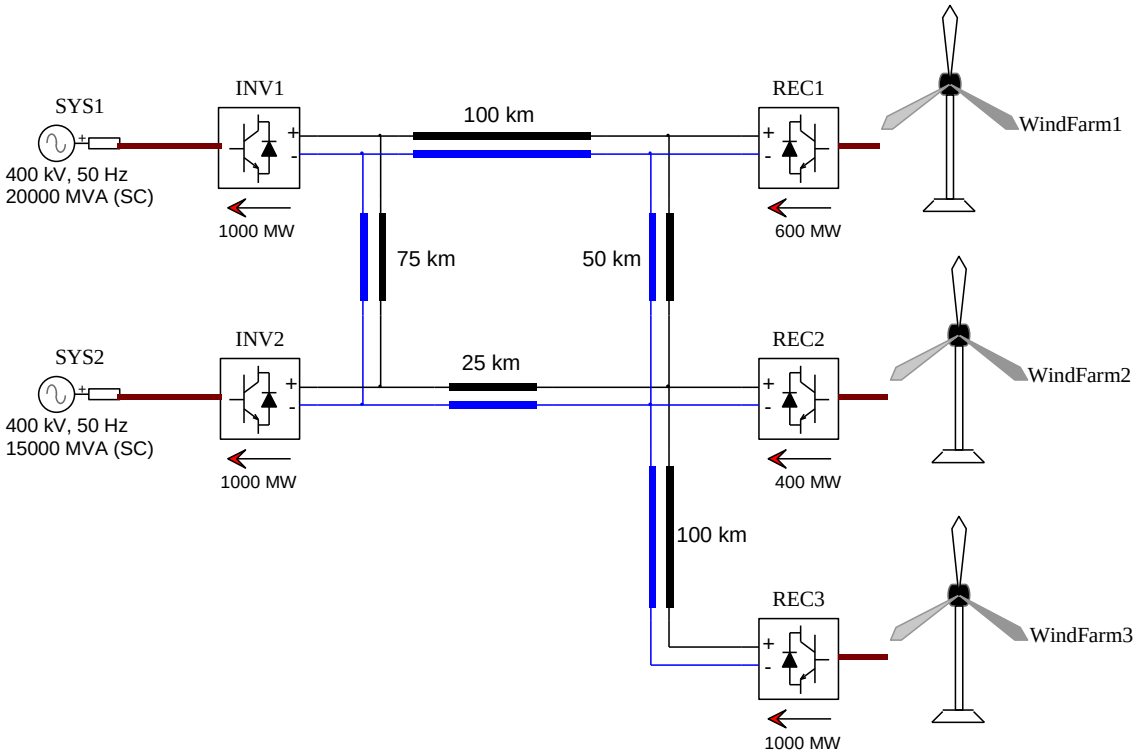


Figure 5.17: Test case 2 – 3L VSC-based MTDC system to integrate off-shore wind generation

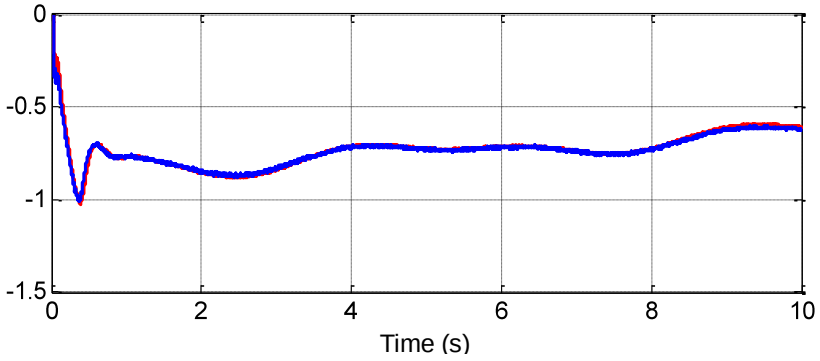
VSC terminals REC1, 2, and 3 as well as INV2 control the power flow and ac voltage (or reactive power), whereas INV1 controls dc and ac voltages. INV2 includes a negative set point for the active power injection which can vary in time as per operational requirements. INV1 will export to SYS1 the active power differential between the three wind farms generation (REC1, 2,

and 3) minus the power injection from INV2 to SYS2. The wind turbines and generators are modeled using Thévenin equivalents networks. The power variability of wind farms is modeled by nonlinear functions that represent variable wind speed generation on the power reference of the rectifier VSCs. All models development and simulations are performed using EMTP-RV (EMTP-RV files "Test Case 2 ASL3.ecf" and "Test Case 2 DML3.ecf"). The numerical integration time-step used is $10\mu s$ for both models.

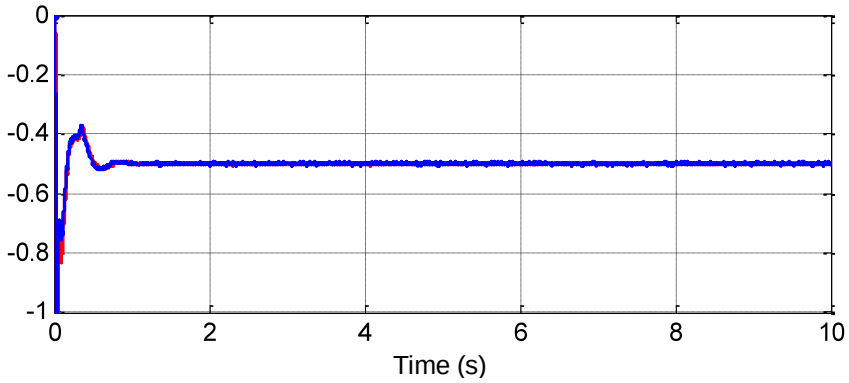
The system data for Test Case 2, including cable configuration and main component parameters, are provided in Appendix C. The overall system configuration and main control blocks of EMTP-RV models are also provided in Appendix C. In the following figures, the ASL3 model (blue line) is compared against its detailed version DML3 (red line) for the 3L VSC topology. Similar results are obtained for the 2L VSC configuration.

5.1.2.1 Wind Variability in Steady-State

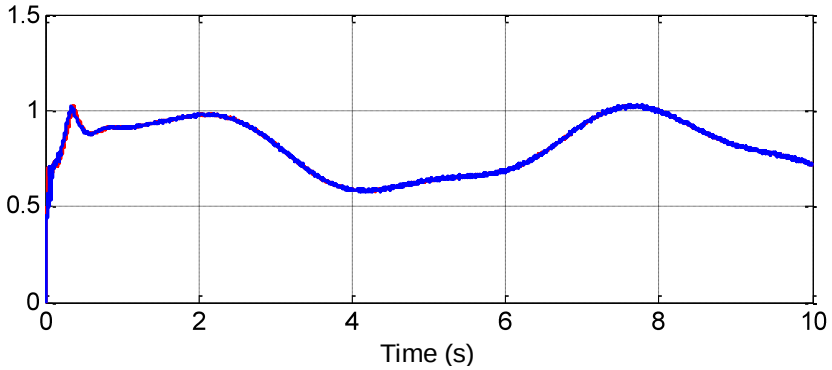
Figure 5.18a-e present the active powers generated by the three wind farms (REC1, 2, and 3) and the powers exported from INV1 and INV2 to SYS1 and SYS2, respectively. The power reference at INV2 is set to -0.5 pu during the 10s simulation interval. It is observed that ASL3 accurately follows the dynamic behavior of the DML3. Figure 5.19 shows that the ac voltage at INV1 is invariant to power injections confirming the independent (power and voltage) control capabilities of the VSC.



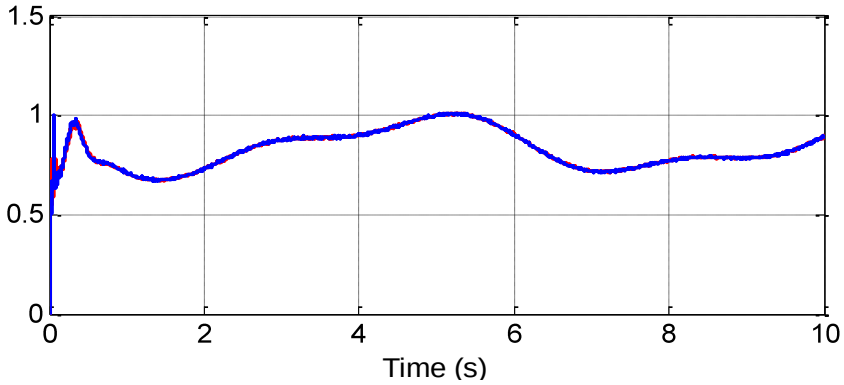
(a) Active power (pu) INV1



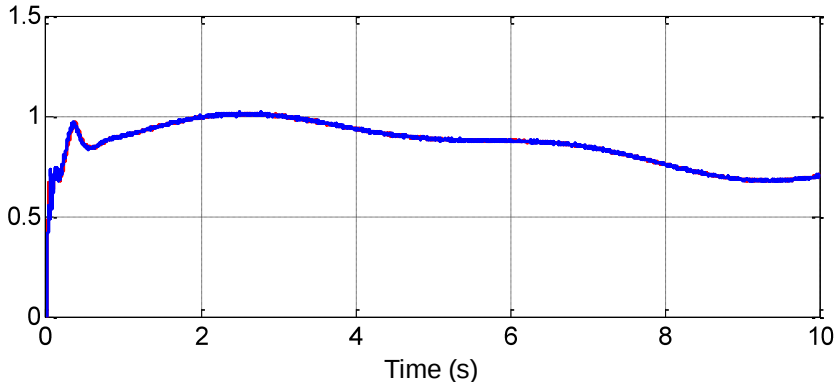
(b) Active power (pu) INV2



(c) Active power (pu) REC1



(d) Active power (pu) REC2



(e) Active power (pu) REC3

Figure 5.18: Active power (pu) entering the VSC terminals – Variable wind generation

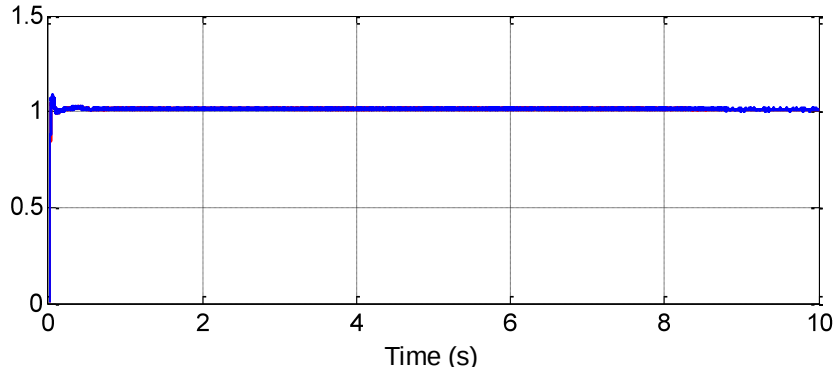
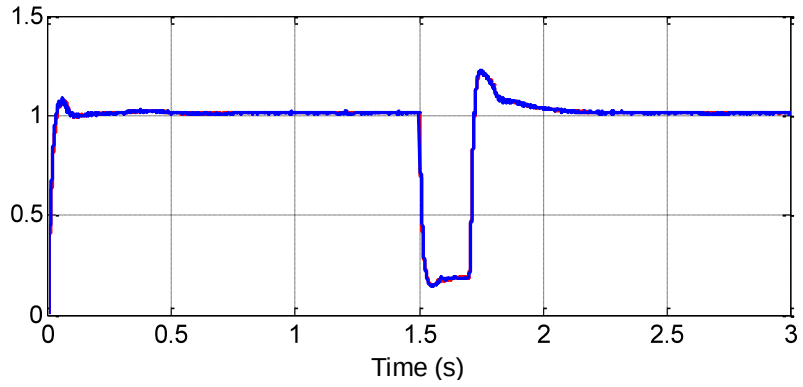


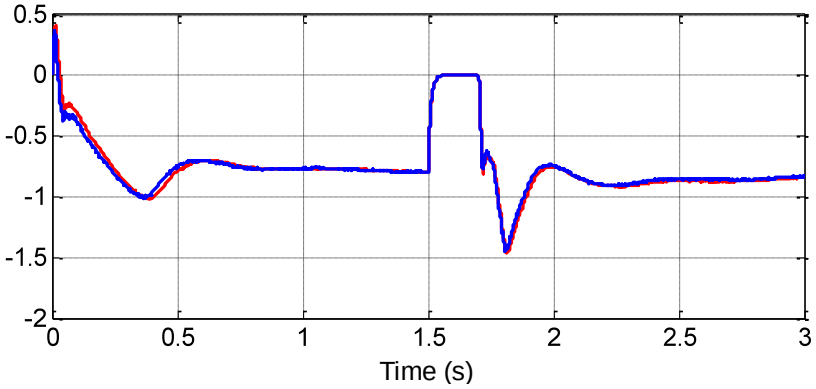
Figure 5.19: AC voltage (pu) at INV1

5.1.2.2 Three-phase Fault on INV1

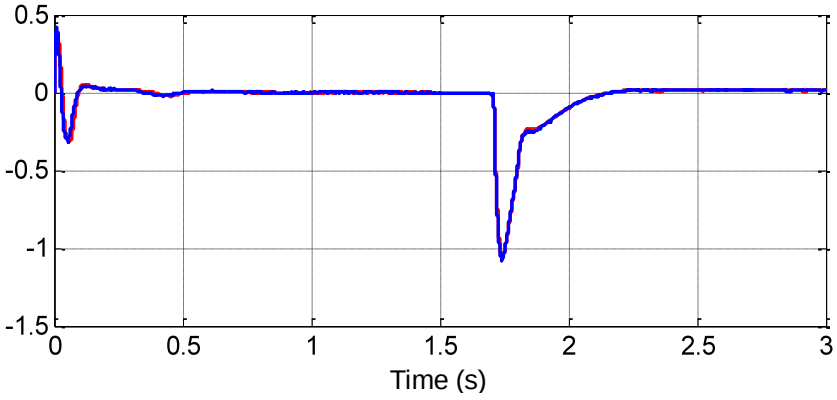
In order to test the transient response of the ASM3, a 200ms three-phase fault is applied on the ac side of INV1 (connection point with SYS1) at 1.5s. Figure 5.20a-d compares the responses for the two models. The ASL3 presents good accuracy and satisfactory results when compared against DML3 and the model could be used, for instance, to efficiently test low-voltage ride-through (LVRT) capabilities of the MTDC system.



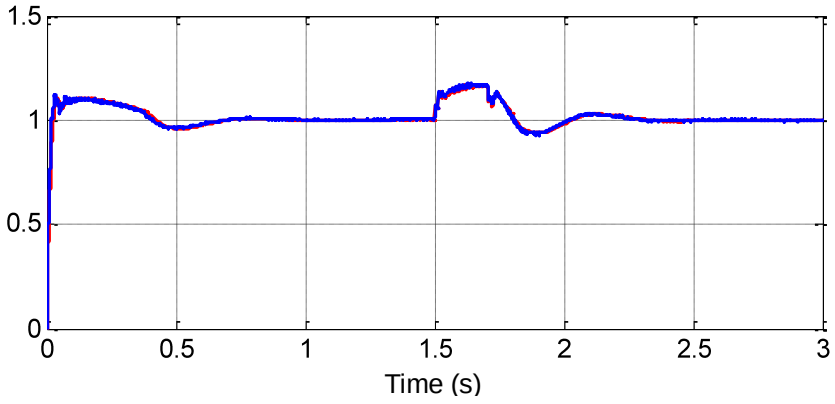
(a) AC voltage (pu) INV1



(b) Active power (pu) INV1



(c) Reactive power (pu) INV1

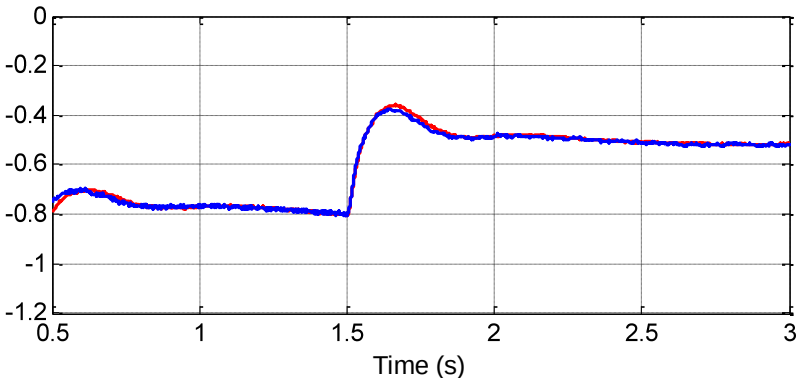


(d) DC voltage (pu) INV1

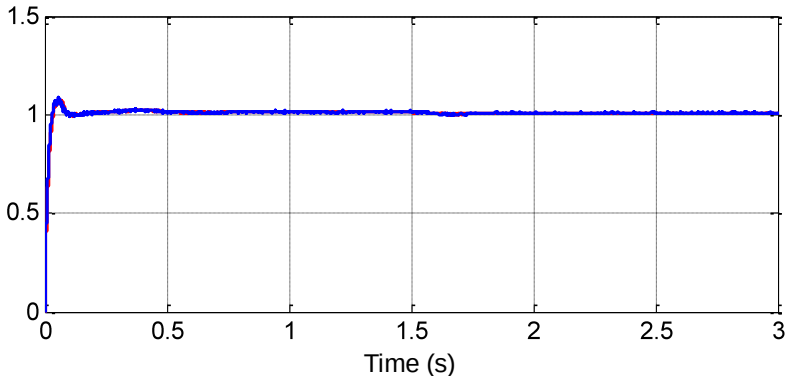
Figure 5.20: Three-phase fault on the HV side of INV1

5.1.2.3 Loss of Generation (Wind Farm 1)

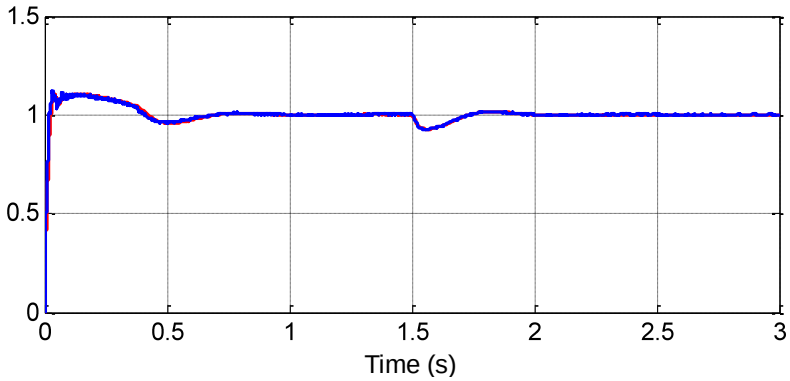
A generation reduction test is performed to compare the dynamic behavior of the ASL3 under such a contingency. The Wind Farm 1 is suddenly disconnected from the system at 1.5s. This outage can be originated from a fault event in the wind farm collector system or from a fault on the VSC terminal. Figure 5.21a-b compare the active power and dc voltage response of the ASL3 against its DML3 version on INV1. The ac voltage remains constant during the loss of generation event as shown in Figure 5.21b. It is demonstrated that ASL3 model accurately replicates the dynamic behavior of the detailed model DML3.



(a) Active power (pu) INV1



(b) AC voltage (pu) INV1



(c) DC voltage (pu) INV1

Figure 5.21: Loss of Wind Farm 1

5.1.2.4 DC Fault

DC faults must be studied for VSC-HVDC systems based on 2L and 3L VSCs since the anti-parallel diodes conduct like in a rectifier bridge to feed the fault. The IGBTs become bypassed and are unable to extinguish the fault current which might damage dc cables and diodes. A permanent dc fault between the positive and negative poles of INV1 is applied at 1.5s. The current flowing from REC1 to the dc fault is presented in Figure 5.22.

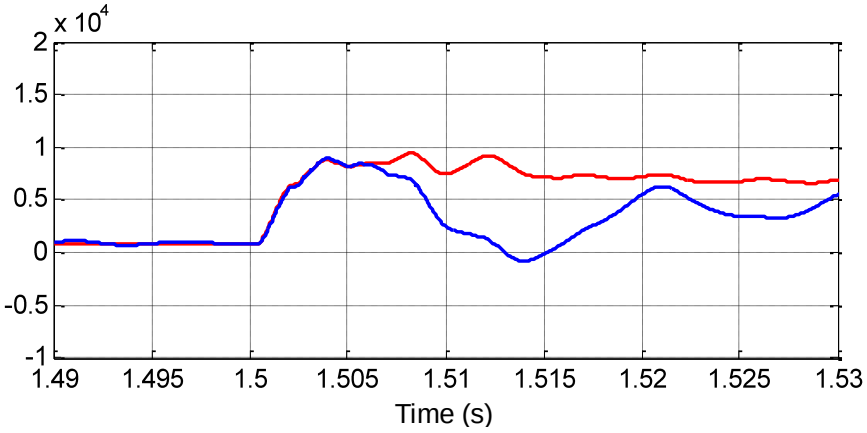


Figure 5.22: Current (A) from REC1 - DC Pole-to-pole fault on REC1

The current during a pole-to-pole fault can reach a very high value (~10pu) in only a few ms if no fault limiters are added on the dc side of the MTDC. The average model ASL3 (red) remains accurate up to 5ms after the fault, but after that time the response diverges as shown in Figure 5.22. Similar to the AM, neglecting the effect of anti-parallel diodes makes the accuracy of the model is very much dependent on the location and type of faults and fault contribution will be different depending on these two factors. Therefore, average models based on current sources and switching functions are not suitable to accurately represent dc-fault transients in MTDC systems and should be used with care.

5.1.2.5 Harmonic Analysis

The harmonic content in 2L and 3L VSCs must be filtered by the use of tuned or damped high-order filters. Filtering will bring harmonic distortion to a value that is below the maximum allowable limits. The Total Harmonic Distortion (THD) of the ac voltage on the secondary side of the three-level VSC is 3.0% and 3.4% for ASL3 and DML3 models, respectively. This result shows a close proximity in terms for harmonic performance for the ASL3, confirming the practicality of the switching function model to conduct harmonic analysis.

5.1.3 MMC-based AVM VSCs – Test Case 3

The dynamic performance of the MMC-based HVDC system shown in Figure 5.23 (Test Case 3) is studied in this section [30]. The system is based on the preliminary design of a 401-level MMC-HVDC system planned to interconnect the 400kV systems of France and Spain by 2013. The interconnection will include two independent HVDC links, each one containing two

MMC terminals with a rated transmission capacity of 1,059MVA each and a dc voltage of ±320kV. Each MMC terminal includes 800 SMs per phase (400 SMs per multi-valve arm) forming the 401 levels. The VSC-HVDC technology based on MMC, has been selected for this project due to dynamic performance and power flow control requirements, and the low ac short-circuit ratio at the point of interconnection of the France-Spain system. It is expected that this project will be the most powerful MMC-HVDC link in operation by 2013.

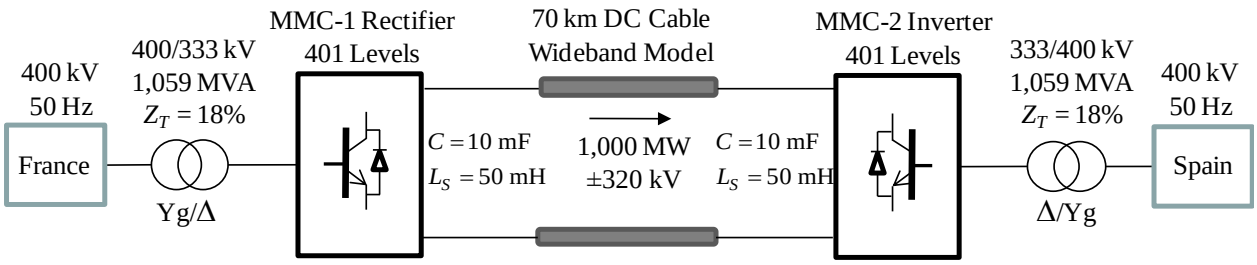


Figure 5.23: Test case 3 – 401-level MMC-HVDC Interconnection between France and Spain

The system data for Test Case 3, including cable configuration and main component parameters, are provided in Appendix D. The overall system configuration and main control blocks of EMTP-RV models are also provided in Appendix D.

The averaged MMC model (AMM) proposed in Section 4.2.3 is compared here against its detailed version (DMM) developed in section 3.2. The selected control strategy considers an active/reactive power flow controller on the sending (rectifier MMC-1) side and a dc voltage/reactive power controller on the receiving (inverter MMC-2) side. The active power flow is set to 1,000MW and the reactive power reference is initially set to zero (unity power factor) at both converters.

All models development and simulations are performed using EMTP-RV (EMTP-RV files “Test Case 3 AMM.ecf” and “Test Case 3 DMM.ecf”). The numerical integration time-step used is $20\mu s$ for both models. The time step is increased for this model thanks to the lower switching frequency of the NLC modulation approach as compared to the PWM method used in 2L and 3L VSCs.

5.1.3.1 AC System Model and Initialization

The ac model includes a dynamic equivalent system of the French and Spanish grids. The total system model comprises 60 transmission lines of 400kV and 23 synchronous generators, 12 of which are modeled in details with their controls. Transmission lines are modeled using the Constant Parameter (CP) model. Such a complete setup allows simulating both electromagnetic and electromechanical (or lower frequency) transients using the same data set and software environment.

Initialization of large networks including HVDC systems is a key issue for EMT-type solvers. To deal with this limitation in a large power system, the MMC-HVDC link is initially connected to ideal voltage sources and then synchronized to the ac grid when the reference power is reached. The voltage magnitudes and angles of the ideal sources are automatically calculated from the load-flow solution of the ac grid. In the load-flow solution the MMCs are modeled as PQ constraints, but PV constraints can be alternatively used depending on the VSC control strategy. The ac grid itself, including synchronous machine controls, is automatically initialized for the time-domain solution. The proposed initialization sequence is presented in Figure 5.24.

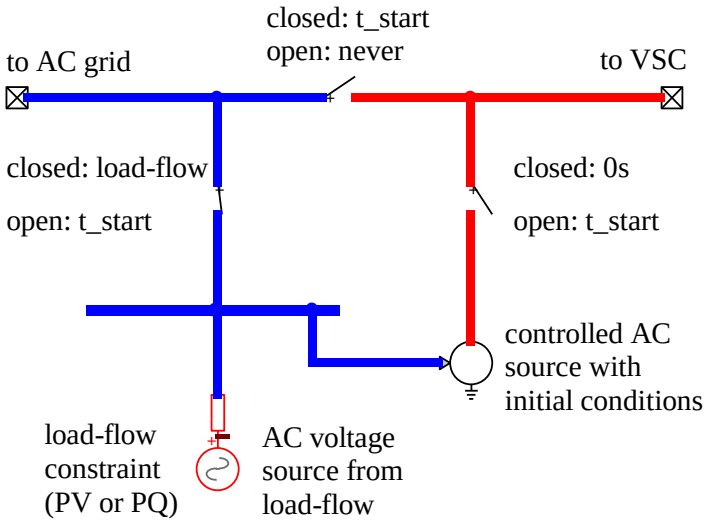


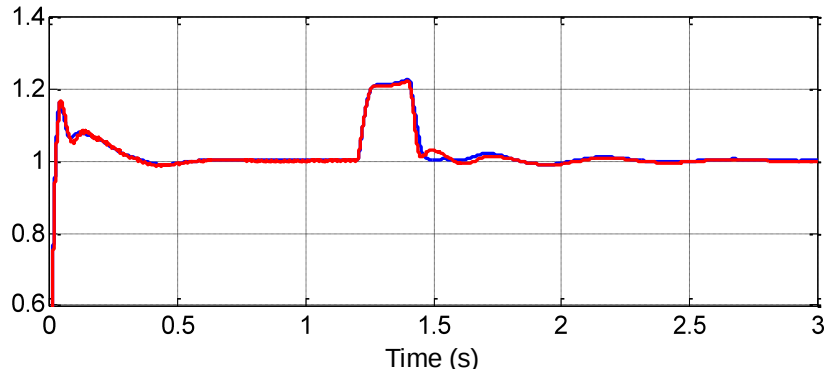
Figure 5.24: AC voltage sources and switching sequence for initialization

5.1.3.2 Three-phase Fault on MMC-2

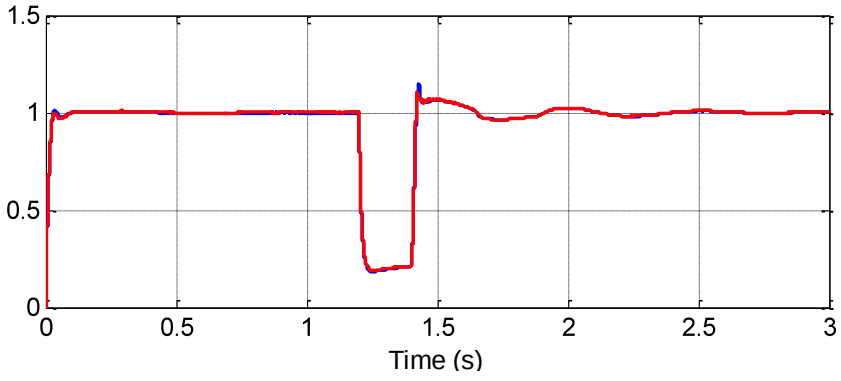
At the simulation time point of $t = 1.2s$, a three-phase fault is applied for 200ms on the HV side of the 400/333kV transformer of MMC-2. The system response including dc and ac

voltages, and active and reactive powers are presented in Figure 5.25a-e. The AMM model is represented by a solid blue line and its detailed version (DMM) by a solid red line.

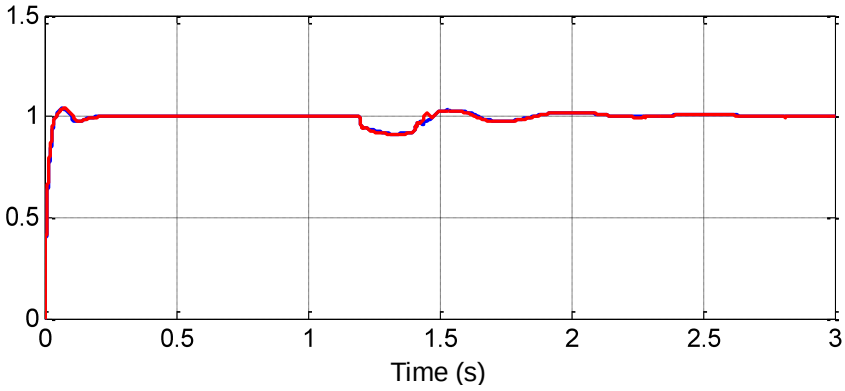
During the fault, the dc overvoltage is limited to 20% by the dc voltage controller. From Figure 5.25c, it is observed that the ac voltage on the rectifier side is only slightly impacted by the fault on the inverter side of the system, which confirms the assumption of independent voltage control of each MMC. The active power is reduced to zero during the fault and it recovers 400ms after a transient overload that is limited by the power control on the rectifier side of the system. It is noticed that the reactive power is invariant during the fault and experiences a short transient right after fault clearing to slowly recover after approximately 600ms. The AMM provides very accurate results for ac and dc dynamics during both steady-state and transient operation.



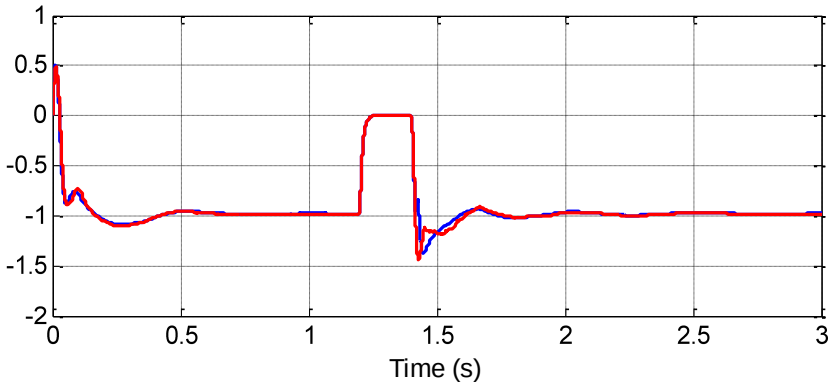
(a) DC voltage (pu) MMC-2



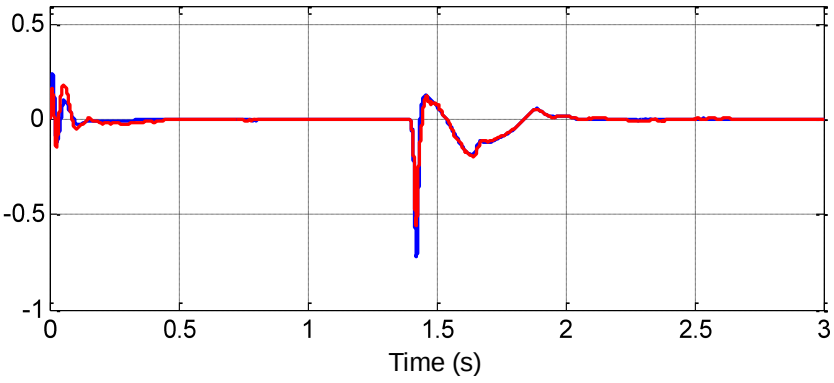
(b) AC Voltage (pu) MMC-2



(c) AC voltage (pu), MMC-1



(d) Active power (pu) MMC-2



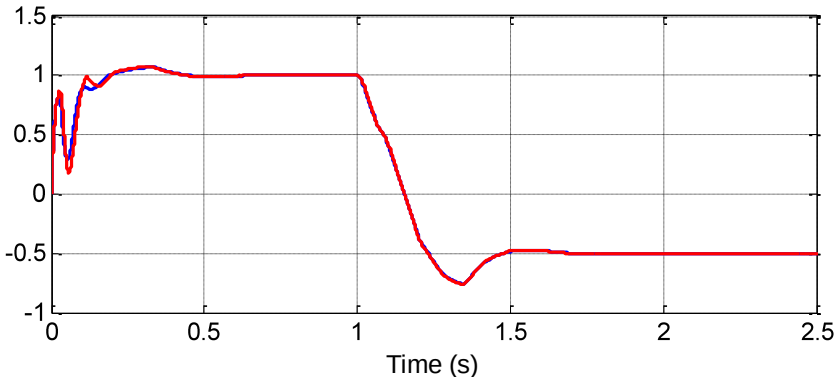
(e) Reactive power (pu) MMC-2

Figure 5.25: Three-phase fault at MMC-2 (Transformer's HV side)

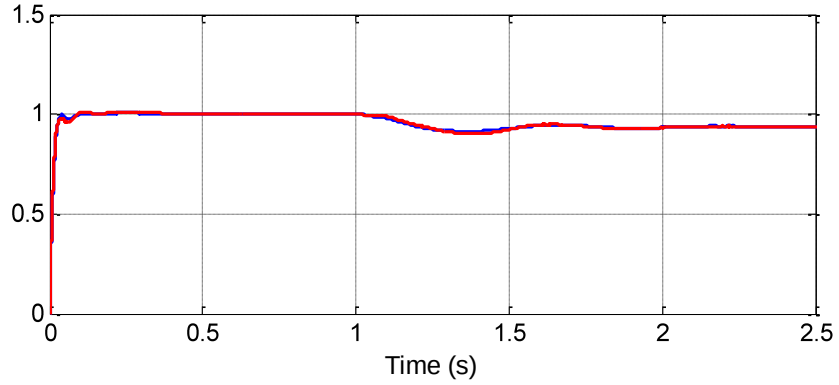
5.1.3.3 Reversal of Active Power Flow

Power reversal is tested by changing the power reference at $t = 1s$ from +1000MW to -500MW using a 200ms ramp reference. Figure 5.26a-b shows that the system can suddenly

reverse the power flow direction by reversing the power set point at MMC-1. The controls allow switching the MMCs from rectifier to inverter operation without significantly altering the ac voltages (Figure 5.26b). The control strategy for each MMC remains unchanged during the power flow reversal, but the ac voltage limiters in the outer controller are relaxed to allow the voltage to vary in a range of ±10%. As the reactive power reference remains unchanged (unity power factor), a voltage drop of 6% is observed at MMC-2 after power reversal. This voltage drop can be compensated by varying the reactive power set point in the outer controller.



(a) Active power (pu) MMC-1



(b) AC voltage (pu) MMC-2

Figure 5.26: Active power reversal

5.1.3.4 DC pole-to-pole fault at MMC-2

DC faults are less frequent in underground cable layouts, but represent an important concern for MMC-HVDC systems. Even though K2 in Figure 3.16a is used to protect and bypass the SM and its diodes, dc faults impose stringent stresses on dc transmission cables. A permanent dc fault between the positive and negative poles of MMC-2 is applied at $t = 1s$. The implemented

protection system assumes that the IBGTs are bypassed by the thyristor K2 $40\mu s$ after the fault is applied. The fault current measured on the dc side of MMC-1 is presented in Figure 5.27. It can be observed that the fault current is limited to 6pu which is a current that can be tolerated by the thyristors and cables for approximately up to 200ms until the ac breaker opens. The AMM (blue line) provides a fair representation of fault currents in cables during dc faults, but contrary to ac side faults, it is less accurate when compared to the DMM (red line).

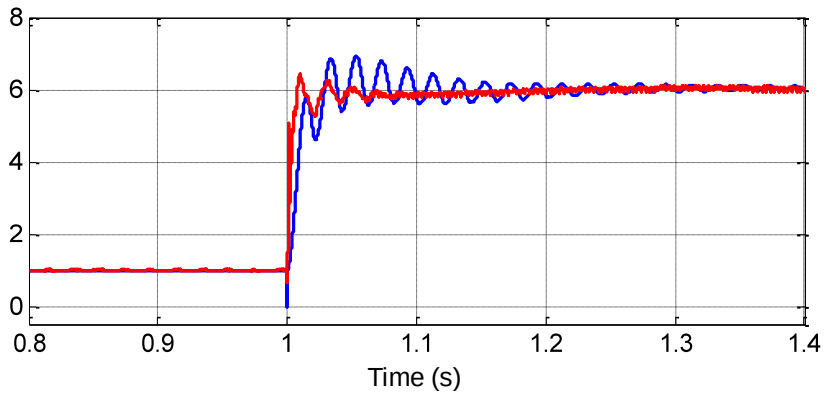
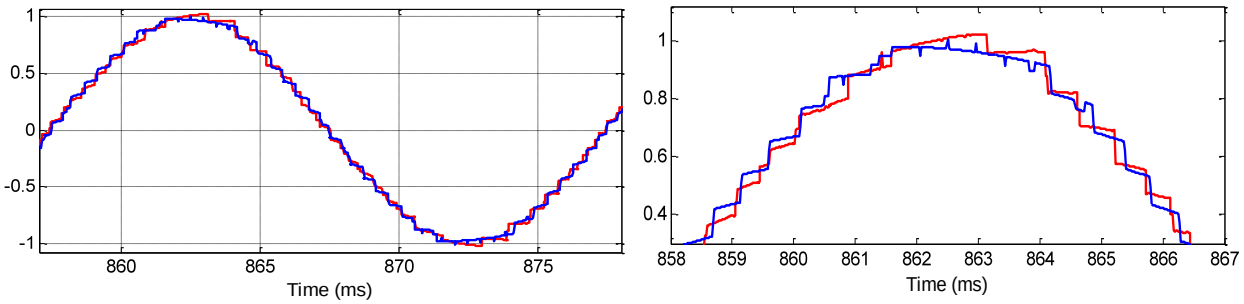


Figure 5.27 DC-fault current contribution (pu) from MMC-1

5.1.3.5 Harmonic Analysis

Figure 5.28a compares the phase-to-neutral voltages on the ac (secondary side transformer) of a 21-level MMC for the DMM (red line) and AMM (blue line) models. Figure 5.28b shows a zoomed representation of the first cycle peak voltages. The Total Harmonic Distortion (THD) of the MMC voltage is 2.63% and 2.72% for the DMM and the AMM models respectively, which corresponds to an error of 3.8%.



(a) One cycle waveforms (b) Zoomed waveforms

Figure 5.28: MMC ac voltage for a 21-level converter (Transformer secondary)

As the number of levels increase in MMCs, the ac voltage waveforms become almost perfectly sinusoidal functions. Figure 5.29 shows the three phase-to-neutral voltages on the ac side of MMC-1 for the DMM. The harmonic content is almost negligible for the 401-level DMM with a Total Harmonic Distortion (THD) value of 0.62% and 0.34% on the secondary (delta) and primary (wye) sides of the converter transformer, respectively. The AMM presents THD values of 0.86% and 0.36% for the secondary and primary transformer voltages, respectively. These values are below the threshold of 1.5% typically specified by international standards for maximum harmonic content and filtering requirements.

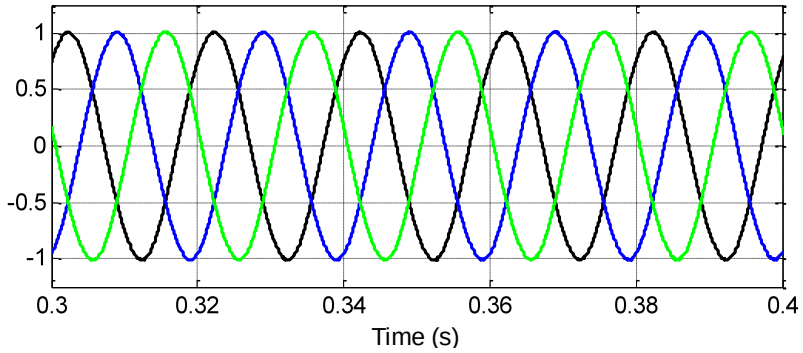


Figure 5.29: AC voltages at MMC-1 (pu), phase-a: black, phase-b: blue, phase-c: green

5.1.4 MMC-based STM VSCs – Test Case 4

The dynamic performance of the MMC-based HVDC system shown in Figure 5.30 (Test Case 4) is used in this section to compare the STM model. The system is a point-to-point synchronous (60Hz) link interconnecting two 340kV systems using 21-level MMC terminals. The Terminals have a rated transmission capacity of 500MVA each and a dc voltage of ±200kV. Each MMC terminal includes 40 SMs per phase (20 SMs per multi-valve arm) forming the 21 levels.

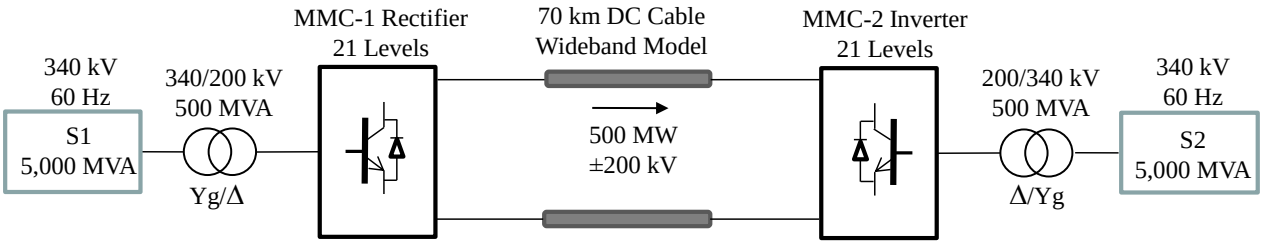


Figure 5.30: Test case 4 – 21-level MMC-HVDC Interconnection

The system data for Test Case 4, including cable configuration and main component parameters, are provided in Appendix E. The overall system configuration and main control blocks of EMTP-RV models are also provided in Appendix E.

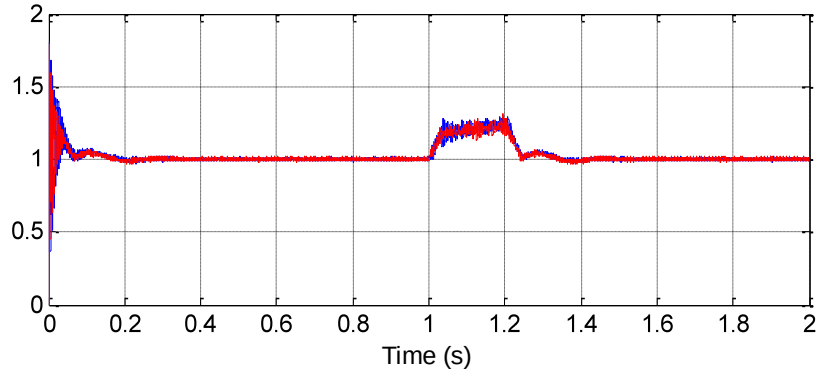
The simplified MMC model (STM) developed in Section 4.2.4 is compared here against its detailed version (DMM) presented in section 3.2. It should be noted that this is not an average model, but a simplified reduction of the converter model that uses Thévenin equivalent circuits. Therefore, its comparison is presented here for reference purposes only.

The selected control strategy considers an active/reactive power flow controller on the sending (rectifier MMC-1) side and a dc voltage/reactive power controller on the receiving (inverter MMC-2) side. The active power flow is set to 500MW and the reactive power reference is initially set to zero (unity power factor) at both converters. All models development and simulations are performed using EMTP-RV (EMTP-RV files "Test Case 4 STM.ecf" and "Test Case 4 DMM.ecf"). The numerical integration time-step used is $20\mu s$ for both models.

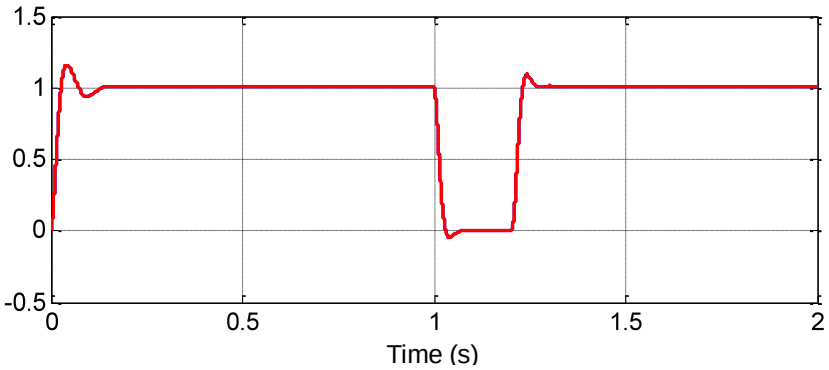
5.1.4.1 Three-phase Fault on MMC-2

At the simulation time point of $t = 1s$, a three-phase fault is applied for 200ms on the HV side of the 340/200kV transformer of MMC-2. The system response including dc and ac voltages and active and reactive powers are presented in Figure 5.31a-e. The STM model is represented by a solid blue line and its detailed version (DMM) by a solid red line.

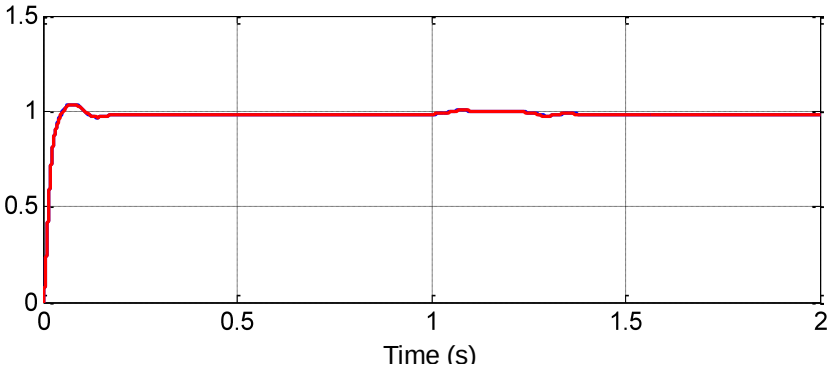
From Figure 5.31c, it is observed that the ac voltage on the rectifier side is only slightly impacted by the fault on the inverter side of the system, which confirms the assumption of independent voltage control on each MMC. The active power is reduced to zero during the fault and it recovers 400ms after a transient overload that is limited by the power control on the rectifier side of the system. It is noticed that the reactive power is invariant during the fault and experiences a short transient right after fault clearing to slowly recover after approximately 800ms. The AMM provides very accurate results for ac and dc dynamics during transient operation.



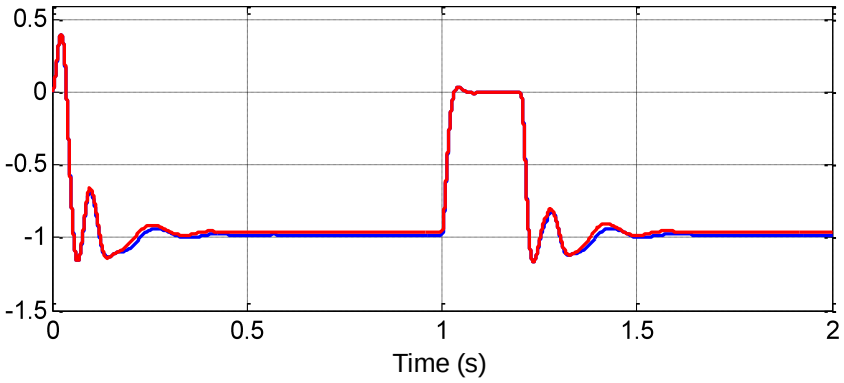
(a) DC voltage (pu) MMC-2



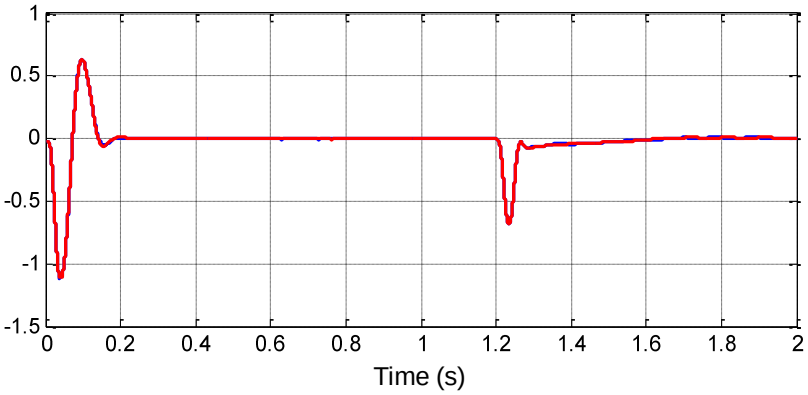
(b) AC voltage (pu) MMC-2



(c) AC voltage (pu), MMC-1



(d) Active power (pu) MMC-2



(e) Reactive power (pu) MMC-2

Figure 5.31: Three-phase fault at MMC-2 (Transformer's HV side)

5.1.4.2 DC pole-to-pole fault at MMC-2

A permanent dc fault between the positive and negative poles of MMC-2 is applied at $t = 1s$. The fault current contribution measured on the dc side of MMC-1 is presented in Figure 5.32. It can be observed that the initial fault current is very high, due to the non-existence of the K2 thyristor in the STM, and it then decays to 6.5pu of the nominal dc current. Different from the AMM response, the STM provides a very good representation of fault currents in cables during dc faults.

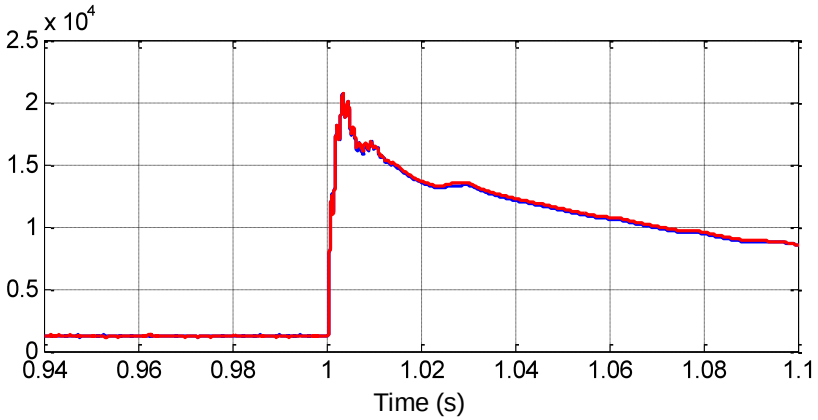


Figure 5.32: DC-fault current contribution (pu) from MMC-1

5.1.4.3 Harmonic Analysis

Figure 5.33 compares the phase-to-neutral voltages on the ac (secondary side transformer) of a MMC for the DMM (red), STM (blue) for the 21-level MMC. The Total Harmonic Distortion (THD) of the MMC voltage is 2.53% and 2.37% for the DMM and the STM models, respectively which corresponds to an error of 6.3%. The STM shows a good accuracy for the harmonics content representation.

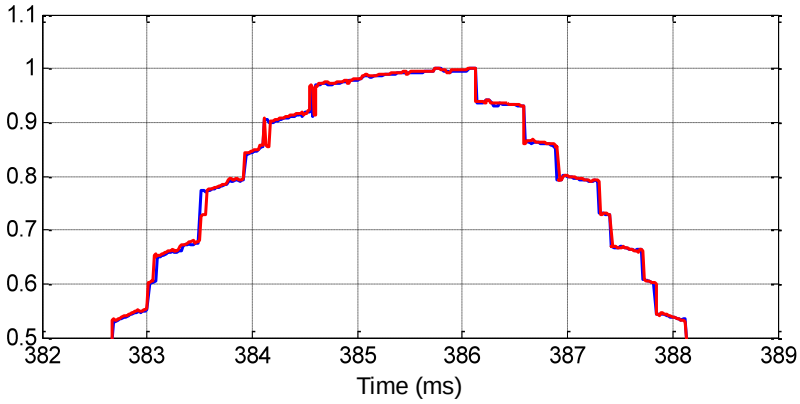


Figure 5.33 MMC ac voltage for a 21-level converter

5.2 Computing Performance Comparison

This section presents a comparison of the computing performance for the different averaged models developed and presented in this work and listed in Table 5.1. The models are compared against their detailed versions. The computing performance tests were done on a computer with a 2.66 GHz Intel Core i7-620M processor and 8 GB of RAM.

5.2.1 AM – Test Case 1

The simulation performance results for the AM and DML3 are presented in Table 5.2. The AM performs significantly better in terms of computer speed. A 3s simulation, using a time-step of 10μs, can be performed five times faster using the AM without compromising the accuracy of the system dynamic response. Since the switching valves are not modeled in the AM, the time-step can be increased up to 50μs without compromising accuracy which improves the speed performance considerably (23 times). By adding proper measurement filters, the time-step may be increased without losing accuracy which brings the simulation time down to less than one second. The same fault case presented in section 5.1.1.4 was simulated for the AM using a much larger time step of 300μs. The waveforms are presented in Figure 5.34.

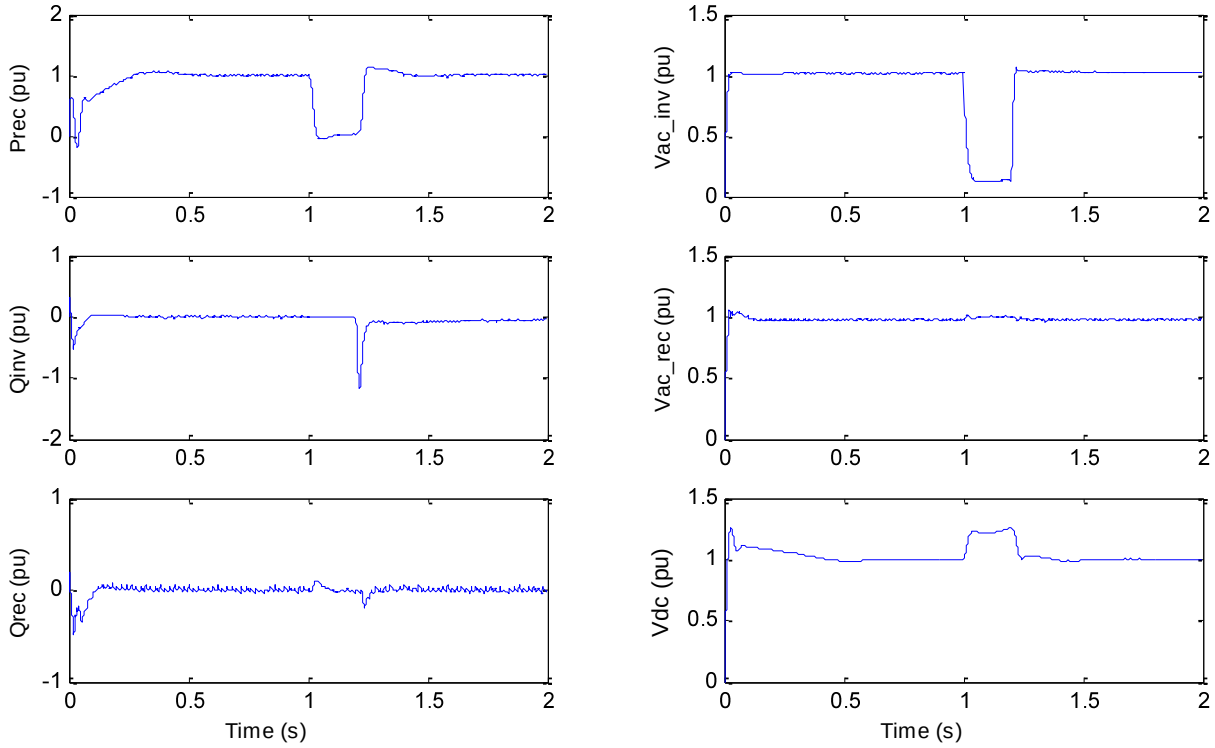


Figure 5.34: AM response to a fault at the inverter side – Simulation time step of 300μs

Table 5.2: AM computing timings for a 3s simulation

Model	Time-step (μs)	Time (s)
DML3	10	158
AM	10	31
	25	13
	50	7

5.2.2 ASL3 – Test Case 2

The simulation performance results for the ASL3 and DML3 are presented in Table 5.3. The ASL3 perform significantly better in terms of computer speed when compared to the DML3. A 3s simulation using a time-step of 10µs can be performed three times faster. In this case, the time step of ASL3 cannot be increased since the switching events are modeled like in the detailed model.

Table 5.3: ASL3 computing timings for a 3s simulation

Model	Time-step (µs)	Time (s)
DML3	10	469.0
ASL3	10	156.3

5.2.3 AMM – Test Case 3

The simulation performance results for the AMM and DMM are presented in Table 5.4. The AMM performs significantly better in terms of computer speed. A simulation of 3s, using a time-step of 20µs, can be performed 367 times faster using the AMM without compromising the accuracy of the system's dynamic response. Both the AMM and DMM remains sufficiently precise when the time-step is increased up to 40µs. Since the switching valves are not modeled in the AMM, a slightly higher time-step can be used without compromising accuracy and therefore allowing further computational speed gains. The AMM approach is much faster than DMM and it can be used in very large systems.

Table 5.4: AMM computing timings for a 3s simulation

Model	Time-step (µs)	Time (s)
DMM	20	25,292
	40	12,929
AMM	20	69
	40	37

5.2.4 STM – Test Case 4

The simulation performance results for the STM and DMM are presented in Table 5.5. The STM performs better in terms of computer speed. A simulation of 3s, using a time-step of 20µs, can be performed between 15 times faster using the DMM without compromising the

accuracy of the system's dynamic response. Both the STM and DMM remains sufficiently precise when the time-step is increased up to 40μs.

Table 5.5: STM Computing timings for a 3s simulation

Model	Time-step (μs)	Time (s)
DMM	20	614
	40	410
STM	20	44
	40	22

5.3 Advantages and Limitations of Averaged Models

Averaged models present advantages and disadvantages and its selection will depend on several factors including complexity, accuracy and computing performance. This section intends to summarize the main advantages and limitation of each modeling approach as well as to provide recommendations on the suitable model to select for different types of power system analysis.

5.3.1 AVM for Two- and Three-level VSCs

Average-value models for conventional 2L and 3L VSCs provide a very accurate response as demonstrated in section 5.1.1. They can accurately represent the fundamental frequency response of VSC-HVDC systems for small and large dynamics. As this model does not represent the IGBT switches, it is not recommended for studying harmonic and/or resonant overvoltages derived from high frequency interactions.

Due to its high computing performance efficiency (up to 20 times), this model can be used to study dynamics and transient on very large networks including hundreds of nodes and/or other power electronics based devices such as wind farm generators and MTDC systems. It is also useful to study dynamic performance for VSC-HVDC control systems and interactions between control systems of different system components.

The AM can provide a fair response during dc faults (first 3ms) and provide a close estimation of the potential peak currents on cable system, but it is not recommended to be used on design-type of studies required to specify the rating of cable systems to be included in technical specifications. The AM can represent and model converter losses, but it cannot be used to study transient events within the converters or faults on the IGBTs valves.

5.3.2 AVM Based on Switching Functions

Average-value models based on switching functions provide a very accurate response as demonstrated in section 5.1.2. They can accurately represent not only fundamental frequency response, but also the harmonic content of the high frequency switching of VSC-HVDC systems for small and large dynamics and for slow and fast transient events. As this model can accurately represent the IGBT switches by means of switching functions, it is recommended for studying harmonic and/or resonant overvoltages derived from high frequency interactions.

Due to its high to moderate computing performance efficiency (5 times), this model can be used to study dynamics and transient on large networks including dozens of nodes and/or other power electronics based devices such as wind farm generators and MTDC systems. It is also useful to study dynamic performance for VSC-HVDC control systems and interactions between control systems of different system components.

Similar to the AM, the ASL3 can provide a fair response during dc faults (first 3ms) and provide a close estimation of the potential peak currents on cable system, but it is not recommended to be used on design-type of studies required to specify the rating of cable systems to be included in technical specifications. The ASL3 can represent and model converter losses, but it cannot be used to study transient events within the converters or faults on the IGBTs valves.

5.3.3 AVM for MMC-based VSCs

Average-value model for MMC-based converters (AMM) provides a very accurate response as demonstrated in section 5.1.3. They can accurately represent the fundamental frequency response of MMC-HVDC systems for small and large slow and fast dynamics. As this model can represent the IGBT switches by means of switching functions, it can be used for studying harmonic and/or resonant overvoltages derived from high frequency interactions.

Due to its impressive computing performance efficiency, this model is strongly recommended to be used for dynamics and transient studies in very large networks including hundreds of nodes and/or other power electronics based devices such as wind farm generators and MTDC systems. It is also useful to study dynamic performance for MMC-HVDC control systems and interactions between control systems of different system components.

The AMM can provide a fair accuracy during dc faults and provide a close estimation of the potential peak currents on cable system, but it is not recommended to be used on design-type of studies required to specify the rating of cable systems included in technical specifications. The AMM can represent and model converter losses, but it cannot be used to study transient events within the converters or faults on the IGBTs valves and sub-modules.

5.3.4 Simplified Models for MMC VSCs

Simplified models based on Thévenin equivalent circuits (STM) provide a very accurate response as demonstrated in section 5.1.4. They can accurately represent the response of MMC-HVDC systems for small and large slow and fast transient and dynamics events. As this model implicitly represents the IGBT switches, it can be used for studying harmonic and/or resonant overvoltages derived from high frequency interactions.

Due to its high computing performance, this model can be used to study dynamics and transient on large networks including dozens of nodes. It is also useful to study dynamic performance for MMC-HVDC control systems and interactions between control systems of different system components.

The STM provide a good response during dc faults and provide a close estimation of the potential peak currents on cable system. It is therefore, recommended to be used on design-type of studies required to specify the rating of cable systems included in technical specifications. The STM can represent and model converter losses, but it cannot be used to study transient events within the converters or faults on the IGBTs valves and sub-modules. These types of studies can only performed using the detailed representation (DML3 or DMM) of MMCs. It should be noted that detailed models can also be used as a benchmark to calibrate and validate other averaged or simplified VSC modes.

5.3.5 Model Suitability for System Studies

Table 5.6 presents a summary of advantages and limitations as well as suitability of each model for different systems studies.

Table 5.6: Summary Table and Comparison of Models

Features	**DM**	**AM**	**ASL**	**AMM**	**STM**
Harmonics	Yes	No	Yes	Yes	Yes
Accuracy	Best	Good	Very good	Very good	Very good
Simulation Time	Very Slow	Very Fast	Fast	Fast	Slow
AC Dynamics	Yes	Yes	Yes	Yes	Yes
AC Fast transients	Yes	No	Yes	Yes	Yes
DC Side transients	Yes	Yes/No	Yes/No	Yes/No	Yes
VSC Internal faults	Yes	No	No	No	No
Resonances	Yes	No	Yes	Yes	Yes
VSC Start-up	Yes	No	No	No	No
Controls interaction	Yes	Yes	Yes	Yes	Yes
Large systems	No	Yes	Yes	Yes	No
Converter Losses	Best	Good	Good	Good	Good

CHAPTER 6 CONCLUSIONS

Detailed representation of VSC-HVDC systems in EMT-type programs includes the modeling of thousands IGBT valves which requires the use of small integration time-steps to accurately represent fast and slow transients. Computational burden introduced by such detailed models significantly reduces the efficiency to study of dynamic and transient events. This limitation is accentuated when complexity and size of the power system is significantly increased as it would be the case of large transmission systems including VSC-based MTDC systems and renewable generation based on power electronic technology. This challenge generates the need to develop more efficient models that provide similar behavior and dynamic response. This challenge was the main motivation of the work presented in this thesis.

The main objective of this research project was to develop averaged models to accurately replicate the steady-state, dynamic and transient behavior of VSC-based HVDC systems in EMT-type programs. In particular, the purpose of this work was to overcome the existing computing limitations associated with the detailed modeling of VSC-based HVDC system integrated into large power grids.

The proposed models represent the average response of switching devices and converter topologies by using averaging techniques, controlled sources and switching functions. This work also contributes to the development of detailed VSC models used to validate the proposed averaged models. The detailed models developed include two- and three-level converter topologies as well as the most recent modular multilevel converter (MMC) topology. Comparison of different converter topologies suitable to VSC-HVDC transmission, including their advantages and limitations, were also discussed.

A control system was implemented based on vector control which permitted independent control of both active and reactive power (and/or voltage) at each VSC terminal. Available modulation techniques were presented and compared in terms of performance and power quality. The modeling approach and developed models were validated against their detailed representation for four test cases including an actual point-to-point VSC-HVDC interconnection between France and Spain and a multi-terminal VSC-based (MTDC) system used to integrate large amounts of offshore wind generation. A detailed description of different VSC-based technologies and control systems were also presented.

The methodology proposed involved the development of detailed models in EMTP-RV that accurately represent the actual behavior of VSC-HVDC technologies. DMs offer several advantages due to its increased accuracy in the modeling of the IGBTs valves. They allow modeling the non-linear behaviour of switching events (through diodes) and representing both switching and conduction losses. DMs also allow simulating specific operation conditions and IGBT states such as blocked states (when both switches in the SMs are OFF) as well as converter's start-up sequence and internal faults. These DMs were used to validate the proposed AVMs for different test cases and transient events.

The validation criteria involved comparing system responses to different disturbances such as ac faults, dc faults, changes on power and voltage order set points, power inversion test and other dynamic and transient tests. The model validation included the comparison of different variables in time-domain and the comparison of the harmonic content of voltages and currents. Different simulation time steps were used as a parameter to compare the computing performance and efficiency of the proposed models.

The main contributions of this thesis can be summarized as follows:

- Provided a comprehensive literature review and description of the available VSC-based HVDC technologies, their main components, applications, and comparison with conventional LCC-based HVDC technologies.
- Presented a comprehensive review and description of the available averaging modeling techniques and methods currently used in power electronic applications as well as explored their applicability to VSC-based HVDC technologies.
- Developed detailed two- and three-level VSC-based HVDC models for different applications in EMTP-RV. These models include converter's IGBT switches, control and protection systems. They were built with the purpose of validating the proposed averaged models.
- Developed detailed MMC-based HVDC models for different applications in EMTP-RV. The models include converter's IGBT switches, control and protection systems. They were built with the purpose of validating the proposed averaged models. These detailed

MMC-based models are the first and only full detailed model benchmark available for validation and for the use in the studies where averaged models may not be suitable.

- Developed efficient averaged models for different VSC-HVDC technologies and applications that accurately represent the dynamic and transient behavior of this technology when integrated into large grids.
- Developed EMTP-RV libraries for averaged and detailed VSC-HVDC models, and also for wind generators models for users of this EMT-type tool.
- Built detailed test cases in EMTP-RV to demonstrate accuracy and performance of the developed models. Test cases included applications such as point-to-point HVDC terminals and MTDC systems to integrate large amounts offshore wind generation.
- Compared and validated existing and new proposed AVMs for different VSC-based HVDC technologies in terms of accuracy and performance efficiency, and assessed their impact on harmonic content and dynamic response behavior.
- Identified advantages and limitations of the developed averaged models and studied their suitability to study different events in power systems.

The present work successfully demonstrated the concept of average-value model applied to VSC-based HVDC systems. The proposed averaged models have been proved to be capable of accurately and efficiently replicate the dynamic performance of the detailed VSC-based HVDC models. All averaged and simplified models presented in this thesis are robust and easily scalable from larger to smaller systems thus expanding the field of applications (such as inverter-based distributed energy resources) and types of studies that can be performed by EMT-type programs. Advantages and disadvantages were presented and recommendations provided for the selection and utilization of the proposed averaged models for different power system studies. It was also concluded that the detailed model remains useful for simulating higher frequency transients, for studying detailed performance conditions inside converters and for calibrating the average models.

The following papers, included in the reference list, were published by the author during the development of this research project:

- *Sections 1 and 4*:

  J. Peralta, S. Dennetiere, and J. Mahseredjian, "Average-value Models for the Simulation of VSC-HVDC Transmission Systems," CIGRE International Symposium, Bologna, Sep. 2011.

- *Section 2:*

  J. Peralta, H. Saad, U. Karaagac, J. Mahseredjian, S. Dennetiere, X. Legrand, "Dynamic Modeling of MMC-based MTDC Systems for the Integration of Offshore Wind Generation," CIGRE Canada Conference, Montreal, QC, Canada, Sep. 2012.

- *Sections 1, 4, and 5:*

  J. Peralta, H. Saad, S. Dennetière, and J. Mahseredjian, "Dynamic Performance of Average-Value Models for Multi-terminal VSC-HVDC Systems," IEEE Power & Energy Society General Meeting, PES'12, San Diego, Jul. 2012.

- *Sections 2, 3, 4, and 5:*

  J. Peralta, H. Saad, S. Dennetière, J. Mahseredjian and S. Nguefeu, "Detailed and Averaged Models for a 401-level MMC-HVDC system", IEEE Trans. on Power Delivery, vol. 27, no. 3, pp. 1501-1508, Jul. 2012.

- *Section 4:*

  H. Saad, J. Peralta, S. Dennetiere, J. Mahseredjian, J. Jatskevich, J. A. Martinez, A. Davoudi, M. Saeedifard, V. Sood, X. Wang, J. Cano, and A. Mehrizi-Sani, "Dynamic Averaged and Simplified Models for MMC-Based HVDC Transmission Systems," IEEE Trans. on Power Delivery, vol. 28, no. 3, pp. 1723–1730, Jul. 2013.

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APPENDIX A CORRESPONDENCE LIST OF FIGURES AND EMTP-RV FILES

Figure No	**Description**	**EMTP-RV File**
2.4	Converter Voltage (pu) (blue: 50 Hz component, black: converter output)	Test Case 1 DML2.ecf
2.6	Converter Voltage (pu) (blue: 50Hz component, black: converter output)	Test Case 1 DML3.ecf
2.11	AC voltage (pu) for a 21-level MMC	Test Case 4 DMM.ecf
3.13	Voltage references and PWM triangular carrier waveforms for a 2L VSC	Test Case 1 DML2.ecf
3.14	Voltage references and PWM triangular carrier waveforms for a 3L VSC	Test Case 1 DML3.ecf
3.19	CCSC for a 401-Level MMC, CCSC is removed at t=1s	Test Case 3 DMM.ecf
4.3	Voltage and Current waveforms for a 2L VSC	Test Case 1 DML2.ecf
4.4	Voltage and Current waveforms for a 3L VSC	Test Case 1 DML3.ecf
4.5	Voltage waveform for 3L VSC during steady-state operation	Test Case 1 DML3.ecf
4.8	VSC voltage waveforms for 2L and 3L converters	Test Case 1 AM.ecf Test Case 1 DML2.ecf Test Case 1 DML3.ecf
4.10	2L Converter voltage (pu): DML2 (dashed blue line), ASL2 (solid black line)	Test Case 1 ASL2.ecf Test Case 1 DML2.ecf
4.11	3L Converter voltages (pu): DML3 (dashed blue line), ASL3 (solid black line)	Test Case 1 ASL3.ecf Test Case 1 DML3.ecf
4.13	AC voltage (pu) for a 21-level AMM	Test Case 4 AMM.ecf
5.2	Active power (pu) VSC-1 with 20% set-point reduction	Test Case 1 AM.ecf Test Case 1 DML3.ecf
5.3	Active power (pu) VSC-2 with 20% set-point	Test Case 1 AM.ecf

Figure No	**Description**	**EMTP-RV File**
	reduction	Test Case 1 DML3.ecf
5.4	Reactive Power (pu) VSC-2 with 10% set-point reduction	Test Case 1 AM.ecf Test Case 1 DML3.ecf
5.5	Reactive Power (pu) VSC-1 with 10% set-point change on VSC-1	Test Case 1 AM.ecf Test Case 1 DML3.ecf
5.6	DC Voltage (pu) Control VSC-2 with 10% set-point change	Test Case 1 AM.ecf Test Case 1 DML3.ecf
5.7	AC Voltage (pu) VSC-2 with 10% set-point change on VSC-2	Test Case 1 AM.ecf Test Case 1 DML3.ecf
5.8	DC Voltage (pu) VSC-2 - Three-phase fault	Test Case 1 AM.ecf Test Case 1 DML3.ecf
5.9	AC Voltage (pu) VSC-2 - Three-phase fault	Test Case 1 AM.ecf Test Case 1 DML3.ecf
5.10	AC Voltage (pu) VSC-1 - Three-phase fault	Test Case 1 AM.ecf Test Case 1 DML3.ecf
5.11	Active Power (pu) VSC-1 - Three-phase fault	Test Case 1 AM.ecf Test Case 1 DML3.ecf
5.12	Reactive Power (pu) VSC-2 - Three-phase fault	Test Case 1 AM.ecf Test Case 1 DML3.ecf
5.13	Active Power (pu) VSC-1 – Power reversal	Test Case 1 AM.ecf Test Case 1 DML3.ecf
5.14	AC Voltage (pu) VSC-2 – Power reversal	Test Case 1 AM.ecf Test Case 1 DML3.ecf
5.15	DC Current contribution (A) from VSC-1 - Pole-to-pole fault	Test Case 1 AM.ecf Test Case 1 DML3.ecf
5.16	DC Current contribution (A) from VSC-2 - Pole-to-pole fault	Test Case 1 AM.ecf Test Case 1 DML3.ecf
5.18	Active Power (pu) entering the VSC terminals – Variable wind generation	Test Case 2 ASL3.ecf Test Case 2 DML3.ecf

Figure No	**Description**	**EMTP-RV File**
5.19	AC Voltage (pu) at INV1	Test Case 2 ASL3.ecf Test Case 2 DML3.ecf
5.20	Three-phase fault on the HV side of INV1	Test Case 2 ASL3.ecf Test Case 2 DML3.ecf
5.21	Loss of Wind Farm 1	Test Case 2 ASL3.ecf Test Case 2 DML3.ecf
5.22	Current (A) from REC1 - DC Pole-to-pole fault on REC1	Test Case 2 ASL3.ecf Test Case 2 DML3.ecf
5.25	Three-phase fault at MMC-2 (Transformer's HV side)	Test Case 3 AMM.ecf Test Case 3 DMM.ecf
5.26	Active power reversal	Test Case 3 AMM.ecf Test Case 3 DMM.ecf
5.27	DC-fault current contribution (pu) from MMC-1	Test Case 3 AMM.ecf Test Case 3 DMM.ecf
5.28	MMC ac voltage for a 21-level converter (Transformer secondary)	Test Case 3 AMM.ecf Test Case 3 DMM.ecf
5.29	AC voltages at MMC-1 (pu), phase-a: black, phase-b: blue, phase-c: green	Test Case 3 DMM.ecf
5.31	Three-phase fault at MMC-2 (Transformer's HV side)	Test Case 4 STM.ecf Test Case 4 DMM.ecf
5.32	DC-fault current contribution (pu) from MMC-1	Test Case 4 STM.ecf Test Case 4 DMM.ecf
5.33	MMC ac voltage for a 21-level converter	Test Case 4 STM.ecf Test Case 4 DMM.ecf

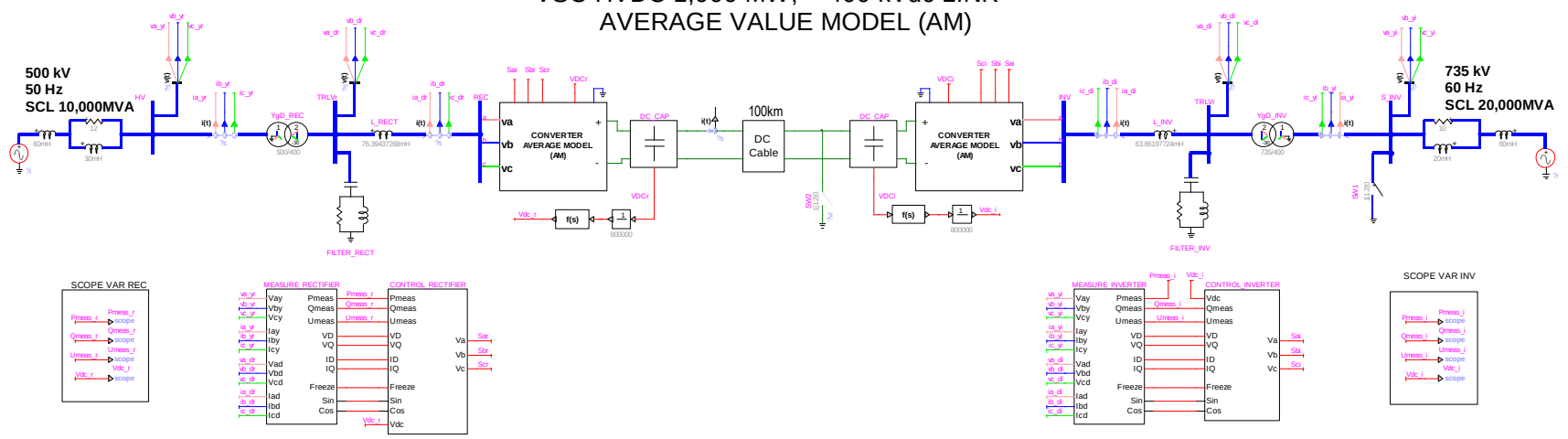
APPENDIX B TEST CASE 1 DATA AND EMTP-RV MODELS DESIGN

i. System Data

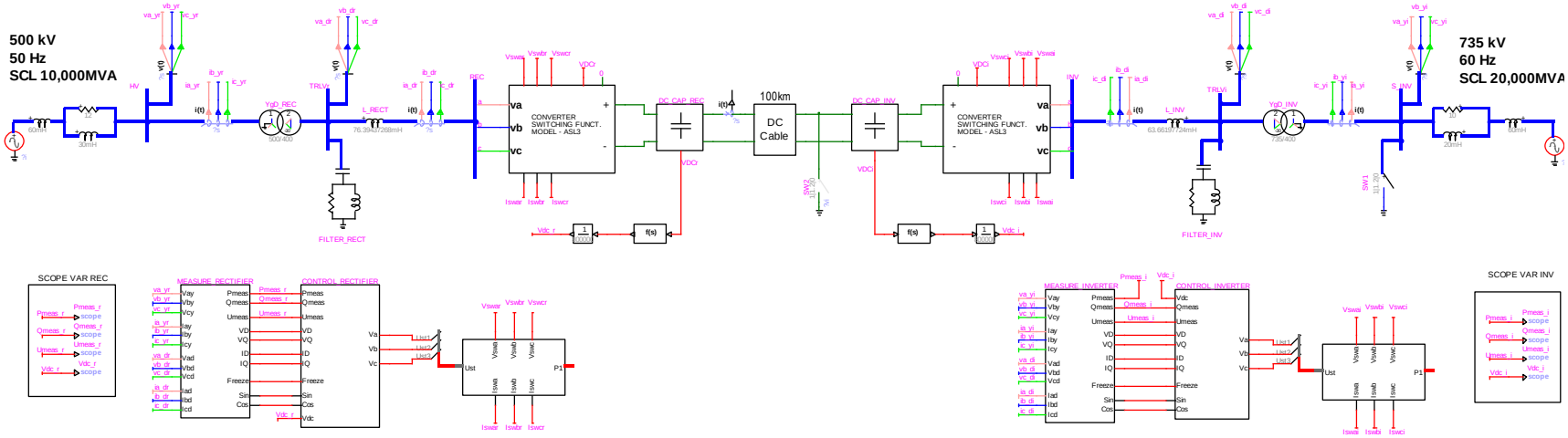
Parameters Rectifier	**Unit**	**Value**		**Parameters Inverter**	**Unit**	**Value**
Short-circuit Level	MVA	10,000		Short-circuit Level	MVA	20,000
AC voltage	kV	500		AC voltage	kV	735
Frequency	Hz	50		Frequency	Hz	60
Transformer Voltage (Prim/Sec)	kV	500/400		Transformer Voltage (Prim/Sec)	kV	735/400
Transformer capacity	MVA	1,000		Transformer capacity	MVA	1,000
Transformer impedance	%	10		Transformer impedance	%	10
Filter Size	MVAr	2x100		Filter Size	MVAr	2x100
Series reactance	mH	76.4		Series reactance	mH	63.7
DC capacitors	µF	2x70		DC capacitors	µF	2x70
DC Cable:						
DC Voltage	kV dc	±400				
Cable R	Ω/km	0.0139				
Cable L	mH/km	0.159				
Cable C	µF/km	0.231				
Cable Length	km	2x100				

ii. EMTP-RV Systems Design – AM, ASL3 and DML3 Models

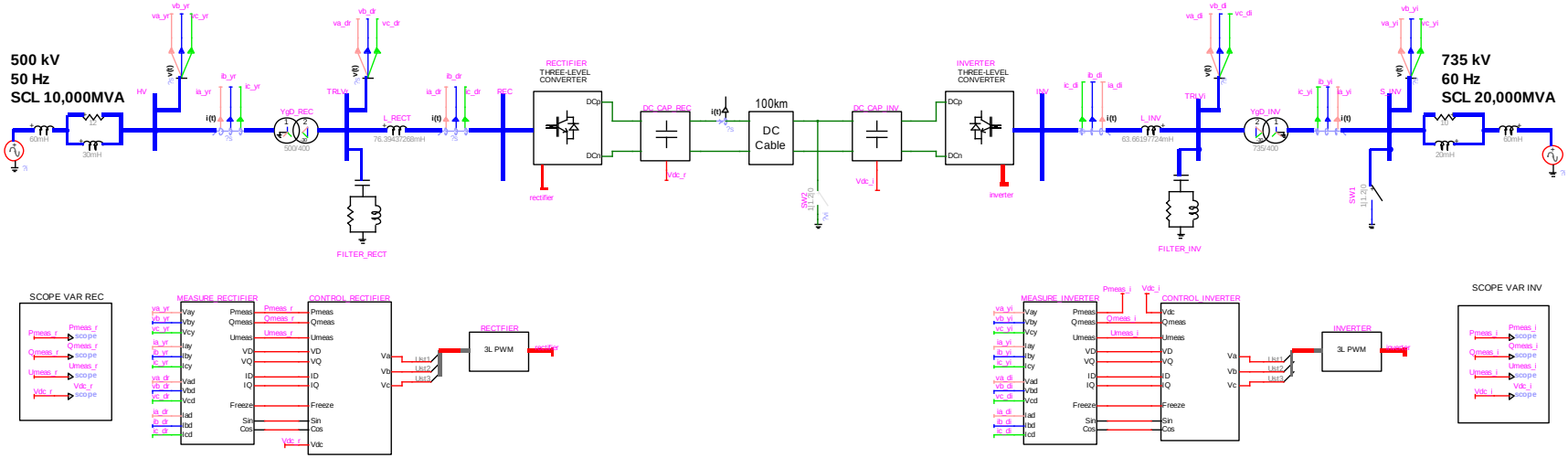
VSC-HVDC 1,000 MW, +-400 kVdc LINK
AVERAGE VALUE MODEL (AM)



VSC-HVDC 1,000 MW, +-400 kVdc LINK
TWO-LEVEL CONVERTER, SWITCHING FUNCTION MODEL (ASL3)

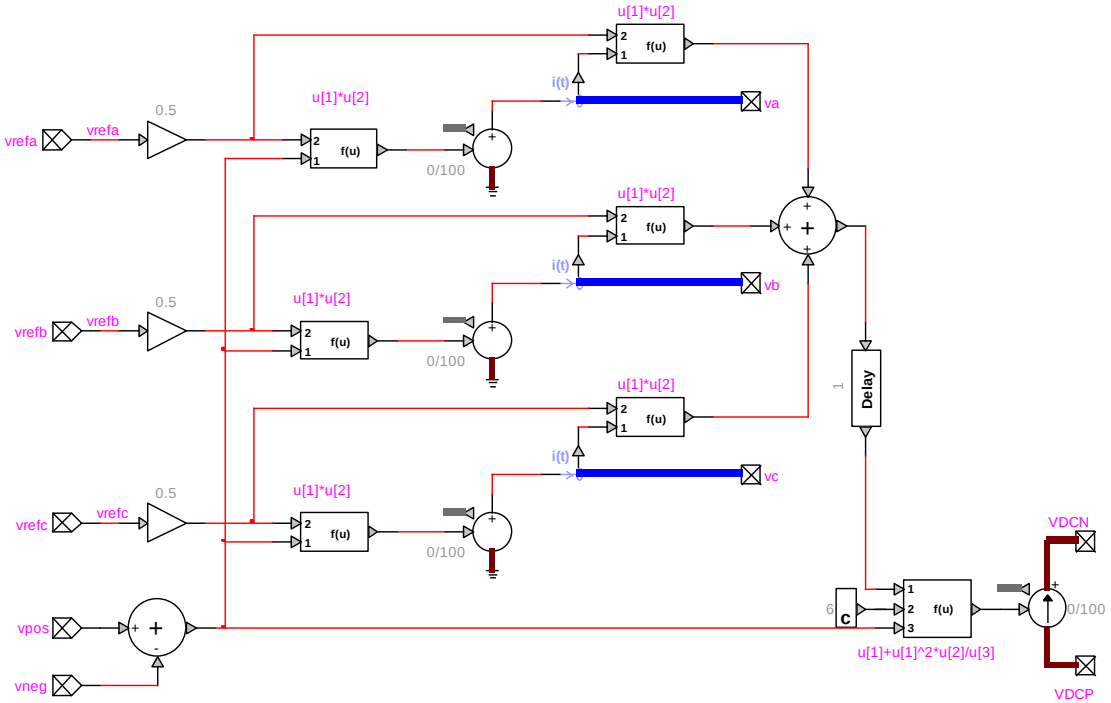


VSC-HVDC 1,000 MW, +-400 kVdc LINK
THREE-LEVEL CONVERTER, DETAILED MODEL (DML3)

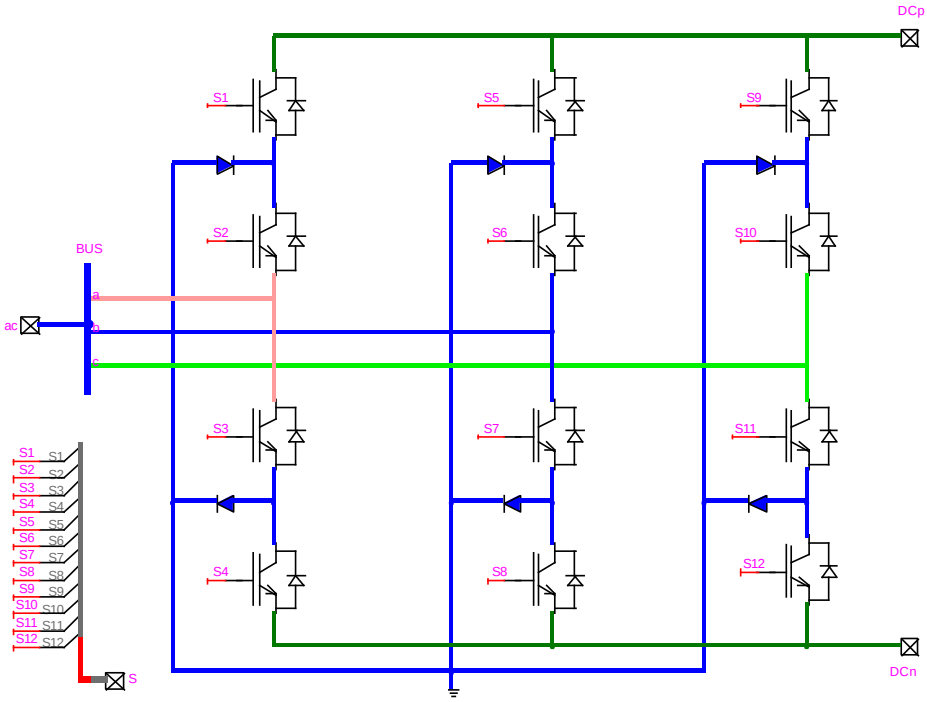


iii. EMTP-RV Converter – AM, ASL3 and DML3 Models

AM & ASL3 CONVERTER MODEL

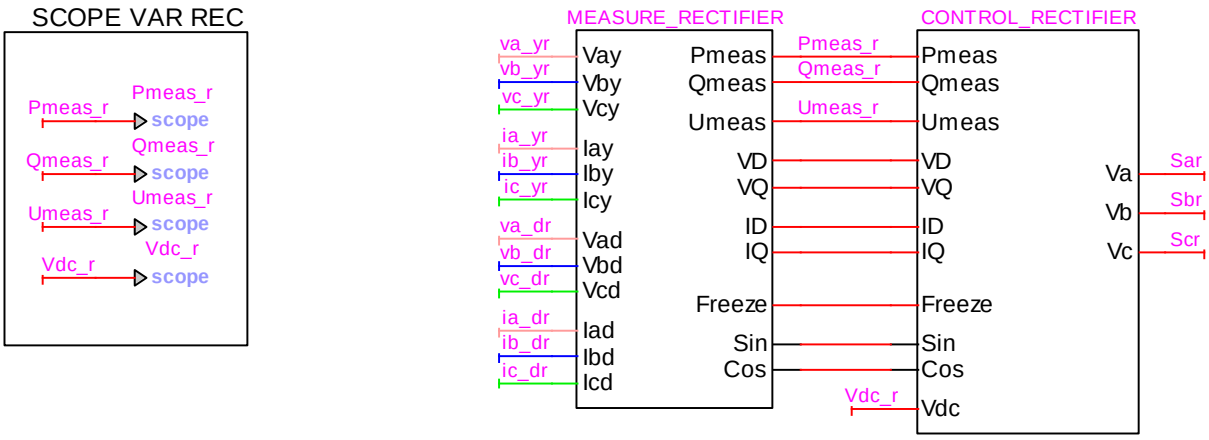


DML3 CONVERTER MODEL

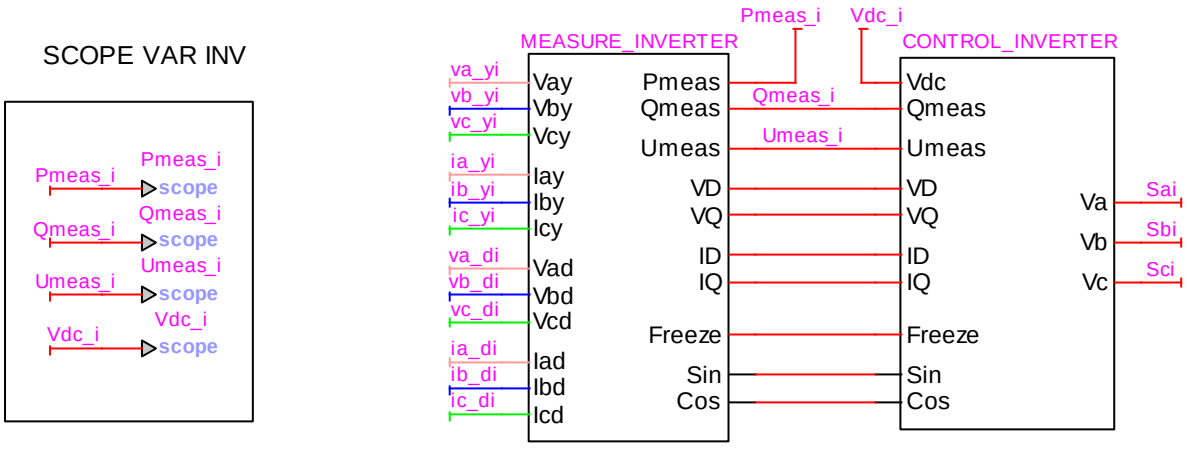


iv. EMTP-RV Control System (All models)

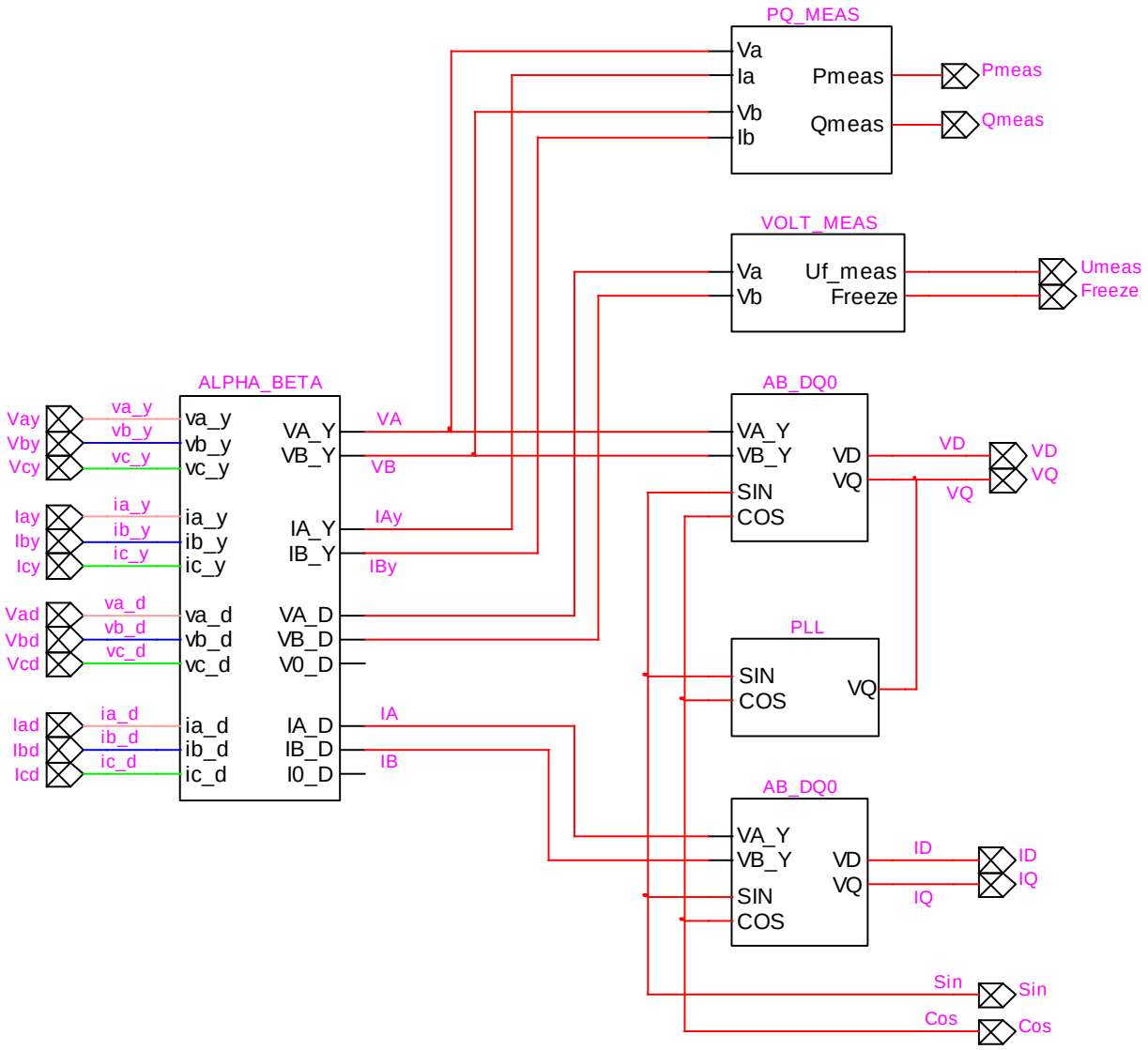
RECTIFIER CONTROL



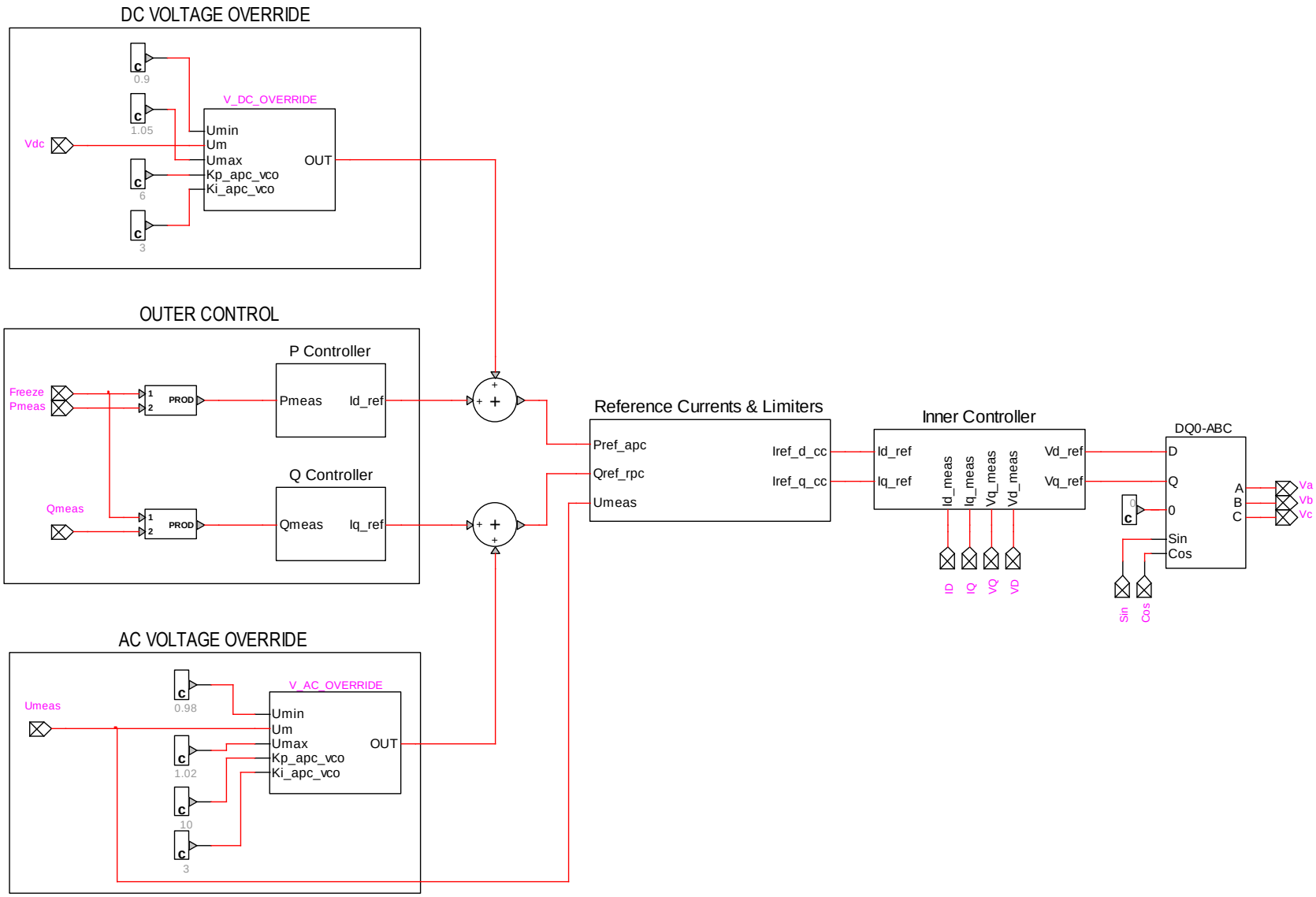
INVERTER CONTROL



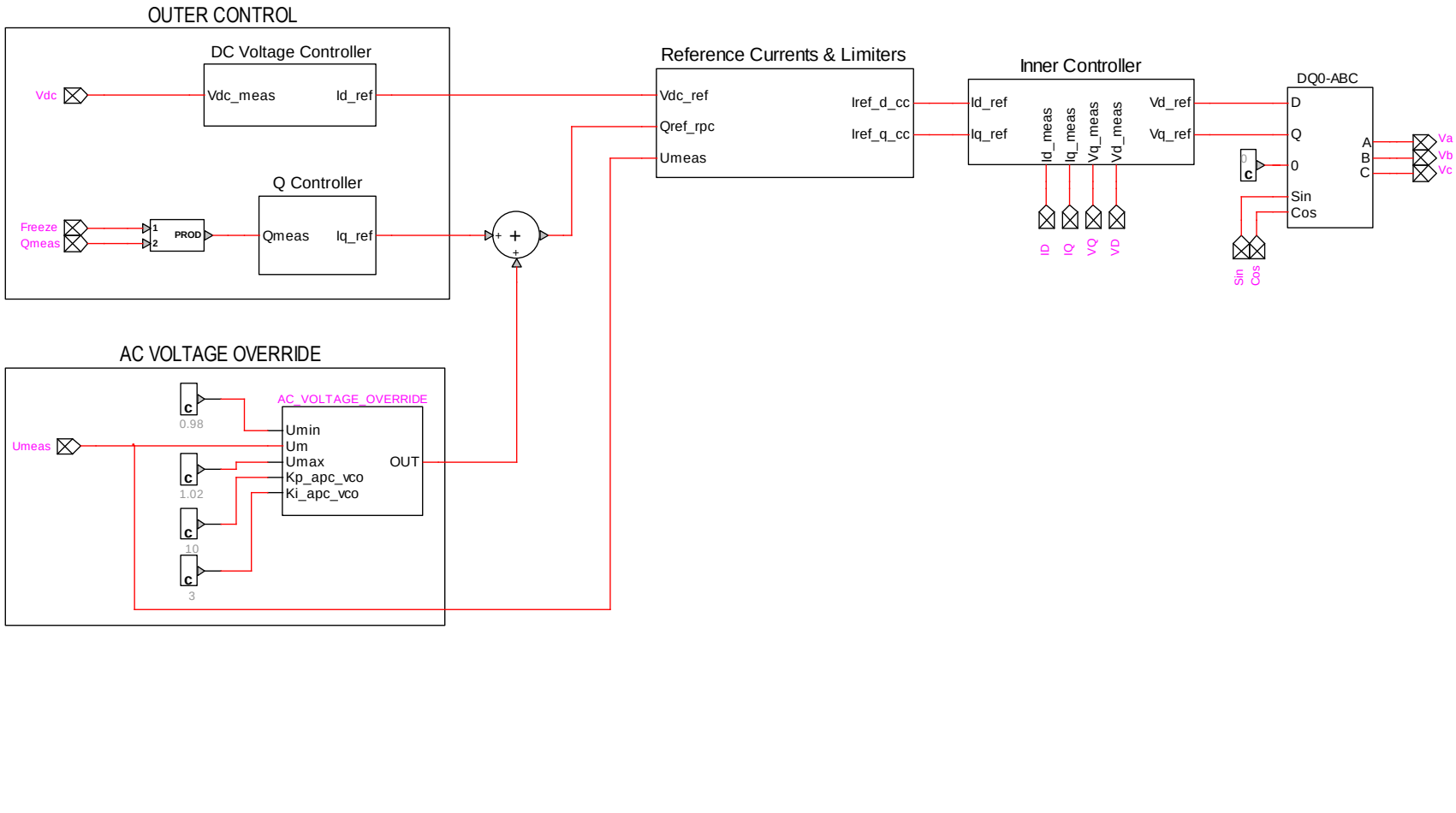
MEASUREMENTS BLOCK



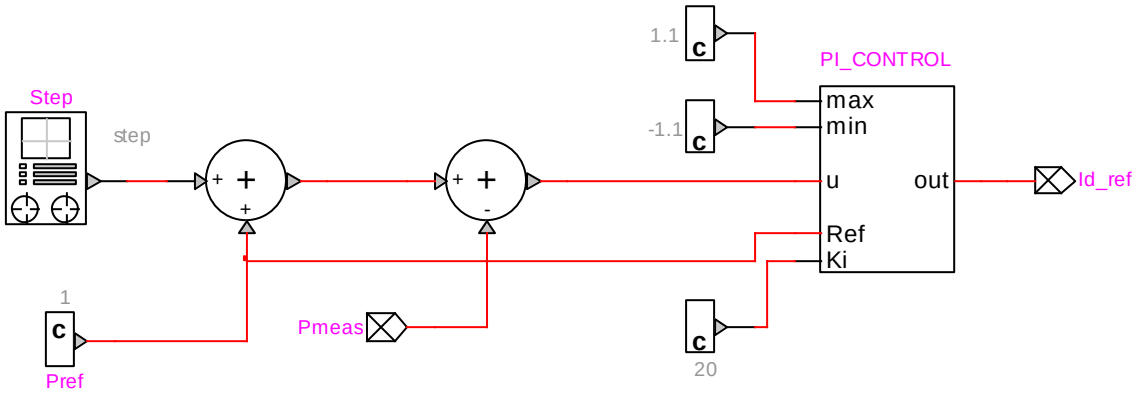
RECTIFIER CONTROL BLOCK



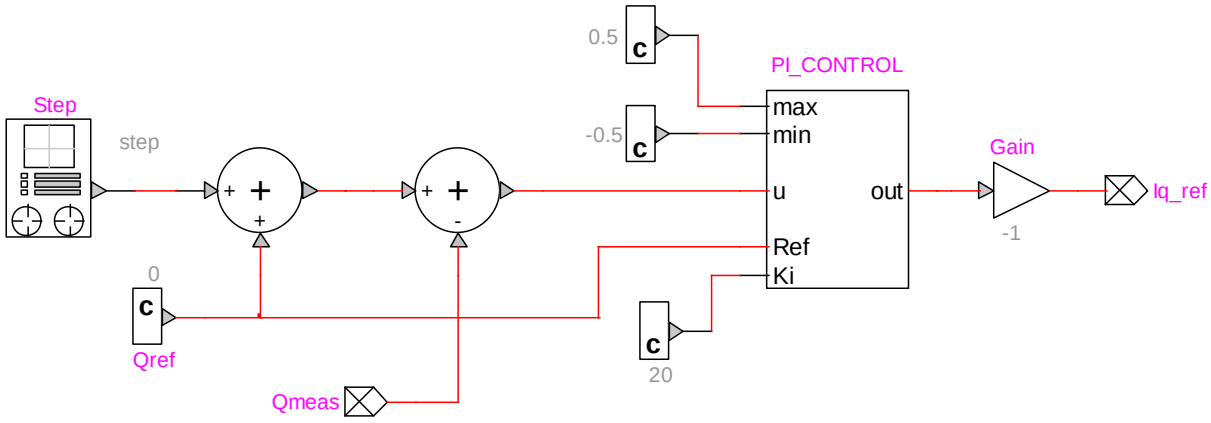
INVERTER CONTROL BLOCK



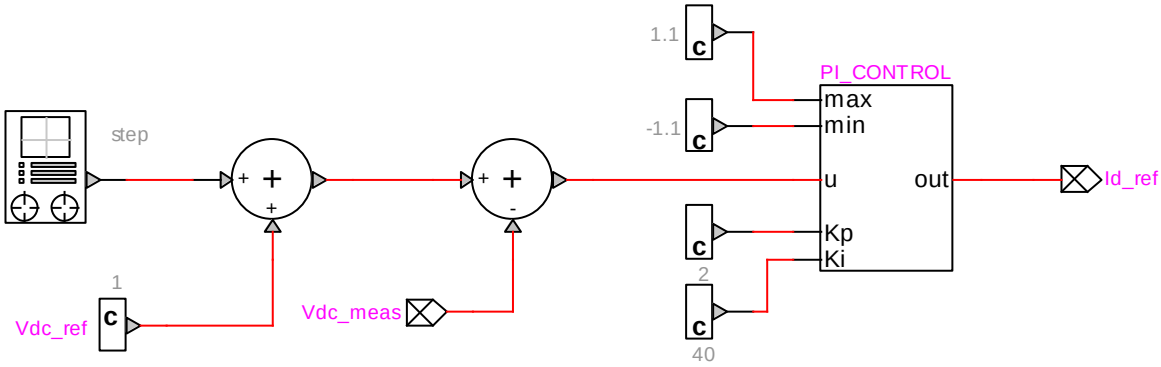
ACTIVE POWER CONTROL



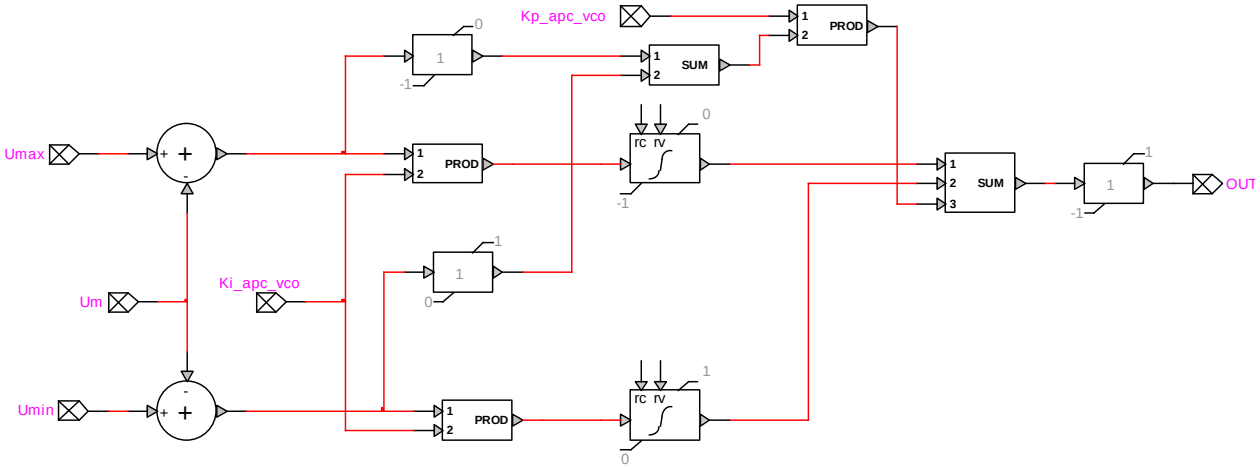
REACTIVE POWER CONTROL



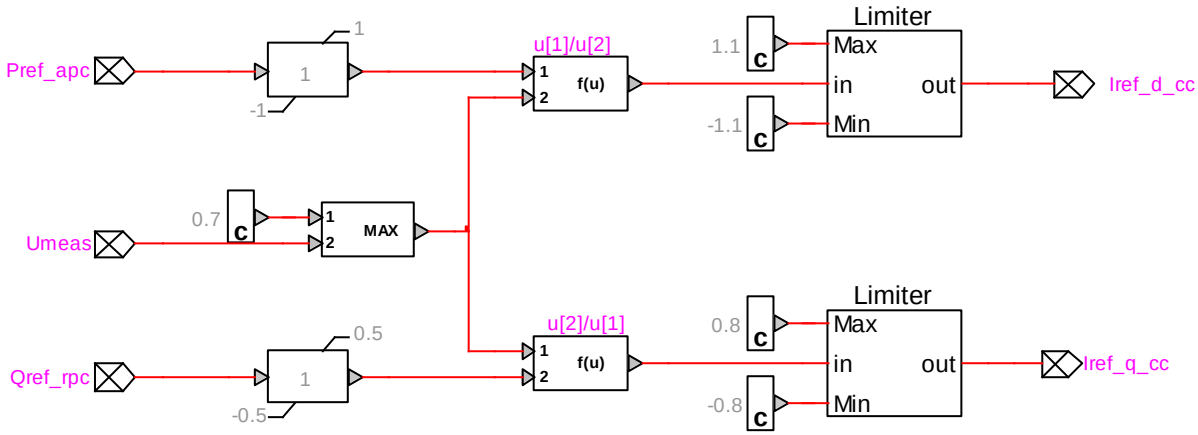
DC VOLTAGE CONTROL



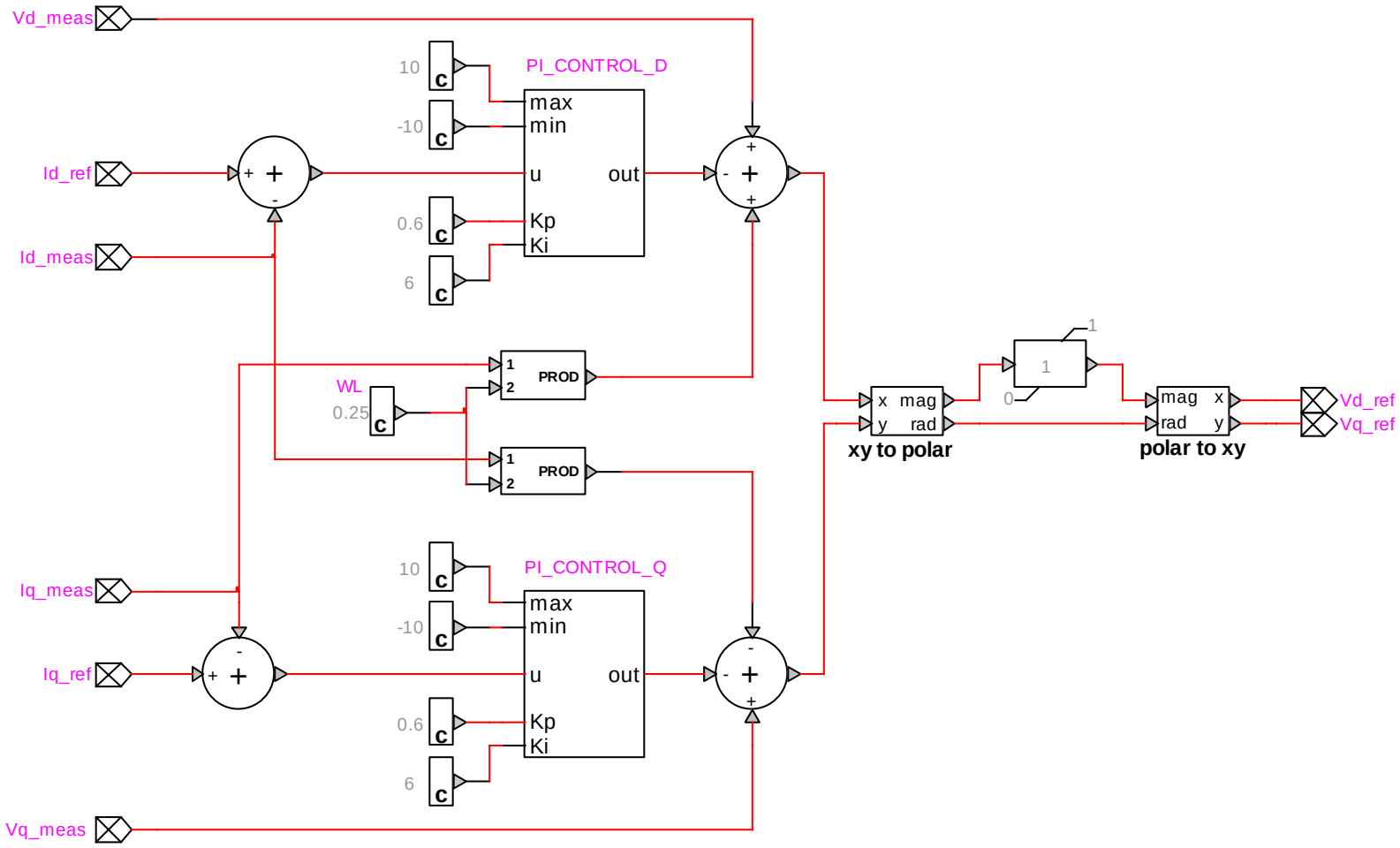
AC & DC VOLTAGE OVERRIDE CONTROL



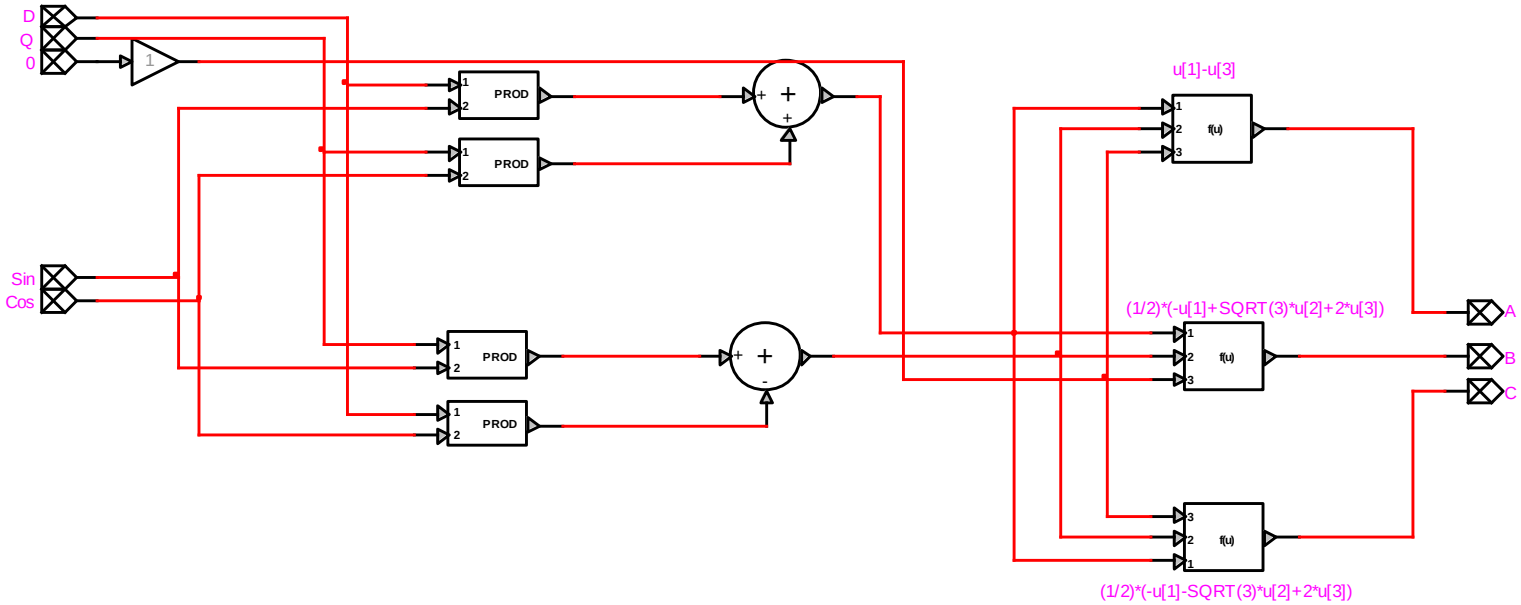
CURRENT REFERENCE AND LIMITERS



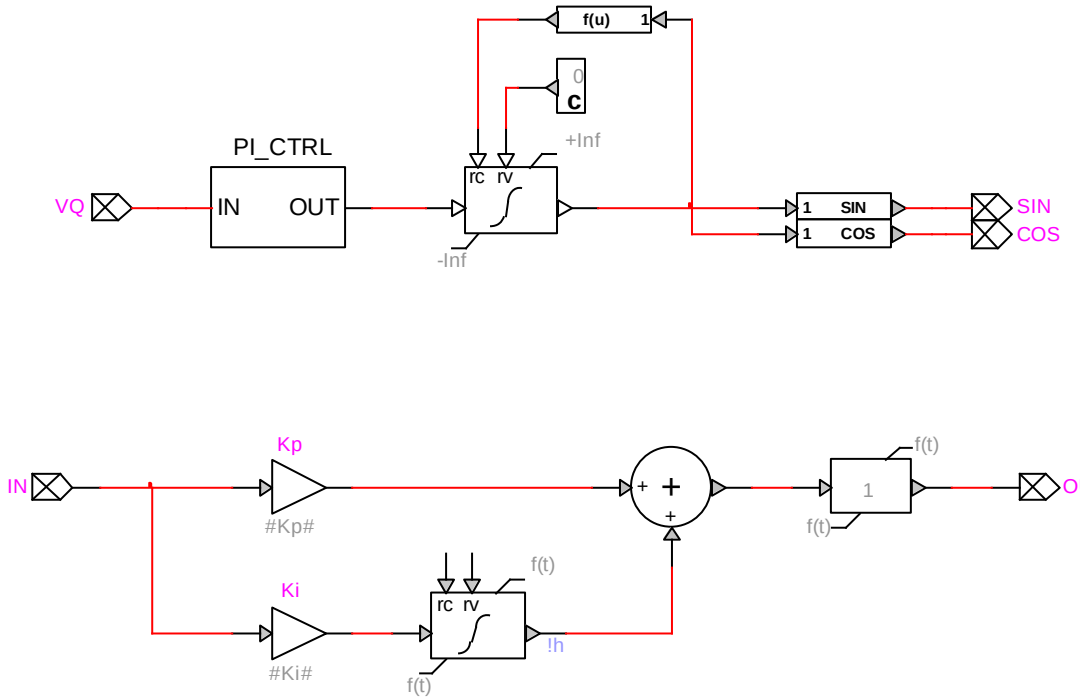
INNER CURRENT CONTROL



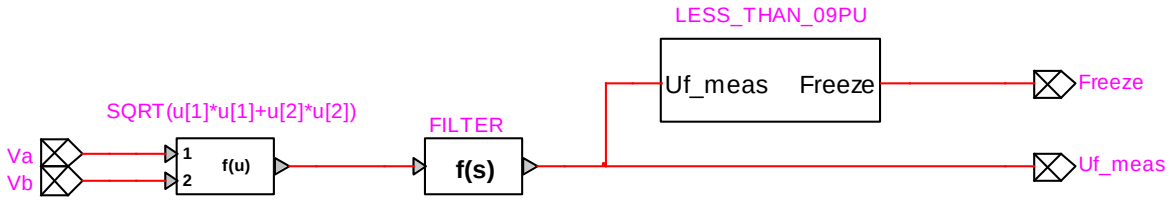
DQ0-ABC TRANSFORMATION

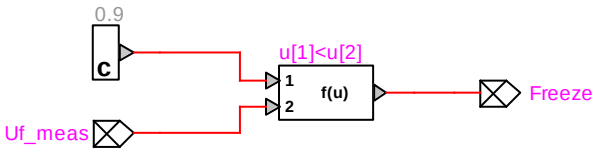


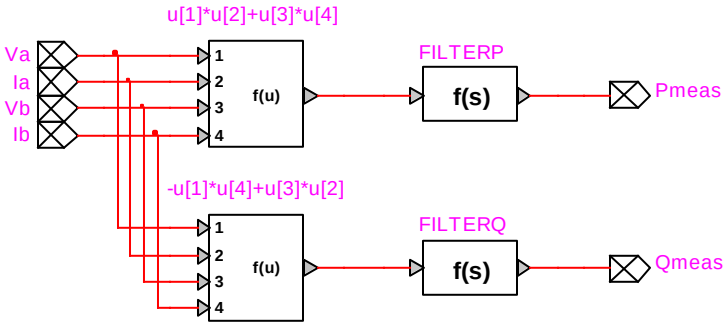
PLL CONTROL BLOCK



VOLTAGE AND POWER CALCULATION

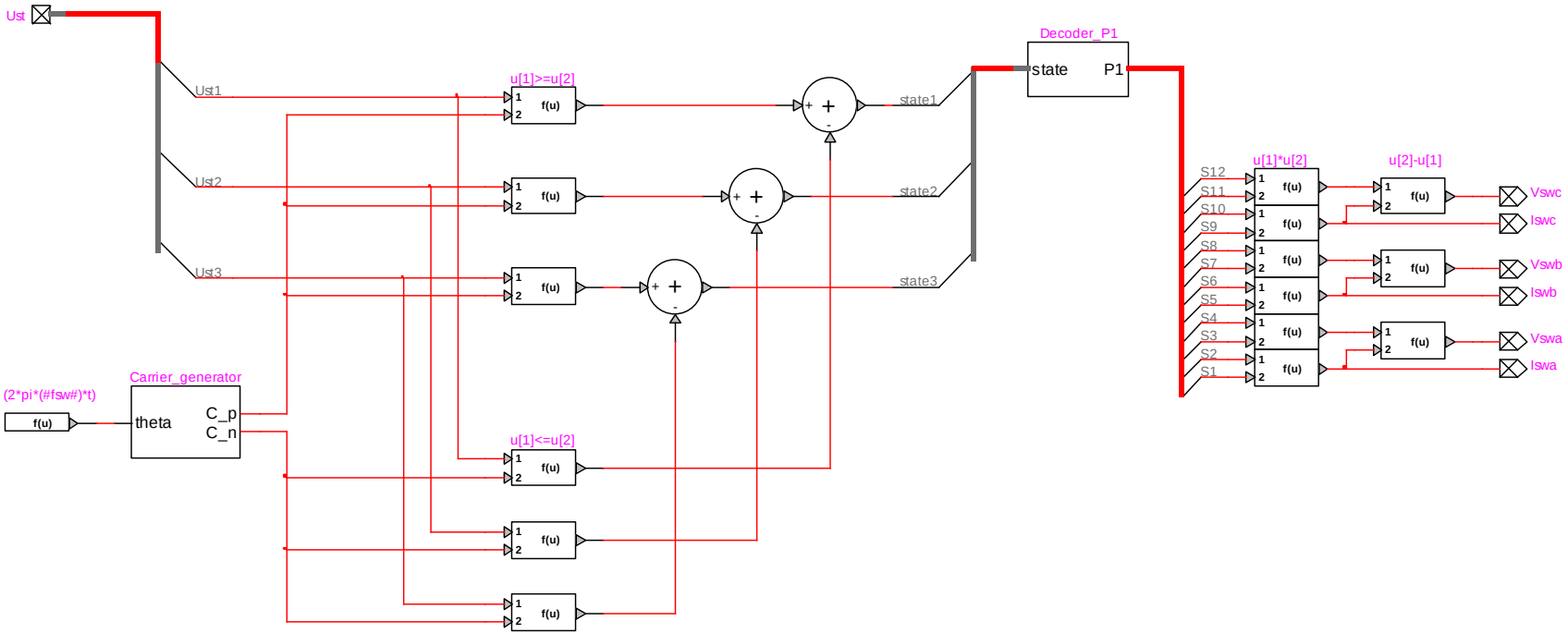




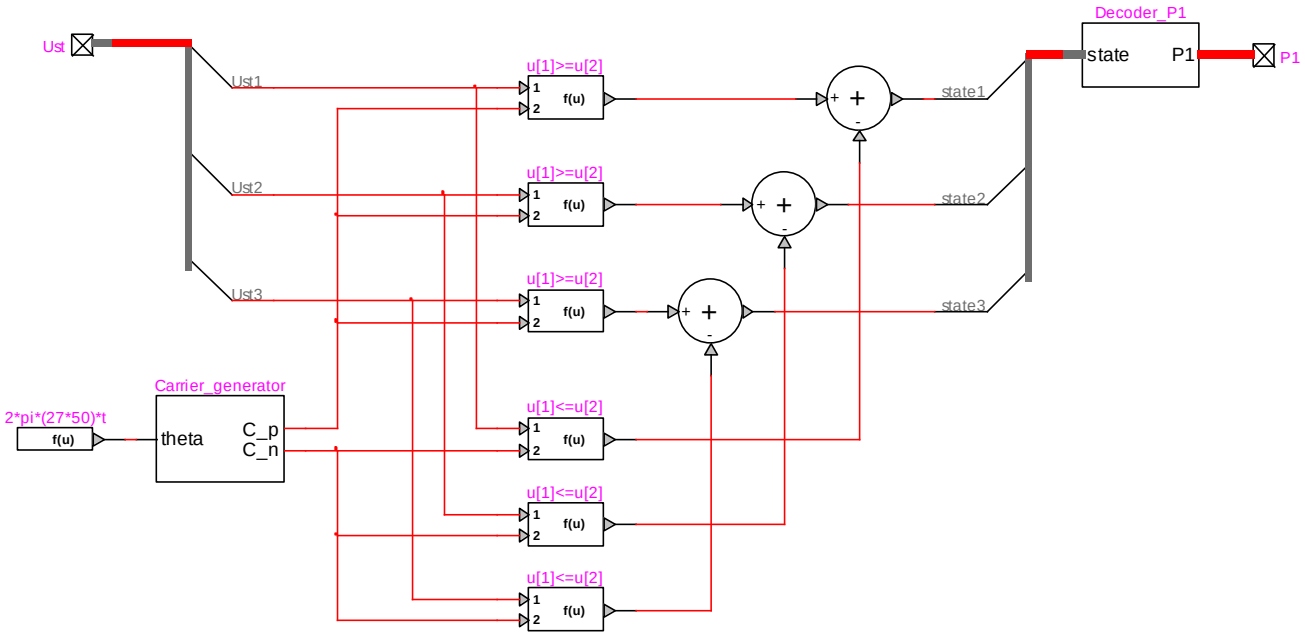


v. EMTP-RV PWM CONTROL – ASL3 and DML3 Models

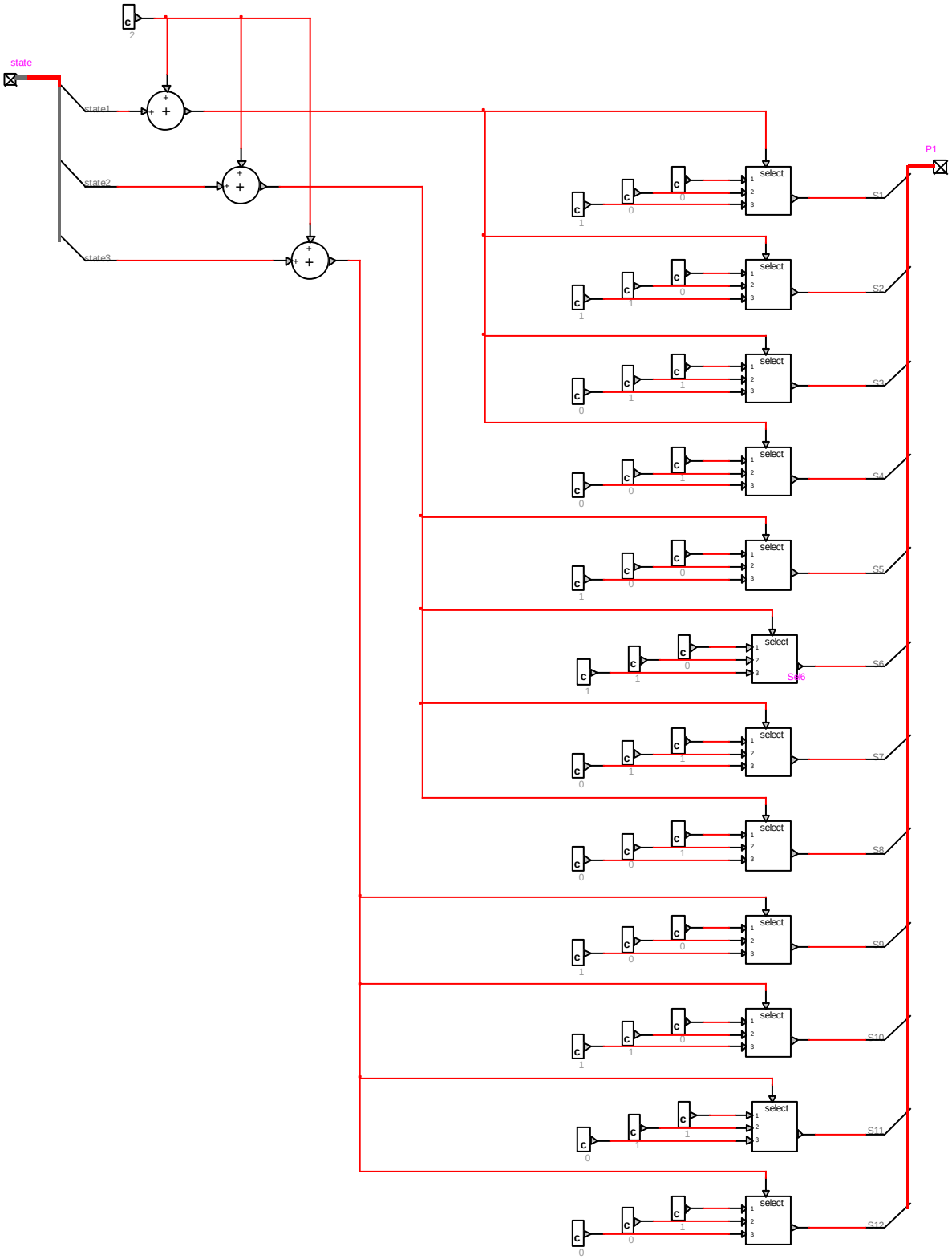
PWM CONTROL – ASL3 MODEL



PWM CONTROL – DML3 MODEL



DECODER OF SIGNAL P1



APPENDIX C TEST CASE 2 DATA AND EMTP-RV MODELS DESIGN

i. System Data

Parameters Rectifier	**Unit**	**Value**		**Parameters Inverter**	**Unit**	**Value**
Gen. Wind Farm 1	MVA	600		SCL SYS1	MVA	20,000
Gen. Wind Farm 2	MVA	600		Frequency SYS1	Hz	50
Gen. Wind Farm 3	MVA	600		AC voltage SYS1	kV	400
AC voltage REC1	kV	400		Capacity INV1	MVA	1,500
AC voltage REC2	kV	400		SCL SYS2	MVA	15,000
AC voltage REC3	kV	400		Frequency SYS2	Hz	50
Frequency REC1	Hz	50		AC voltage SYS2	kV	400
Frequency REC1	Hz	50		Capacity INV2	MVA	1,000
Frequency REC1	Hz	50		Transformer impedance	%	15
Transformer impedance	%	15		Transformer Voltage	kV	400/320
Transformer Voltage	kV	400/320		Filter Size	MVAr	2x100
Filter Size	MVAr	2x100		Series reactance	%	15
Series reactance	%	15		DC capacitors	µF	2x70
DC capacitors	µF	2x70				
Transformer impedance	%	15				
DC Cable:						
DC Voltage	kV dc	±320				
Length REC1-INV1	km	100				
Length REC1-REC2	km	50				
Length REC2-REC3	km	100				
Length REC2-INV2	km	25				
Length INV1-INV2	km	75				

CABLE DATA – EMTP-RV WIDEBAND MODEL

Geometrical and electrical data

Cable data

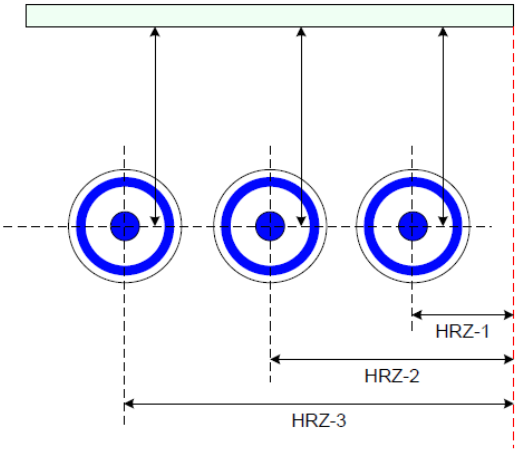
Cable type: Single core Number of cables: 2

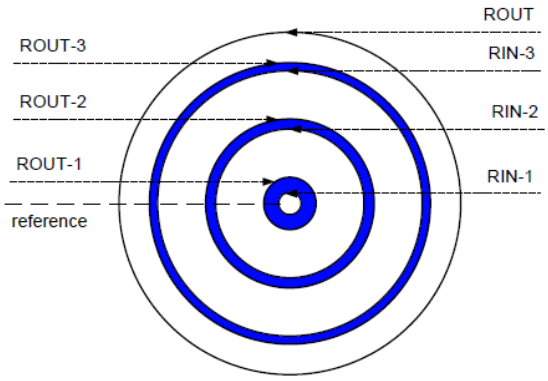
Cross-bond the Sheaths: ☐

	Cable Number	Number of conductors	Vertical Distance (m)	Horizontal Distance (m)	Outer Insulation Radius (m)
1	1	2	1.33	-0.25	63.9e-3
2	2	2	1.33	0.25	63.9e-3

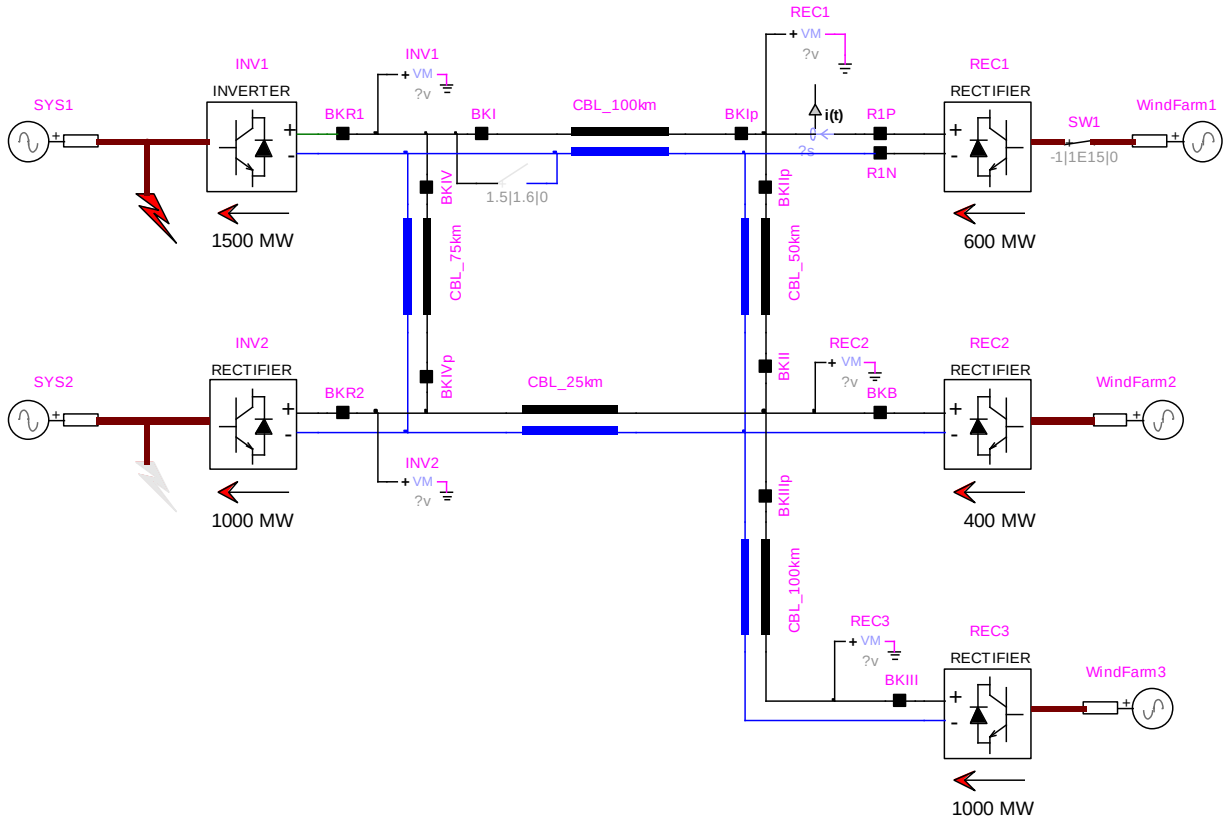
Conductor/Insulator data

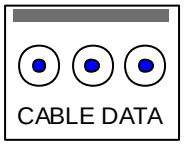
	Cable Number	Conductor Number	Inside Radius Rin [m]	Outside Radius Rout [m]	Resistivity Rho [Ohm-m]	Relative Permea-bility MUE	Insulator Relative Permea-bility MUE-IN	Insulator Relative Permi-ttivity EPS-IN	Insulator Loss Factor LFCT-IN	Phase Number KPH
1	1	1	0	32.0e-3	1.72e-8	1	1	2.5	0.004	1
2	1	2	56.9e-3	58.2e-3	2.83e-8	1	1	2.5	0.004	2
3	2	1	0	32.0e-3	1.72e-8	1	1	2.5	0.004	3
4	2	2	56.9e-3	58.2e-3	2.83e-8	1	1	2.5	0.004	4





ii. EMTP-RV System Design – MTDC VSC-HVDC



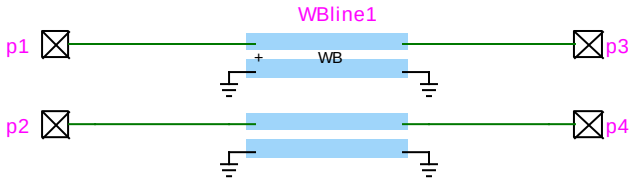


model in: cablewb_100km_rv.cyz

cableWB_100km

cablewb_100km_rv.cyz

model in: wbfit_cablewb_100km_rv.dat

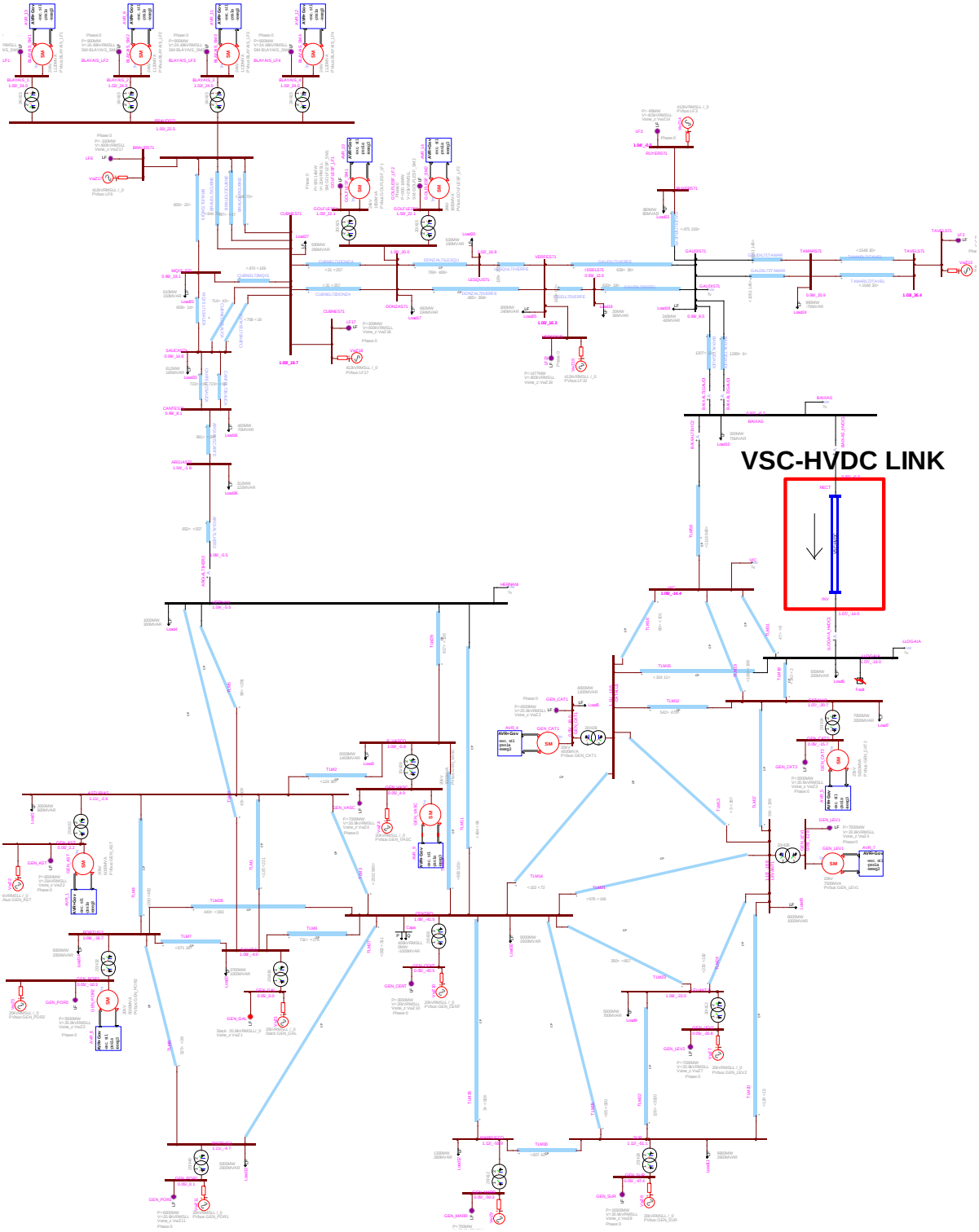


APPENDIX D TEST CASE 3 DATA AND EMTP-RV MODELS DESIGN

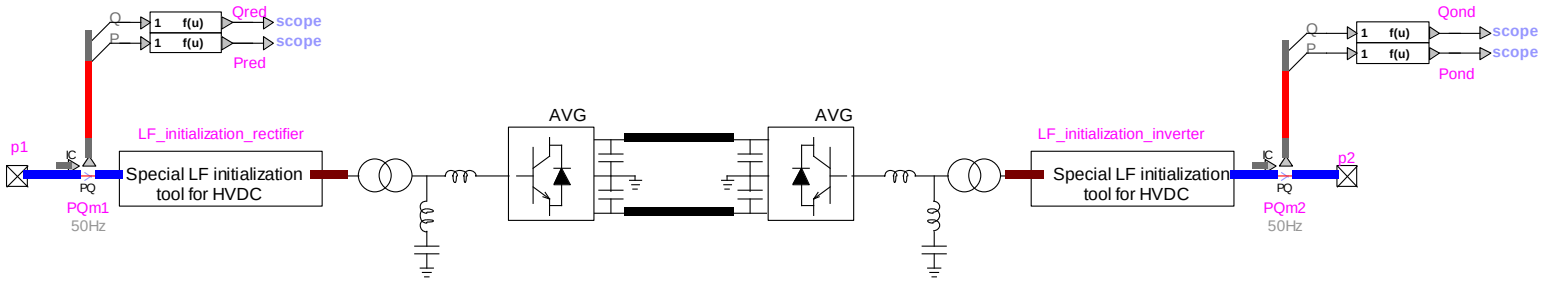
i. System Data

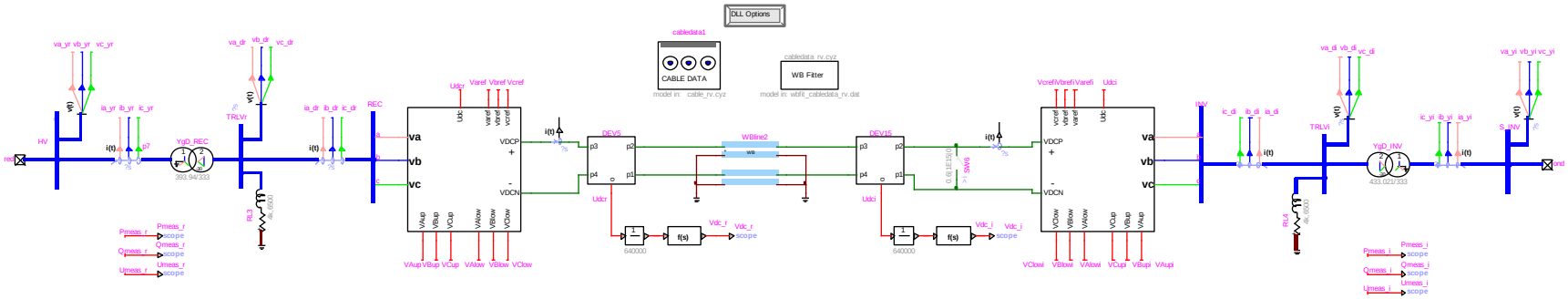
Parameters Rectifier FRANCE	**Unit**	**Value**		**Parameters Inverter SPAIN**	**Unit**	**Value**
Short-circuit Level	MVA	10,000		Short-circuit Level	MVA	10,000
AC voltage	kV	400		AC voltage	kV	400
Frequency	Hz	50		Frequency	Hz	50
Transformer Voltage (Prim/Sec)	kV	400/333		Transformer Voltage (Prim/Sec)	kV	400/333
Transformer capacity	MVA	1,059		Transformer capacity	MVA	1,059
Transformer impedance	%	18		Transformer impedance	%	18
Filter Size	MVAr	N/A		Filter Size	MVAr	N/A
Series reactance	mH	50		Series reactance	mH	50
SM capacitors	mF	10		SM capacitors	µF	10
DC Cable: Same configuration and cable model as Test Case 2						
DC Voltage	kV dc	±320				
Cable Length	km	2x70				

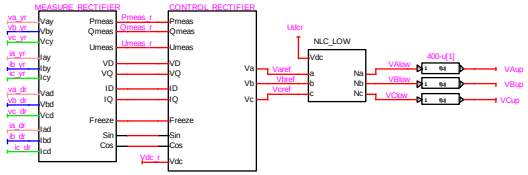
ii. EMTP-RV Design – France-Spain Interconnection

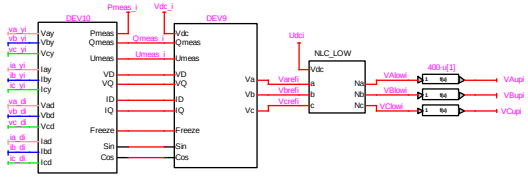


MMC-HVDC AMM MODEL

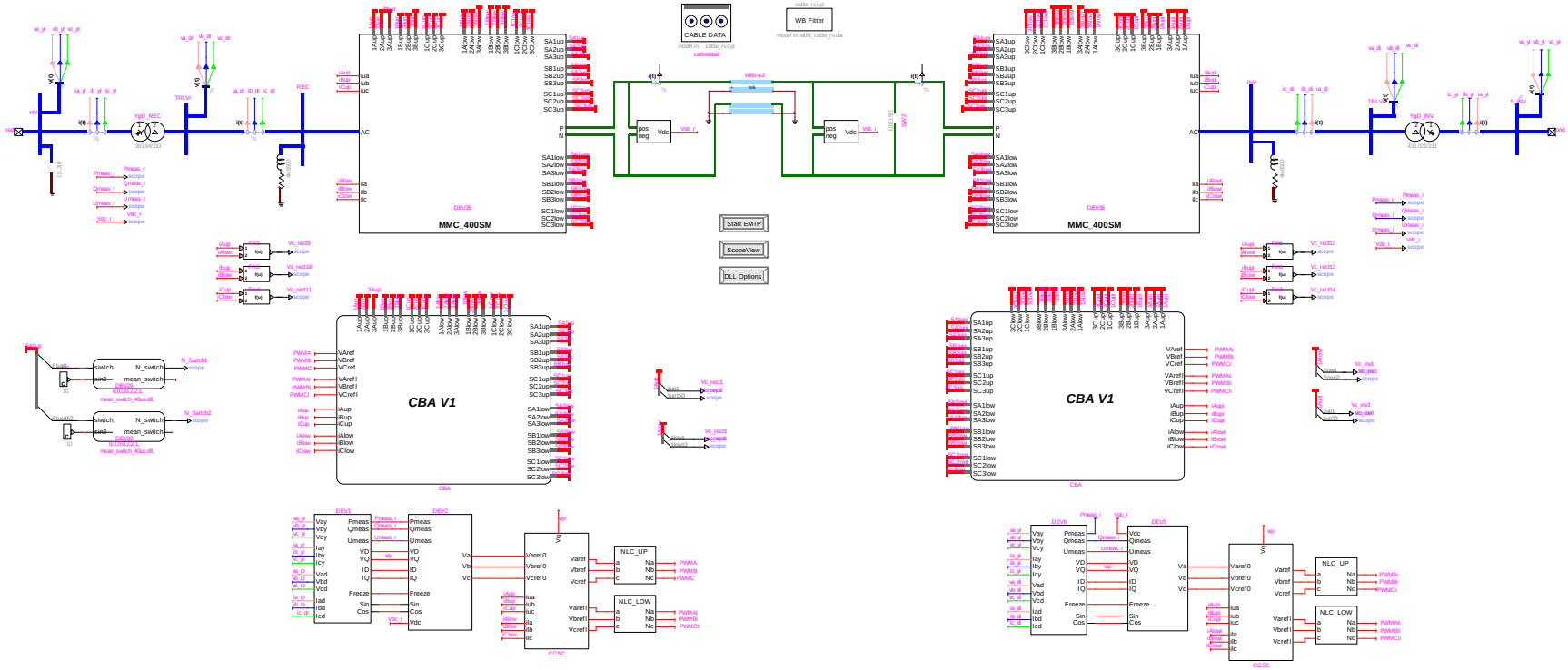






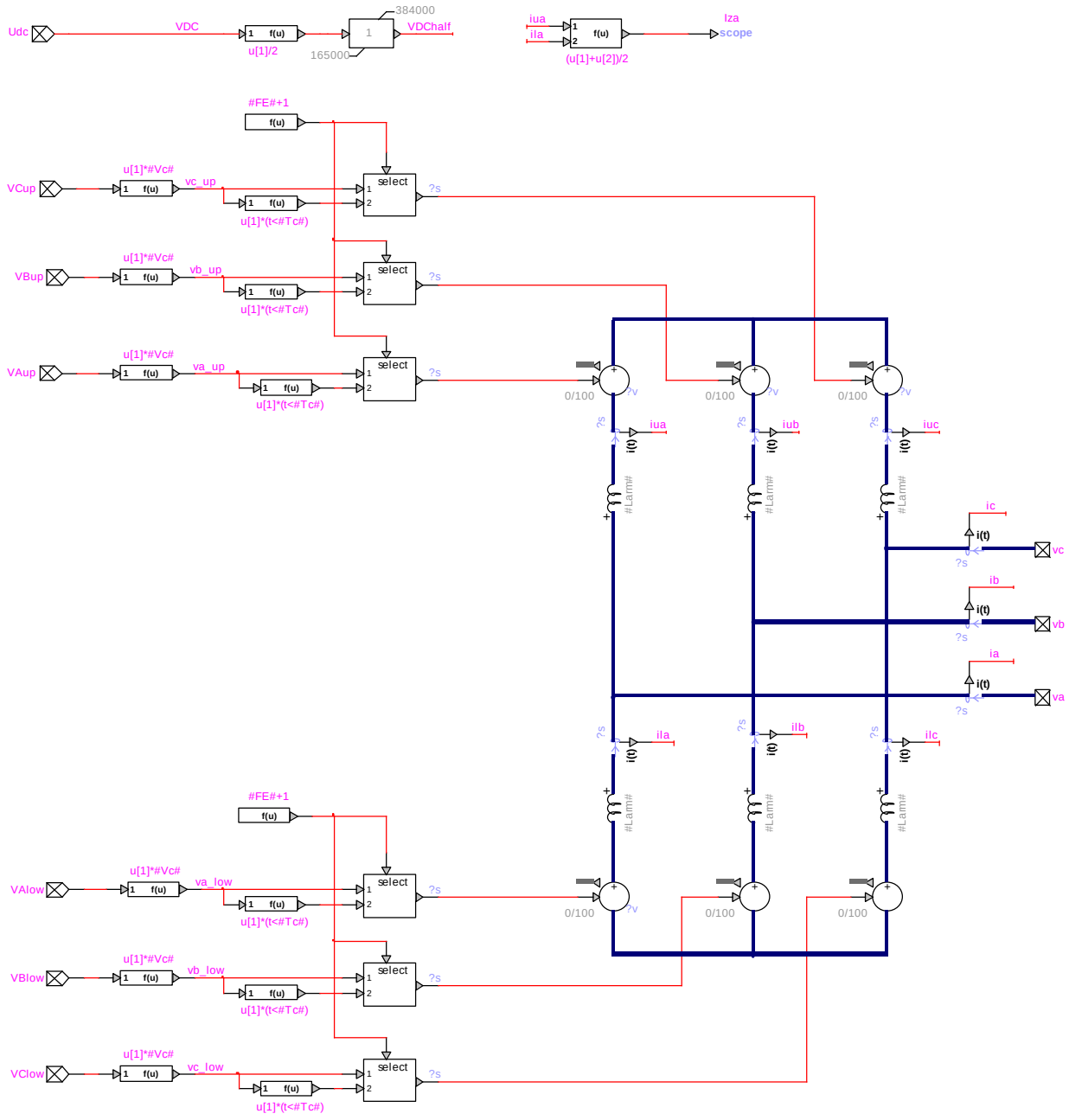


MMC-HVDC DMM MODEL

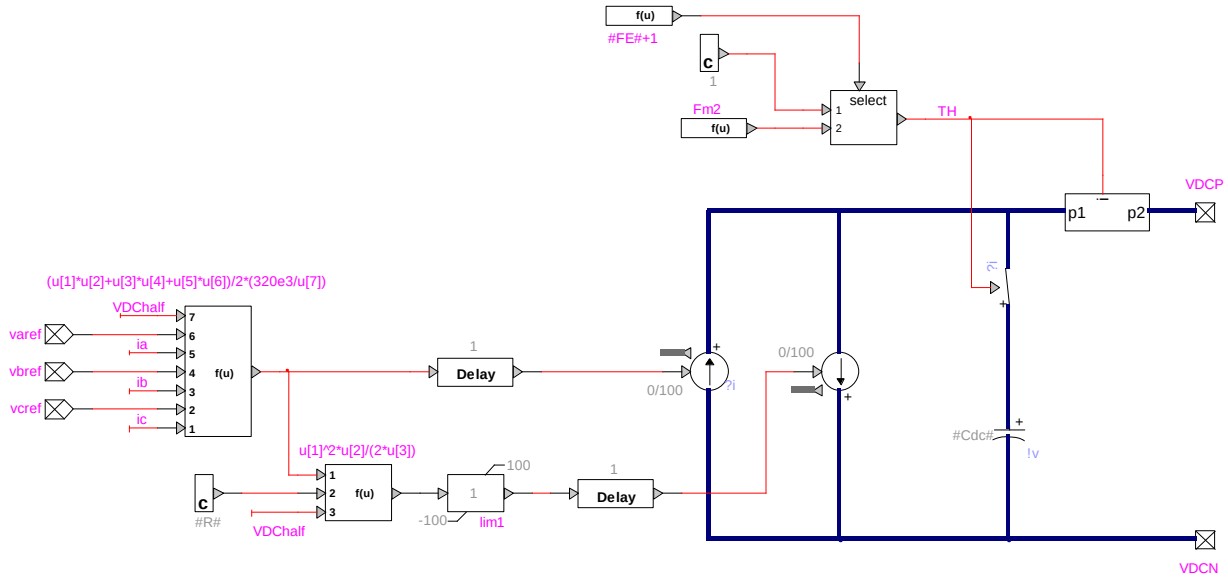


iii. EMTP-RV Converter – AMM and DMM Models

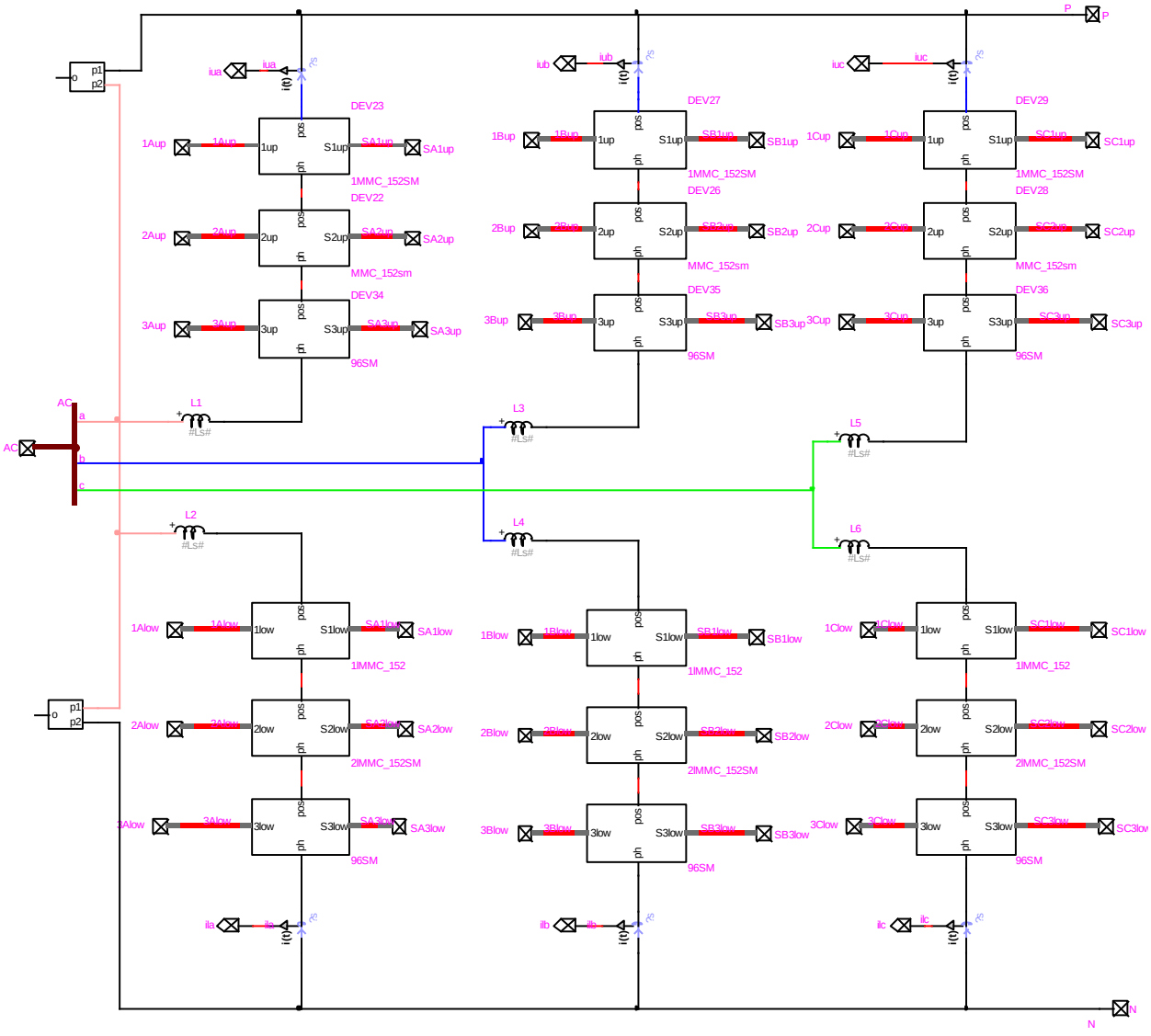
AMM CONVERTER – AC SIDE

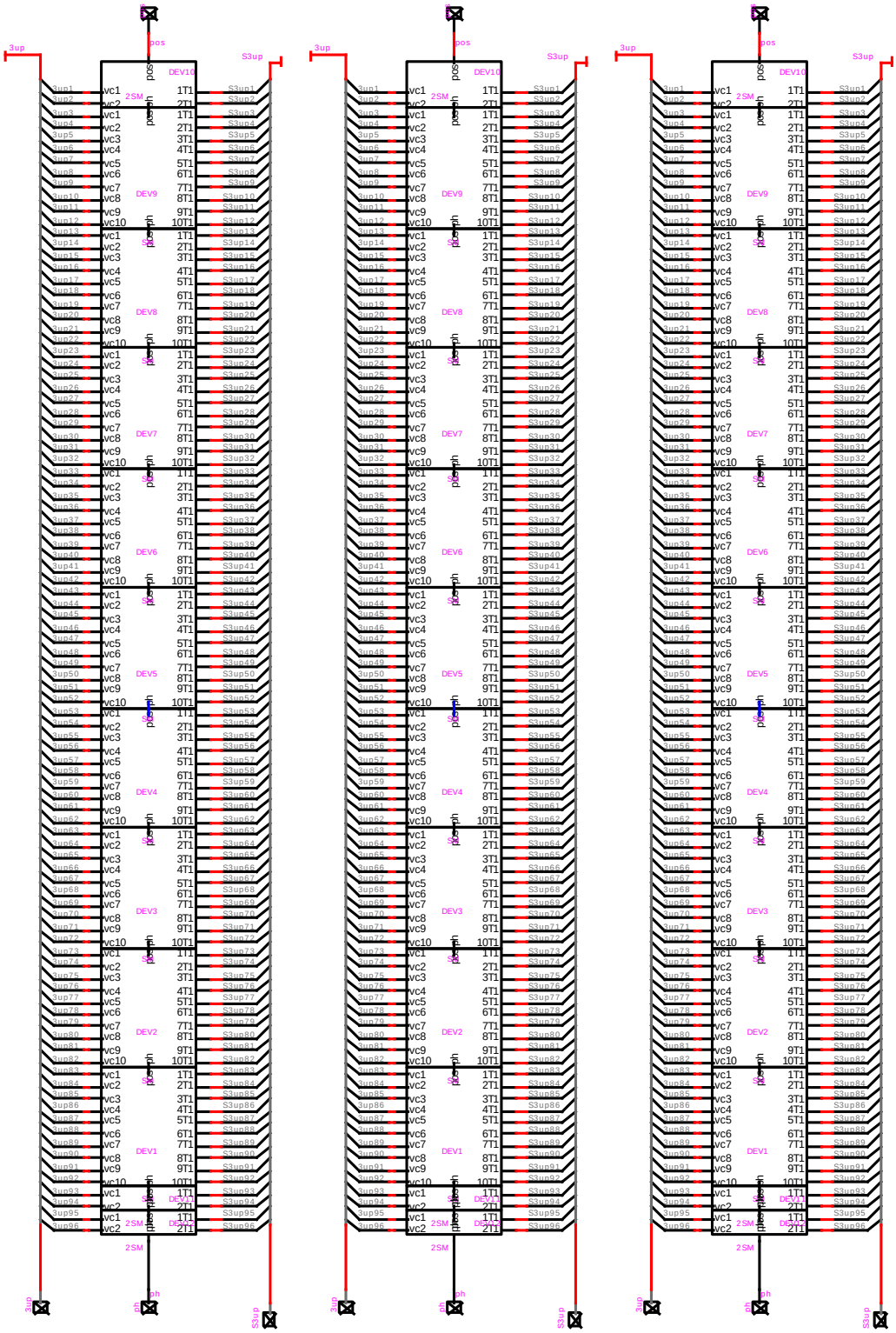


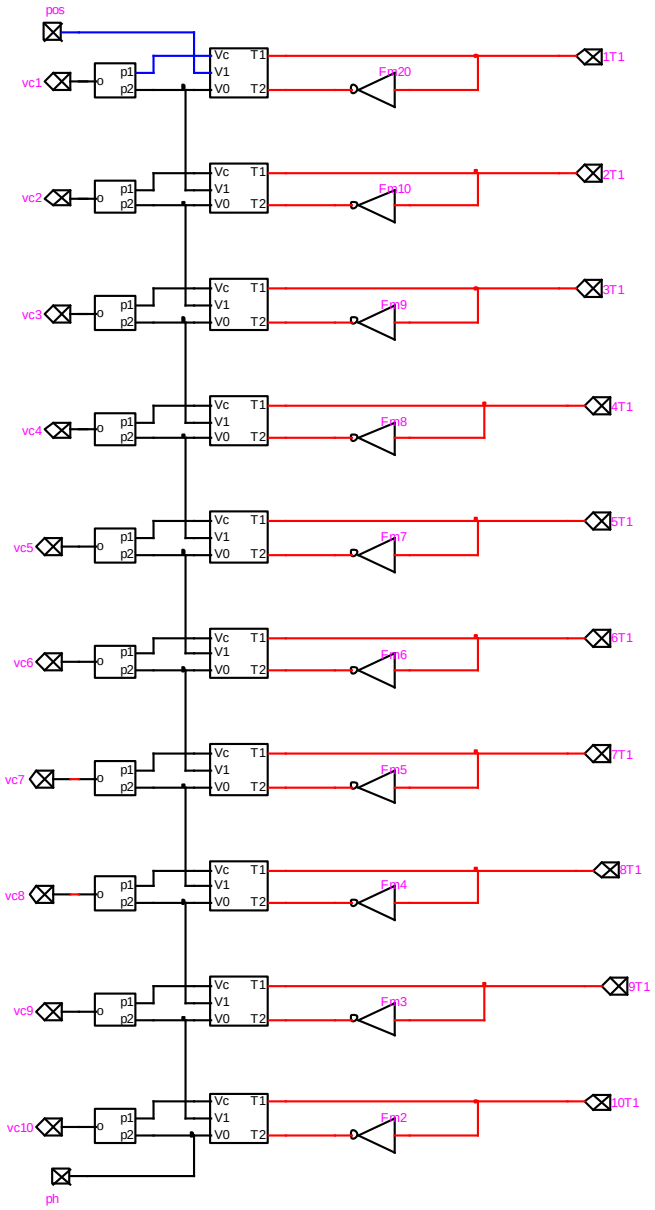
AMM CONVERTER – DC SIDE

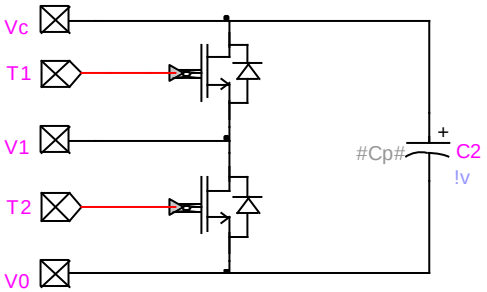


DMM CONVERTER MODEL



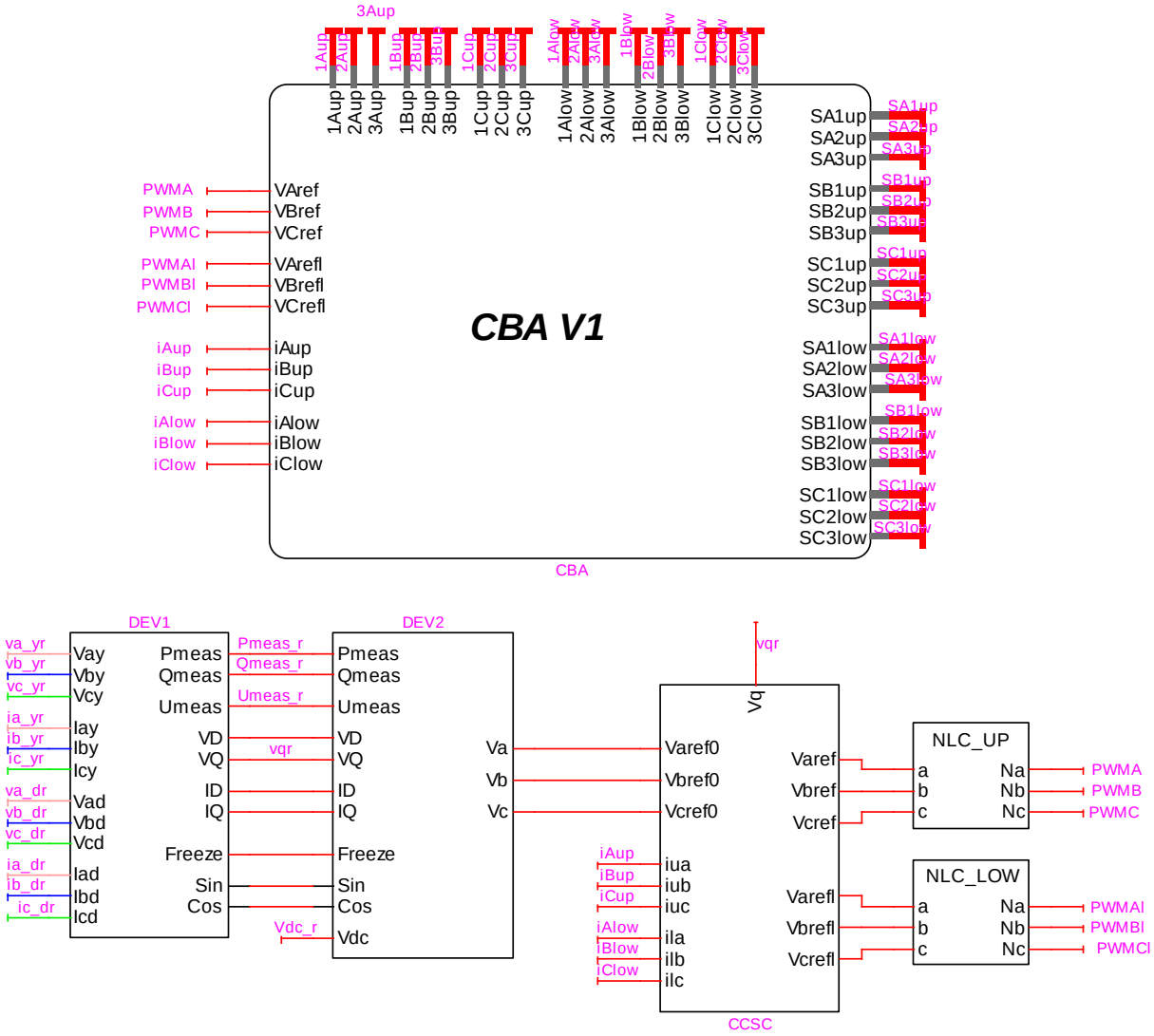



pos
vc1
vc2
vc3
vc4
vc5
vc6
vc7
vc8
vc9
vc10
ph
p1
p2
Vc
V1
V0
T1
T2
Fm20
Fm10
Fm9
Fm8
Fm7
Fm6
Fm5
Fm4
Fm3
Fm2
1T1
2T1
3T1
4T1
5T1
6T1
7T1
8T1
9T1
10T1

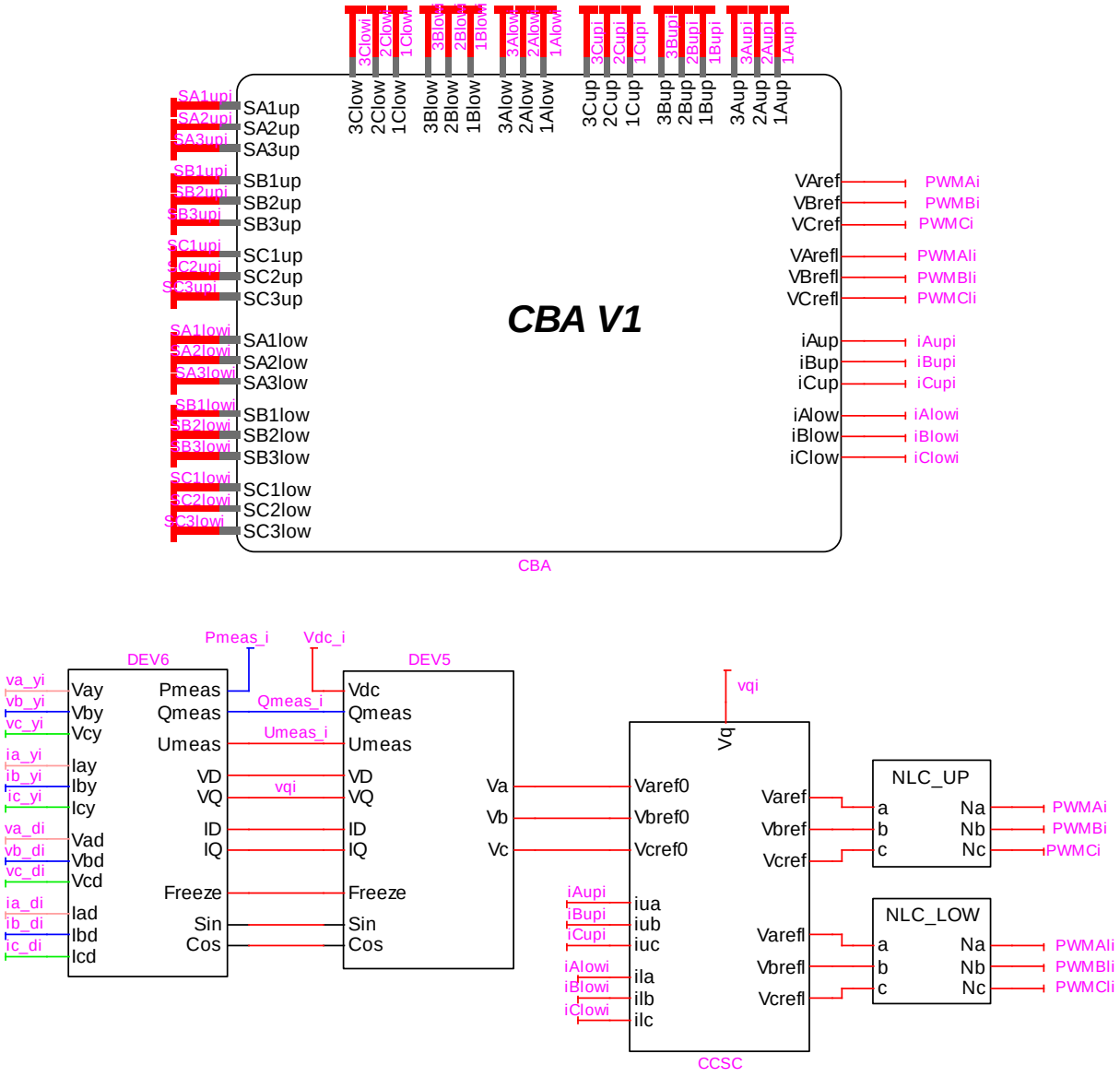

Vc
T1
V1
T2
V0
#Cp#
C2
!v

iv. Control System

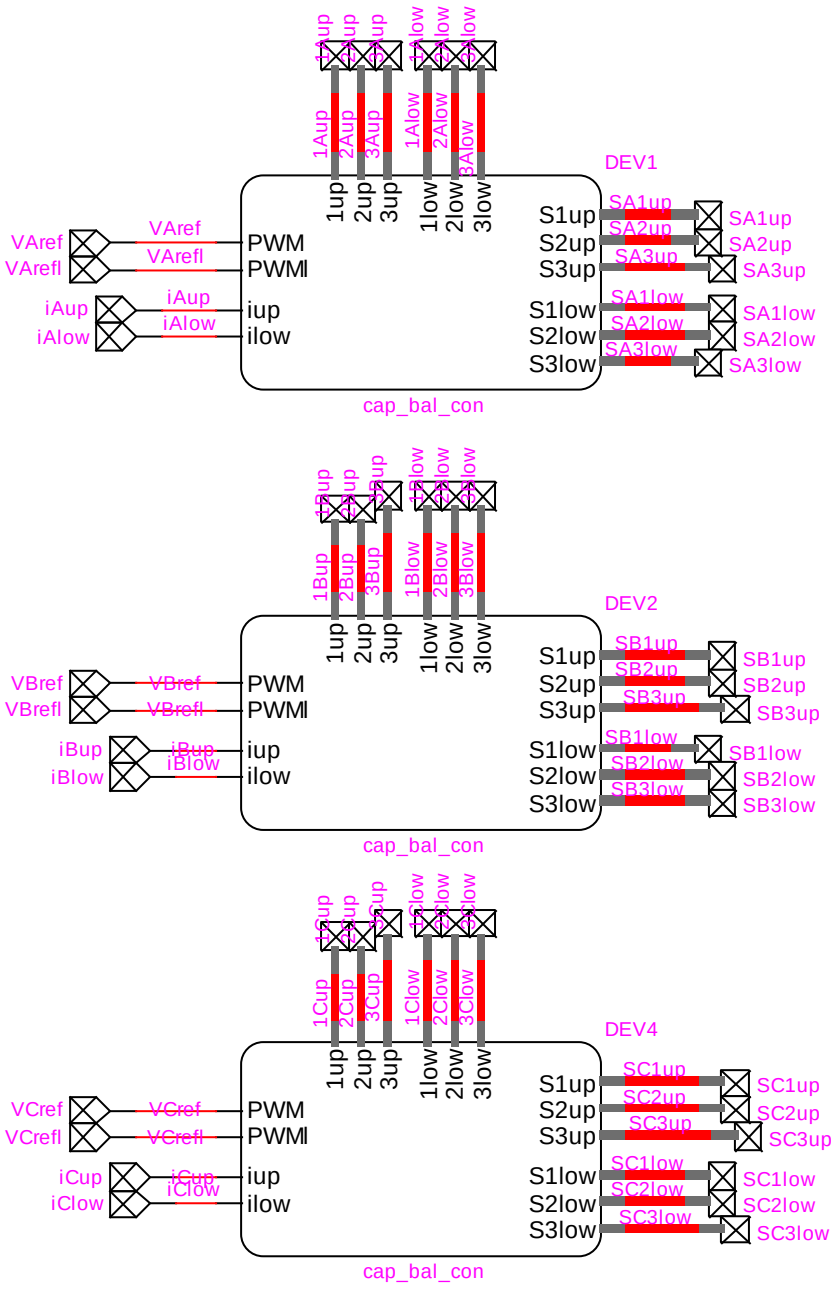
DMM RECTIFIER CONTROL

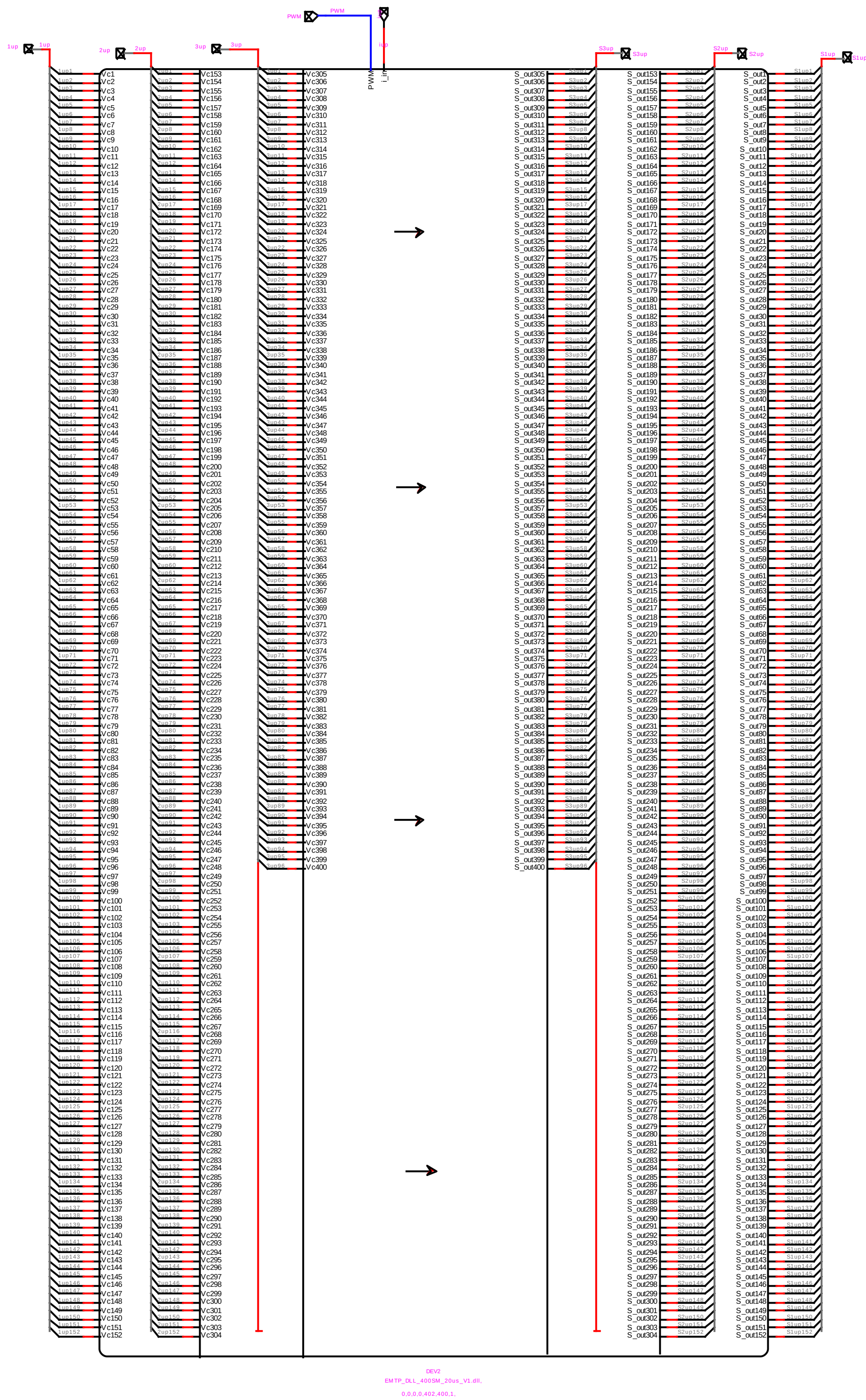


DMM INVERTER CONTROL

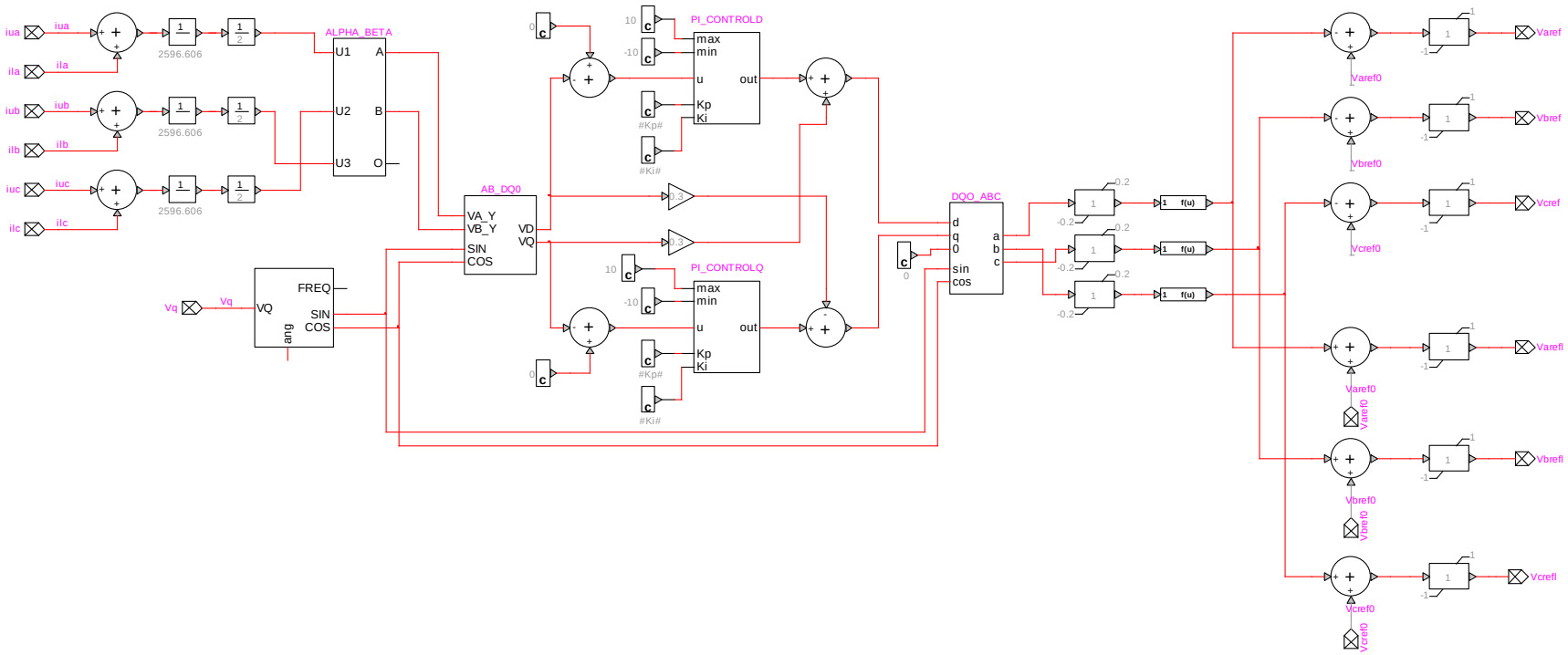


DMM BCA CONTROL





DMM CCSC CONTROL



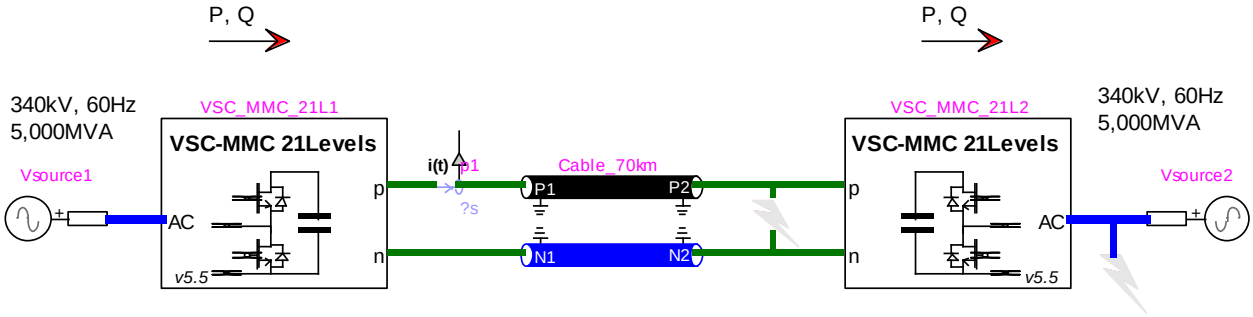
APPENDIX E TEST CASE 4 DATA AND EMTP-RV MODELS DESIGN

i. System Data

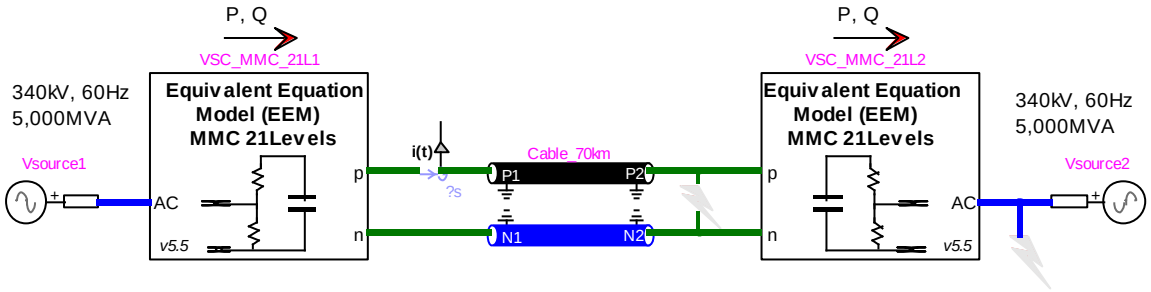
Parameters Rectifier	**Unit**	**Value**		**Parameters Inverter**	**Unit**	**Value**
Short-circuit Level	MVA	5,000		Short-circuit Level	MVA	5,000
AC voltage	kV	340		AC voltage	kV	340
Frequency	Hz	60		Frequency	Hz	60
Transformer Voltage (Prim/Sec)	kV	340/200		Transformer Voltage (Prim/Sec)	kV	340/200
Transformer capacity	MVA	500		Transformer capacity	MVA	500
Transformer impedance	%	18		Transformer impedance	%	18
Filter Size	MVAr	N/A		Filter Size	MVAr	N/A
Series reactance	%	15		Series reactance	%	15
SM capacitors	mF	0.833		SM capacitors	mF	0.833
DC Cable: Same configuration and cable model as Test Case 2						
DC Voltage	kV dc	±320				
Cable Length	km	2x70				

ii. EMTP-RV Design: DMM and STM Models

DMM MODEL – 21 LEVEL MMC

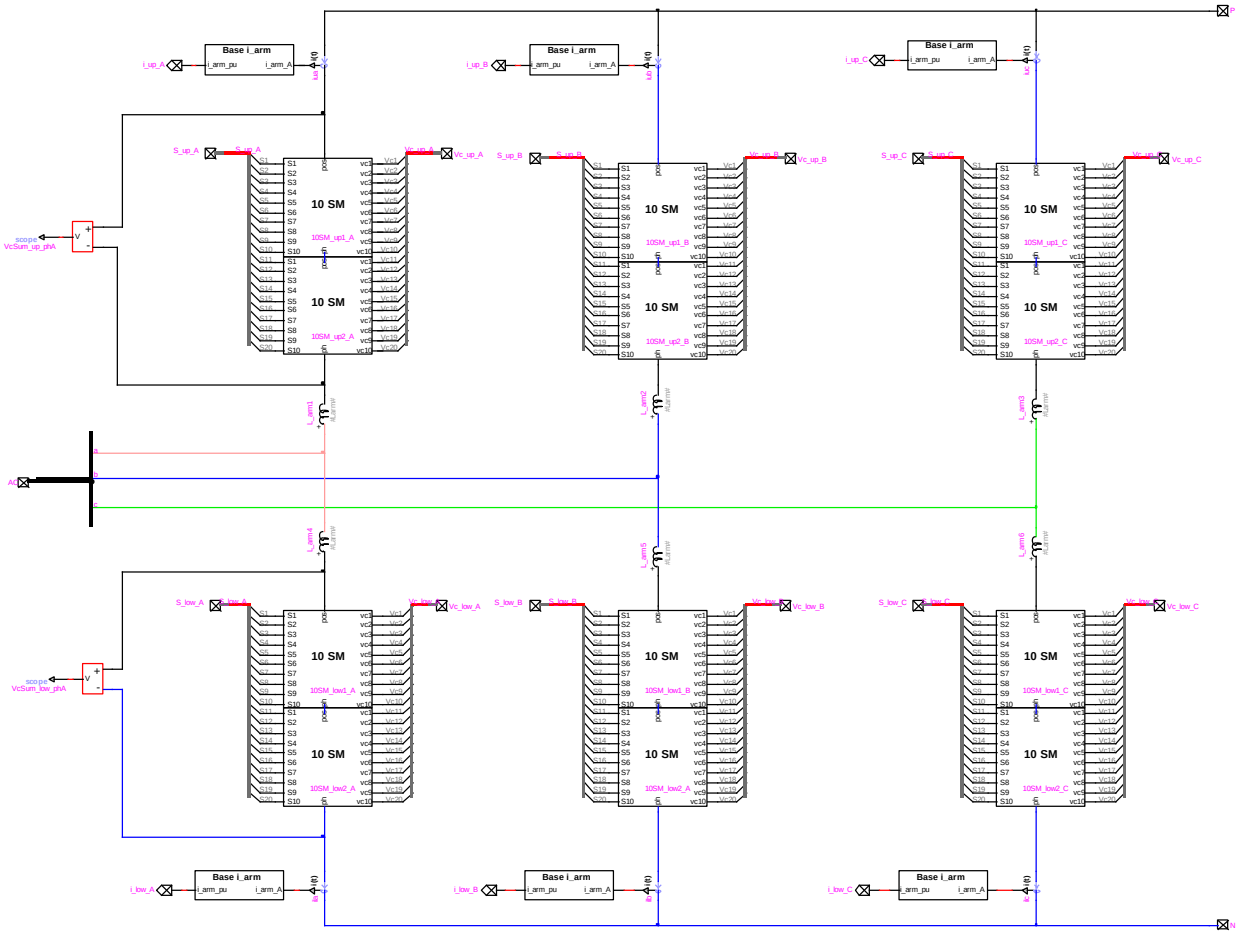


STM MODEL – 21 LEVEL MMC

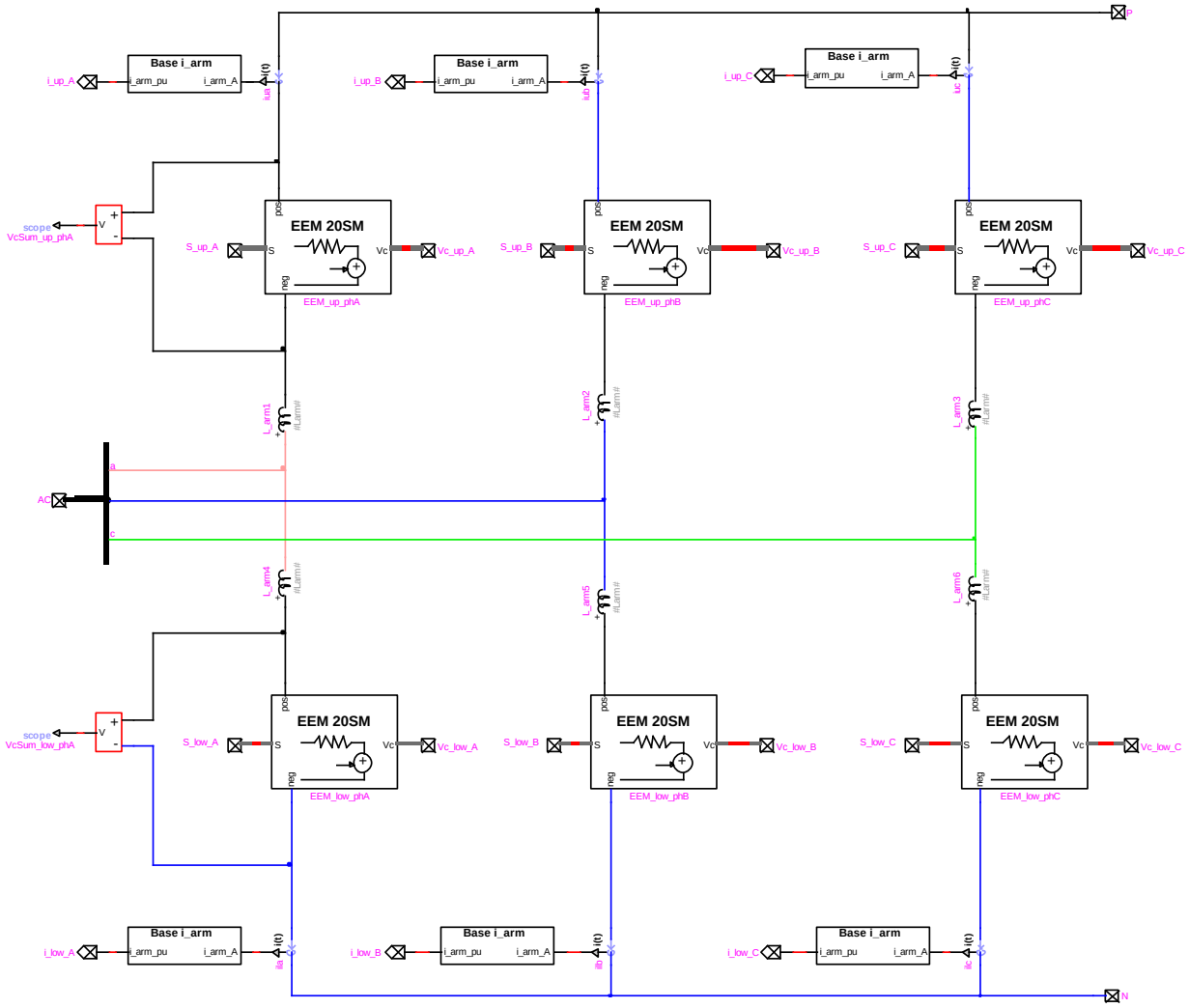


iii. EMTP-RV Converter – DMM and STM Models

DMM CONVERTER MODEL



STM CONVERTER MODEL



STM CONVERTER – CONTROL OF EQUIVALENT THEVENIN CIRCUIT