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CHARGE PUMPS FOR IMPLANTABLE MICROSTIMULATORS IN LOW AND HIGH-VOLTAGE TECHNOLOGIES

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Ce mémoire intitulé:

CHARGE PUMPS FOR IMPLANTABLE MICROSTIMULATORS IN LOW AND HIGH-VOLTAGE TECHNOLOGIES

présenté par: KAR Goutam Chandra
en vue de l'obtention du diplôme de: Maîtrise ès sciences appliquées
a été dûment accepté par le jury d'examen constitué de:

M. AUDET Yves, Ph.D., président
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RÉSUMÉ

L'objectif principal de cette thèse est de concevoir et mettre en œuvre une pompe de charge qui peut produire suffisamment de tension afin de l'implémenter à un système de prothèse visuelle, conçue par le laboratoire PolyStim neurotechnologies. Il a été constaté que l'une des parties les plus consommatrices d'énergie de l'ensemble du système de prothèse visuelle est la pompe de charge. En raison de la nature variable du tissu nerveux et de l'interface d'électrode, la tension nécessaire par stimuler le tissu nerveux est très élevé et consomme extrêmement d'énergie. En outre, afin de fournir du courant biphasique aux électrodes il faut produire des tensions positives et négatives. La génération de tension négative est très difficile, surtout dans les technologies à faible tension compte tenu des limites de la technologie. Le premier objectif du projet est de générer la haute tension nécessaire qui va consommer une faible puissance statique. La technologie de haute tension a été utilisée dans le but d'atteindre cet objectif. Le deuxième objectif est de générer la tension requise dans la technologie de basse tension et ainsi surmonter les limites de la technologie. Dans les deux cas, une attention particulière a été portée afin que personne ne latch-up apparaît pour le cycle négatif.

L'architecture de la conception proposée a été présentée dans cette thèse. La pompe de charge a été conçu et mis en oeuvre à la fois dans la technologie CMOS 0,8 µm offert par TELEDYNE DALSA et technologie 0,13 µm CMOS offert par IBM. En raison de la tension requise, 0,8 µm technologie a été utilisée pour atteindre la sortie et conçu pour minimiser la consommation de puissance statique. La même architecture a été mise en oeuvre en technologie 0,13 µm pour enquêter sur la tension de sortie obtenue avec une faible consommation électrique.

Les deux puces ont été testées en laboratoire PolyStim. Les résultats testés ont montré une variation moyenne très faible de déviation inférieure à 5% par rapport au résultat de simulation. Pour la conception en 0,8 µm, nous avons été en mesure d'obtenir plus de 25 V avec une consommation électrique très faible d'énergie statique de 3,846 mW et une charge d'entraînement maximum de 2 mA avec un maximum d'efficacité de 84,2%. Pour le même processus en 0,13 µm, les resultats ont été plus que 20V, 0,913 mW, 500 µA, et 85,2% respectivement.

ABSTRACT

The main objective of the thesis is to design and implement a charge pump that can produce enough voltage required to be implemented to the visual prosthesis system, designed by the PolyStim Neurotechnologies laboratory. It has been found that one of the most power consuming parts of the whole visual prosthesis system is the charge pump. Due to the variable nature of the nerve tissue and electrode interface, the required voltage of stimulating the nerve tissue is very high and thus extremely power consuming. Also, in order to provide biphasic current to the electrodes, there is a requirement of generating both positive and negative voltages. Generating negative voltage is very hard especially in low voltage technologies considering the technology limitations. The first objective of the project is to generate required high voltage that will consume low static power. High voltage technology has been used to achieve the goal. The second objective is to generate the required voltage in low voltage technology overcoming the technology limitations. In both cases, special care has been taken so that no latch-up occurs for the negative cycle.

Architecture of the proposed design has been presented in this thesis. The charge pump has been designed and implemented in both 0.8 µm CMOS technology offered by TELEDYNE DALSA and 0.13 µm CMOS technology offered by IBM. Because of the required voltage, 0.8 µm technology has been used to achieve the output and designed to minimize the static power consumption. The same architecture has been implemented in 0.13 µm technology to investigate the achievable output voltage with low power consumption.

Both the chips have been tested in polyStim laboratory. The tested results have shown very low variation of less than 5% average deflection from the simulation output. For the design in 0.8 µm, we have been able to get more than 25 V output with very low static power consumption of 3.846 mW and maximum drive load of 2 mA with maximum efficiency of 84.2%. For the same design in 0.13 µm, the outputs were more than 20V, 0.913 mW, 500 µA, and 85.2% respectively.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS AND SYMBOL

ATP	Adenosine Triphosphate
BJT	Bipolar Junction Transistor
LGN	Lateral geniculate nucleus
CMOS	Complementary Metal Oxyde Semiconductor
RCP	Reduced concentration of Products
DC	Direct Current
FPGA	Field-Programmable Gate Array
IC	Integrated Circuit
MOSFET	Metal Oxyde Semiconductor Field Effect Transistor
OMS	Organisation Mondiale de la Santé

n	Slope factor
V_t	Thermal voltage
V_A	Early voltage
V_{th}	Threshold voltage of MOS transistor

INTRODUCTION

Biomedical engineering has shown a great prospect in recent past to restore physiological functions. Research in the field of biomedical engineering has experienced remarkable growth in recent decades. This excitement is particularly noticeable in the case of implantable medical devices. Following the technical and commercial success of the pacemaker and the cochlear implant, the pacemakers become commonly considered an avenue to restore physiological functions lost. This trend is supported by the miniaturization of microelectronics circuits to integrate to systems of increasing complexity surfaces on the order of mm^2.

Blindness is a typical example of a physiological disorder that much interest in the scientific community for a long time. In April 2010, approximately 39 million blind people worldwide have been identified (World Health Organization [WHO], 2010). According to the organization, 25% of this blindness cannot be prevented or treated in normal way. To be able to handle other cases considered irreversible, many researchers are studying the development of electronic prostheses enable patients to regain functional vision. It is in this context, the PolyStim neurotechnology laboratory at the École Polytechnique Montreal has initiated the project Cortivision, a visual implant directly stimulating the visual cortex. The latest advances in this project show a working prototype successfully used in experiments in vivo in rats (Coulombe, 2007).

An important constraint for any implantable device is power consumption. In the case of Cortivision, the implant is powered by an external battery whose power is transmitted by a wireless inductive link. The system being used on a daily basis due to several hours per day, it is crucial to limit power consumption to extend battery energy of the implant. A second design constraint of the intracortical microstimulator is the high impedance of the interface between the electrode and the biological tissue. This requires the use of high voltages often incompatible with processes low voltage.

The main objective of this research project is the realization of a intracortical microstimulator with reduced power consumption compared to the previous prototype (Coulombe, 2007, S. Ethier, 2011). To achieve this, new forms of potentially more effective stimuli are generated and can be compared to the basic design. The idea is to generate a charge pump which can produce enough voltage to provide the required supply. Because producing high voltage supply results in consuming very high power, considerable reduction of the power consumption is required by the circuitry as a total of more than 1000 channels is considered. The resulting prototype will experimentally validate the results obtained using the model developed by cortical Polystim (Robillard, 2008). Another objective of this work is to reproduce the whole design in low voltage technology to produce the highest amount of output voltage. The limitations of low voltage technology make it more difficult to produce enough supply voltage but it is necessary to integrate the whole system in a single chip also to reduce power consumption. This circuit is essential for the prototyping of a fully implantable system including no discrete component.

This master thesis consists of five chapters. The first chapter summarizes the basic concepts of physiology that are necessary for the identification of system specifications. It is about the first neuron, the basic unit of the nervous system and its excitation process. Second, the human visual system is briefly described with an emphasis on the visual cortex. Thirdly, it is a question of the interface formed between the electrodes and tissues, as well as its model. Finally, the basic principles of functional electrical stimulation are described.

The second chapter is devoted to a review of the literature. First, an overview presenting the various existing visual implants and their characteristics is performed. Subsequently, a review of various circuits useful for this project is presented. These circuits involve the generation of various forms of pulses used for stimulation and the generation of high voltages.

As of third chapter, the full design and description of the low-power high voltage charge pump has been described. Both simulation and experimental results have been discussed. Then a comparison of different work has been presented.

A general discussion by linking different parts of the memory is performed in the fourth chapter. Further discussions with defective circuits manufactured and not present in the article are also found.

Finally, the conclusion summarizes all the work done in this thesis and recalls the important results. Recommendations based on results which relate to the project's next steps Cortivision are also mentioned.

CHAPTER 1

FUNDAMENTAL CONCEPT ON ELECTROPHYSIOLOGY

First, it is important to recall some concepts of neuron physiology and bioelectricity necessary for understanding the phenomena and systems forming the heart of this thesis. This first chapter includes these key concepts by starting with the neuron and its principle of excitement. Subsequently, the entire visual system is described, particularly the primary visual cortex. Then, types of stimulation electrodes and how they form interface with living tissue are described. Finally, there is the question of functional electrical stimulation, its parameters, as well as notions of security.

1.1 The neuron

The neuron is the basic element of the nervous system. This cell allows the generation and propagation of nerve spikes in the body. Figure 1.1 illustrates the anatomy of a typical neuron.

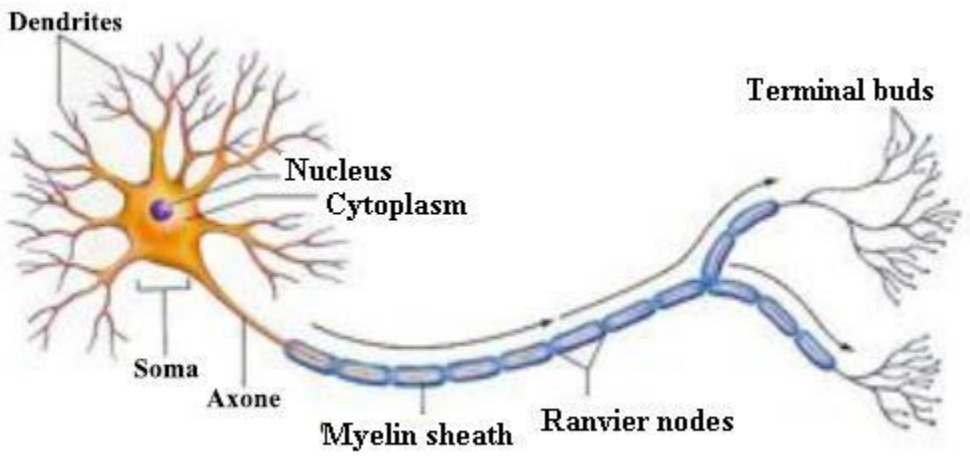


Figure 1.1: Physiology of the neuron. Modified from (StateMaster, 2009).

The dendrites are considered as inputs of the neuron. These capture the stimuli from cells cyclic up. At the other end, the terminal buds are outputs to transmit nerve spikes to other neurons. The connection between two neurons, called the synapse is not direct. It is rather a narrow space in

which biochemical travel are called neurotransmitters. These are released by the terminal buttons of a neuron transmitter to the arrival of nerve spikes and are picked up by the dendrites of the receiving neuron. The uptake of neurotransmitters regenerates nerve spikes that converge towards the center of the receptor neuron, that is to say the soma. Treatment of all signals received by the dendrites is then carried out according to the type of neuron. The response of the soma is then propagated along the axon. Myelin sheath, consisting of Schwann cells wrapped, wraps the axon of a neuron. Some sections of the axon are not covered; they are called nodes of Ranvier. This structure aims to accelerate the propagation of spikes along the axon can be over a meter long, depending on the type of neuron.

1.1.1 The cytoplasmic membrane

The cell membrane of the neuron plays a fundamental role in the generation and propagation of nerve spikes. As for all cells in the body, it is composed of a double layer of phospholipids, low permeability layer molecules and ions. However, it is traversed by proteins that act as channels and as ion pumps. These proteins facilitate the dissemination and allow the selective transport of ions between the intracellular and extracellular environments, ensuring self-regulation of the cell. Major ions involved in bioelectric phenomena are Na^+, Cl^-, K^+ and Ca^{2+}. At equilibrium, the extracellular medium typically has a higher concentration of sodium ions and chlorine, while the intracellular medium has a higher concentration of potassium ions.

The concentrations of various ions in the intracellular and extracellular environments are such that there is a difference in electric potential between sides of the cytoplasmic membrane. This trans-membrane potential is conventionally defined as the neuron potential, normally is about -70 mV. It is the resting potential, also known as the equilibrium potential or rest of the cell. Membrane voltage is at the heart of bioelectric phenomena of the cell. For example, ion channels have a number of gates of that state, that is to say, open or closed, depending on what the potential is.

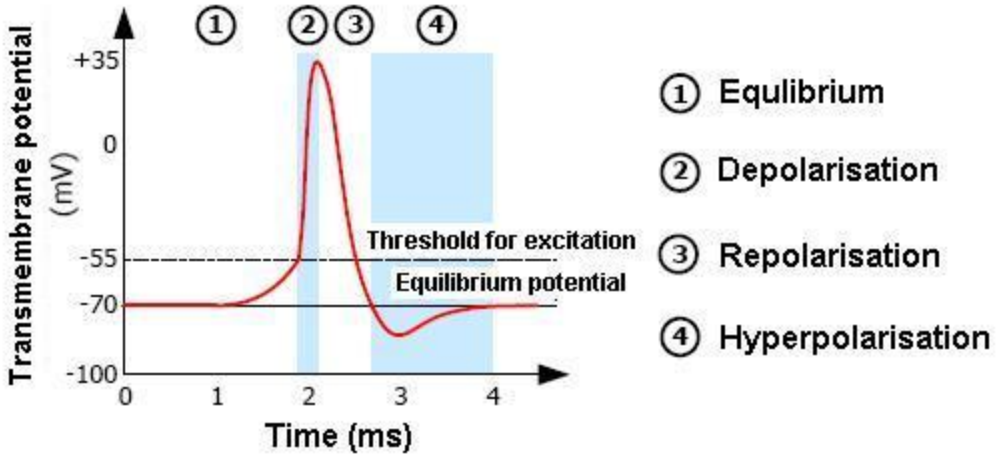
This allows them to distribute the ions through the membrane or block. These are the mechanisms for opening and closing different gates that allow the generation of action potentials.

1.1.2 The action potential

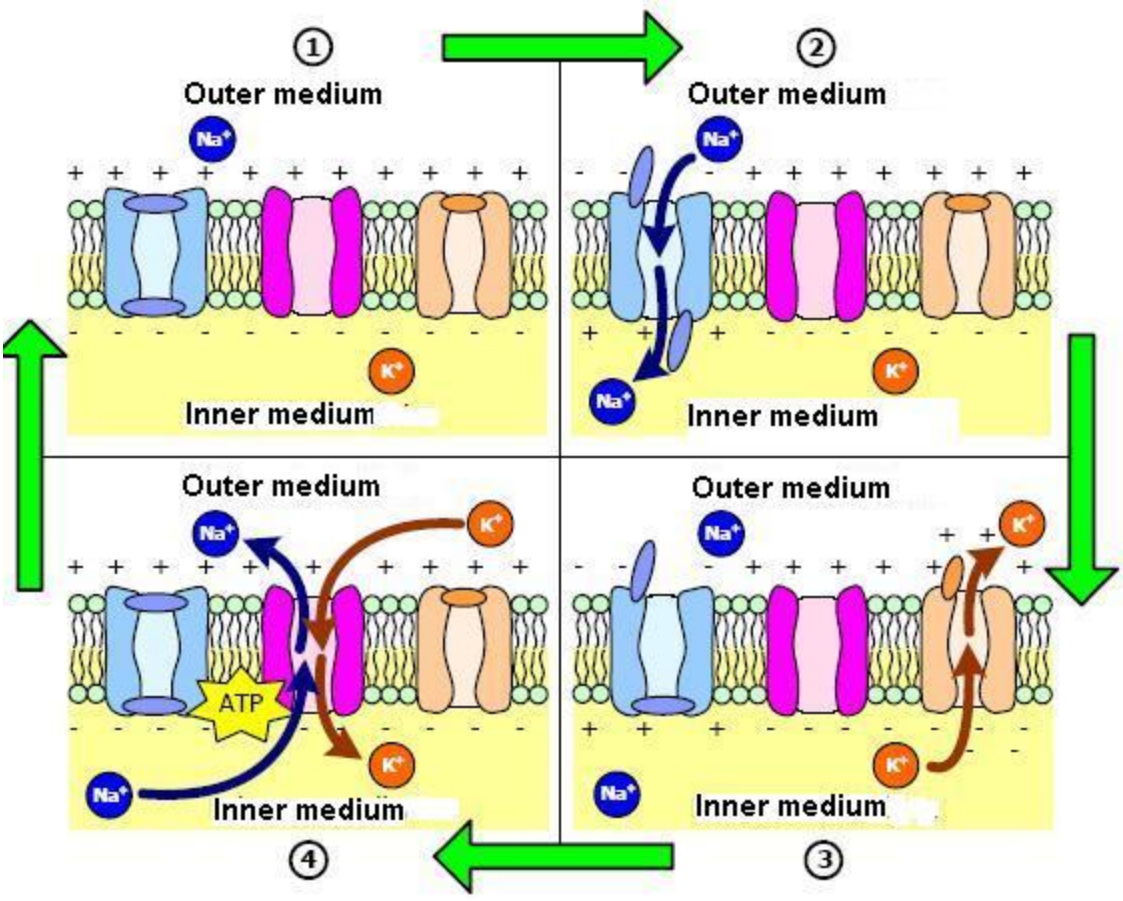
Several phenomena can disrupt the electrical balance of the neuron. In the case of sensory neurons, the physical changes of the environment, such as temperature, pressure or light, have a direct effect on the internal potential. Another possible disruption is receiving a nerve impulse from a neighboring neuron. The last case is a local variation of extracellular potential generated by an external electrical stimulation, for example.

These disturbances of balance electrochemical cell change its transmembrane voltage. If this is kept under the excitation threshold of the neuron (about -55 mV), the mechanisms of diffusion and ion transport restore balance and no excitation is generated. On the other hand, when the membrane potential exceeds this threshold, spike is triggered. This is the action potential. The latter is generated by a mechanism of the type "all or nothing", that is to say that the amplitude and duration of the action potential are independent of the intensity of the stimulus to its origin.

The phenomenon is illustrated briefly in Figure 1.2. First, in step 1, the neuron is in balance and membrane potential of -70 mV. A stimulus is thereafter increased to the threshold potential internal excitation of the cell. From that moment there is local depolarization of the membrane of the neuron, which corresponds to step 2 in Figure 1.2. This is a sharp increase in the transmembrane voltage caused by the massive influx of Na^+ ions inside the cell as a result of the opening of the gates of sodium channels. When the action potential reaches its maximum value of about 35 mV, repolarization phenomenon is switched on. So one of the gates of the sodium channels closes, and the door opens potassium channels, allowing a major outflow of K^+ ions to the extracellular medium. The result is a decrease in membrane potential, as is shown in step 3, resulting in hyperpolarization of the cell membrane. This means that the membrane potential falls below its equilibrium value. At this time, or in step 4, it pumps Na^+ - K^+ exchange of Na^+ (outward) and K^+ (inward) to rebalance the internal potential of the neuron. These transfers occurring ions against the electrochemical gradient diffusion pumps, expend energy provided by adenosine triphosphate (ATP) to achieve them.



(a)



(b)

Figure 1.2: Trigger mechanism of an action potential. (a) Temporal variation of the membrane potential. (b) Illustrates the mechanism of ion channels in the membrane (StateMaster, 2009).

The action potential amplitude with fixed stimulus intensity to its origin is rather modulated by the firing frequency of action potentials of the neuron. This frequency, known as firing frequency, has a limit. Immediately after the onset of an action potential, there is a period during which the membrane is insensitive to extracellular potential, thus preventing the generation of a second action potential. This period, due to the hyperpolarization of the membrane, is called refractory period.

1.1.3 Propagation of an action potential

Once triggered, the spike must be transmitted through the nervous system to be interpreted. The propagation of the action potential along the axon is explained by the theory of the cable (Gulrajani,1998), the phenomenon is shown schematically in Figure 1.3. Briefly, the intracellular and extracellular environments are considered drivers of ionic current. When action potential is triggered at a point A of the membrane, the membrane potential is changed here. The potential difference between point A and point B then generate intracellular and extracellular ionic currents from A to B during depolarization. These currents depolarize the membrane B, and if they reach the threshold of excitability, trigger another action potential at this point. This phenomenon is repeated from B to C and so on throughout the axon, it is a chain reaction conservative.

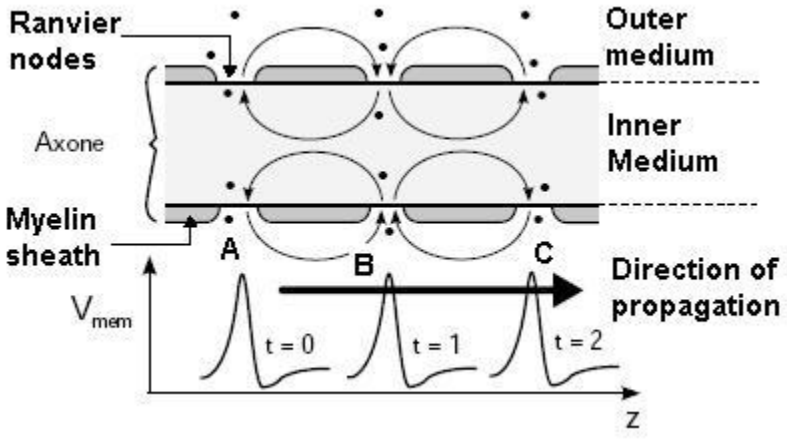


Figure 1.3: Propagation of an action potential along an axon militated neuron(StateMaster, 2009).

When the axon is militated, the myelin sheaths prevent any passage of ions through certain sections of the cell membrane. Regions of the membrane where action potentials can be generated are then discretized by nodes of Ranvier as shown in Figure 1.3. The distance between nodes causes the triggering of an action potential at a point allows the direct excitation of the next node without being slowed down by its own refractory period. This type of propagation, called salutatory conduction, then takes place more rapidly in the absence of myelin.

Notions concerning the action potential are introduced; the next section deals with the human visual system, especially the primary visual cortex, which represents an area of interest in this work.

1.2 Visual system

The visual system in humans is critical and complex. It mainly extends in the retina to the visual cortex located in the back of the brain. Several other cortical areas are solicited for more cognitive processing, but they will not be considered here. Figure 1.4 shows the anatomy of this system and the path that the information captured by the eye.

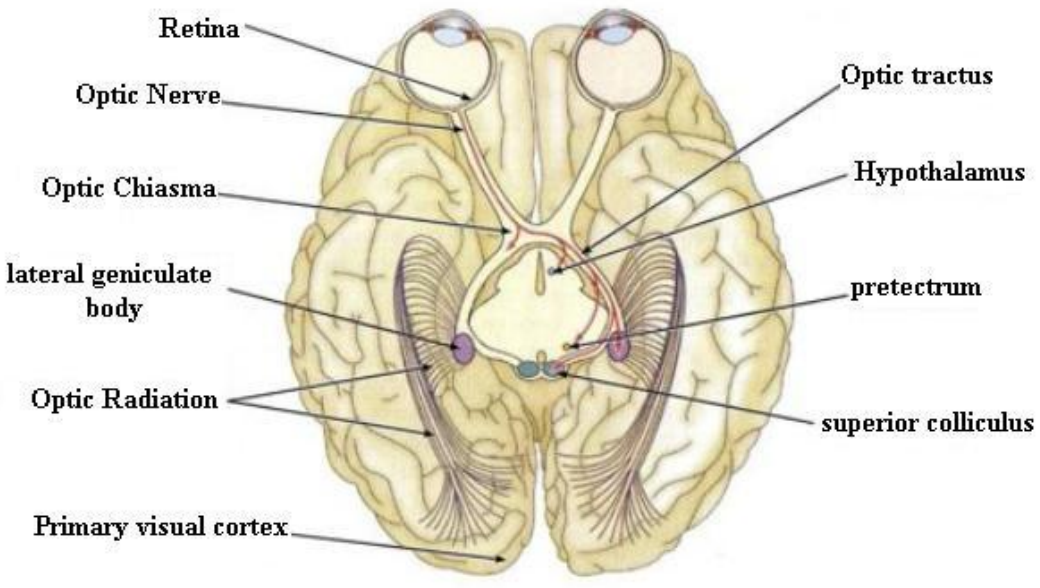


Figure 1.4: Anatomy of the human visual system. Modified from (Coulombe, 2007).

The light is first converted into nerve spikes by the retina at the back of each eye. They are composed of three layers of neurons with specific functions, are the photoreceptors, bipolar neurons and ganglion cells. Already at the retina, the visual information processing is performed. The axons of the ganglion cells meet at a point on the retina, called optical disc to form the optic nerve. It enters the skull and travels the optic chiasm, where there is partial crossing of axons and the optic tract. Each of these points has a role in the treatment of nerve spikes. Axons then reach the lateral geniculate nucleus (LGN), one relay before the primary visual cortex. The LGN is composed of six distinct layers of cells, each receiving a particular projection from the retina. Up to this point, the propagation and processing of signals generated by the retina are performed in parallel. In addition, it should be noted that about 80% of excitatory connections, from the LGN to the primary visual cortex, it performs so important feedback on the treatment at the LGN. Finally, the information is transmitted to the primary visual cortex through projections called optical radiation.

1.2.1 Primary visual cortex

The visual cortex consists of several dozen areas performing simple treatments, such as the analysis of orientation and color, or treatments such as cognitive and associative recognition of objects or spatial positioning. Only the primary visual cortex, also known as striate cortex or V1, is considered in this work since it is the entry point for more complex processing of visual information.

From a total thickness of 2 mm, the primary visual cortex is located in the posterior occipital lobe. It contains many types of neurons, mainly pyramidal cells and stellate. This area of the cortex is divided into six distinct layers, each having a composition and functions. By studying the neuronal connections between these layers and between different areas, it has been shown that the signals come from the LGN in the visual cortex by layer 4 of area V1. This layer, especially the sub-layer 4C, plays a role in the progression and treatment of information in vision. Subsequently, the information is projected to layers 2, 3 and 5, in addition to feedback to

the LGN. These layers retransmit the signals received from the layer 4 surrounding areas for more advanced treatment.

In this arrangement adds layers of primary visual cortex organization in columns, as shown in Figure 1.5. Initially, the layer 4C is divided evenly in the ocular dominance columns by alternating bands of about 0.5 mm wide. In a second step, the columns are spread orientation in the direction orthogonal to that of the dominant eye. For each of these columns in the cortex, electrical activity is dependent on a fixed orientation of the light stimulation. It has been shown experimentally that 180^{o} are covered by 1 mm on average. Finally, the last column elements are stains. These cylindrical pillars collect and process information about color. In Figure 1.5a, is schematized cortical module, that is to say, a block of 2 mm × 2 mm with two complete groups of ocular dominance twice orientation of 180^{o} and 16 spots. As a summary, Figure 1.5b represents a column detailed V1 cortex on which the various layers and the signal inputs are identified. Inputs from magnocellular and parvocellular layers respectively are 1 and 2, and 3 to 6 of LGN. They are different type of retinal ganglion cells which are projected.

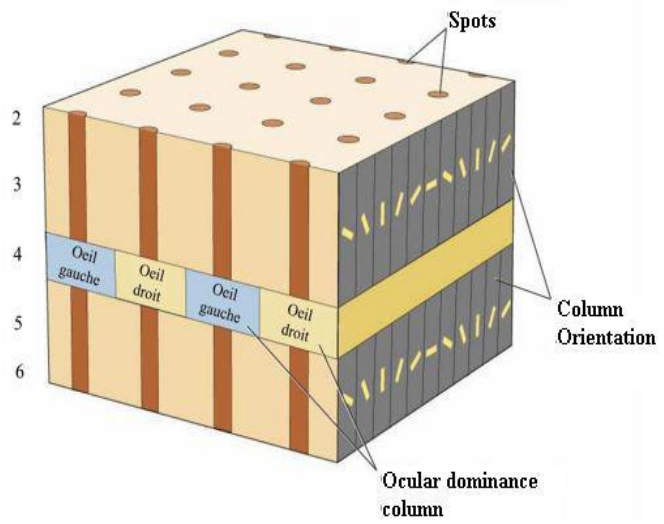


Figure 1.5: Organization of the primary visual cortex (Cortical module) (McGill University, 2009).

1.3 Stimulation electrodes

In the biomedical field, the electrodes are essential for both signal acquisition and biological tissue stimulation. They have a function of transducer for converting the electrical current in the ion current, and vice versa. This conversion is done using the complex electrochemical reactions occurring at the electrode-tissue interface. The impedance of this interface is non-linear and depends on several factors such as stimulus measure/inject (intensity, frequency), the electrode (material, geometry, surface) and the environment (temperature, ion concentrations).

1.3.1 Reactions of the electrode-electrolyte interface

Contact between an electrode and biological tissue is summarized by an electrochemical phenomenon between a metal and an electrolyte (Merrill et al., 2005). The cell medium is considered electrolyte containing ions Na^+, Cl^- and K^-. Once the electrode is working, an interface consisting of a double layer of charge is formed at its surface. This is the result of redistribution of loads in both environments, the adsorption of some anions and attraction of polarized molecules such as water molecules. The equilibrium is reached.

When a current is injected from the electrode, as in the case of stimulation, the amount of charge at the interface is changed and the balance is disturbed. Two types of charge transfer between the metal and the electrolyte can then occur depending on the number of injected charges. When this amount is low, the charge transfer is said capacitive or non-faradaic that is to say that no electron passes through the interface. The result is a redistribution of charges in the electrolyte. This phenomenon is reversible by removing the same amount of charge of the electrode. When the disturbance of the balance is too high, a second type of charge transfer occurs or injection faradic charges. In this case, electrons are injected into the electrolyte causing oxidation-reduction reactions at the interface whose general form is given by equation (1.1)

$$O + ne^- \leftrightarrow R \qquad (1.1)$$

Where O is oxidized species, the reduced species R and n are the number of electrons transferred. Depending on various factors such as the material and the electrode surface, and the intensity and duration of stimulation, ions toxic to tissues can be produced and released into the cell medium. These reactions are all reversible. According to their speed of reaction, it is possible that harmful products are distributed far from the electrode to a reverse flow of charges can be recovered.

1.3.2 Interface Model

A model of the electrode-tissue interface considering the different charge transfer is an essential tool for the design of a pacemaker. Indeed, an electrical point of view, it is crucial to have a good knowledge of the output load circuit, that is to say, the impedance of the contact. Many researchers have focused on the modeling of the interface giving rise to models more refined (Laaziri, 2005). Recently, Laaziri proposed a more realistic model as shown in Figure 1.6.

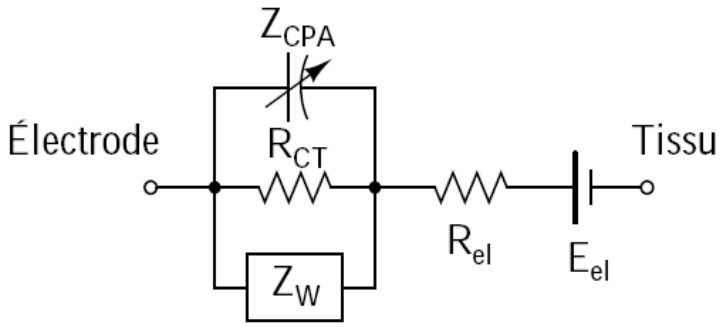


Figure 1.6: Electrode-tissue interface model ((Laaziri, 2005)

Here is a brief description of the component. First, Z_{CPA} is the impedance of the capacity corresponding to the C_{dl} ionic double layer formed at the surface of the electrode. This capability models the charge transfer non-faradaic. The amplitude of the impedance depends on the stimulus and the material of the electrode. Then R_{CT} represents the resistance of faradaic charge transfer between the electrode and the tissue of the stimulation current. The impedance Z_W, called the Warburg impedance, modeled the effect of ion diffusion around the electrode. This impedance is dependent on the stimulus highly complex, and the surface of the electrode and ion

concentration of the cell medium. Finally, resistance R_{el} and the voltage source E_{el} correspond to the resistance of the extracellular medium and the equilibrium potential of the interface between the electrode and tissue.

1.3.3 Types of Electrodes

Depending on the application and the location of the body where they are used, the electrodes can take different forms. Figure 1.7 shows some examples of implantable electrodes. Insulated electrodes, or electrodes cuff, are useful for the stimulation of the peripheral nerves since they allow direct contact with them. For the acquisition of signals or tissue stimulation, surface electrodes are commonly used. Finally, with its pointed, the microelectrode penetrates tissue with stimulation directly to a given depth. Grouped into matrices, the microelectrodes can provide a high density, which is desirable for intracortical stimulation.

For its part, the implant project of Cortivision has been done using microelectrode array. Only the tips are exposed to about 100 microns, the surface of contact with the cortical tissue is reduced. Therefore, the impedance of the electrode-tissue interface is high. According to measurements made by Pigeon, it can reach approximately 100 kΩ for low-frequency stimulation (Pigeon, 2004).

1.4 Principle of electrical stimulation

As mentioned above, action potentials can be triggered in excitable tissues, such as the cortex, artificially with electrical stimulation through an electrode. To be effective, the stimulus must succeed in raising the transmembrane voltage above the threshold for triggering an action potential.

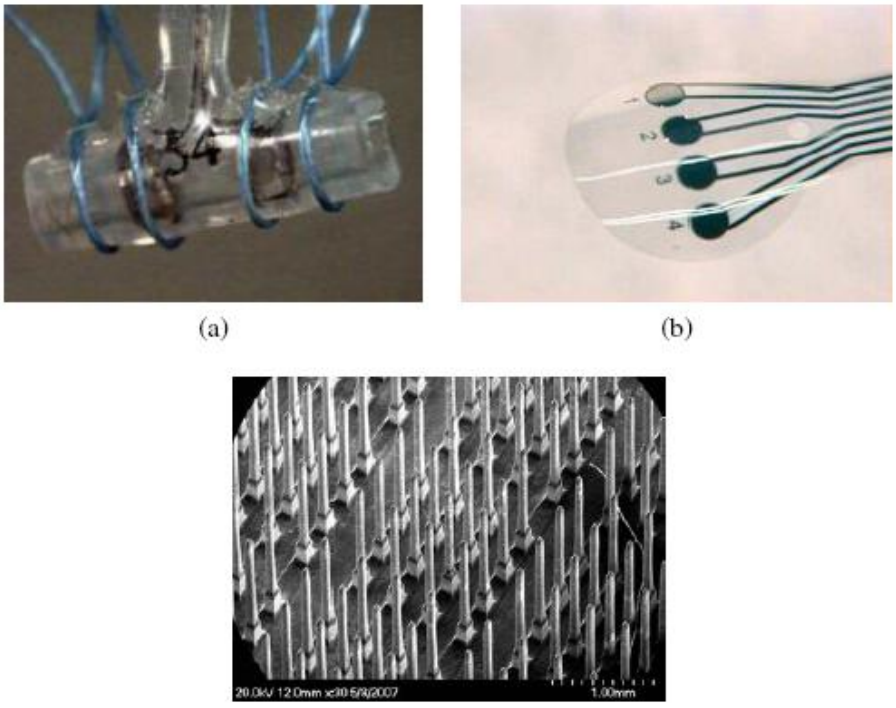


Figure 1.7: Different examples of implantable electrodes. (a) Electrode sheath. From (Cramp, 1999). (b) Surface electrodes. From (Rodger et al., 2006). (c) Matrix microelectrodes. From (Ayoub, 2007).

1.4.1 Parameters

In general, the stimuli used are rectangular biphasic pulses of current. Tissue response to these stimuli has been characterized and is shown in Figure 1.9. This is the time-intensity curve showing the threshold current density and duration of a pulse which triggers action potentials in tissue. This threshold I_{th} follows the following equation:

$$I_{th} = \frac{I_0}{1-e^{\Delta t/T}} \qquad (1.2)$$

Where ΔT is the pulse duration, current I_0 is the base current or the current absolute minimum needed to excite neurons, and τ is the minimum time to allow current to reach $2I_0$ which is the excitation threshold current.

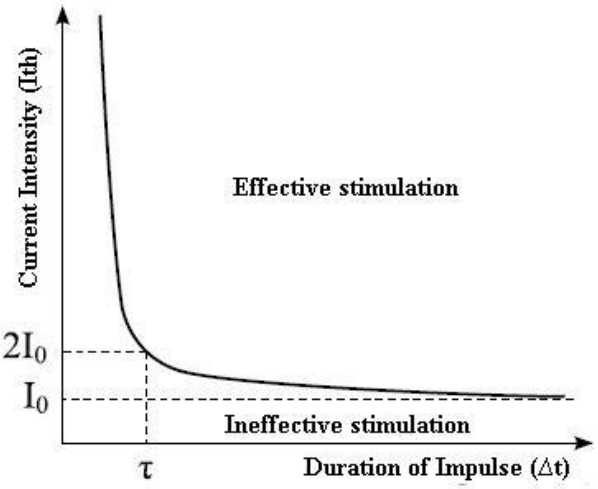


Figure 1.8: Intensity-duration curve defining the excitation threshold of the neuron (Merrill et al., 2005).

To ensure the effectiveness of the stimulation, it is generally composed of several biphasic pulses repeated at a given frequency, as shown in Figure 1.10. These pulses are also grouped into trains, repeated themselves at a given rate. To maximize the effectiveness of the stimulator, it is advantageous for all stimulation parameters of Figure 1.10 to be variable. Indeed, the effect of each of these parameters is not fully known and may vary from one person to another, it is essential that the microstimulator be as flexible as possible.

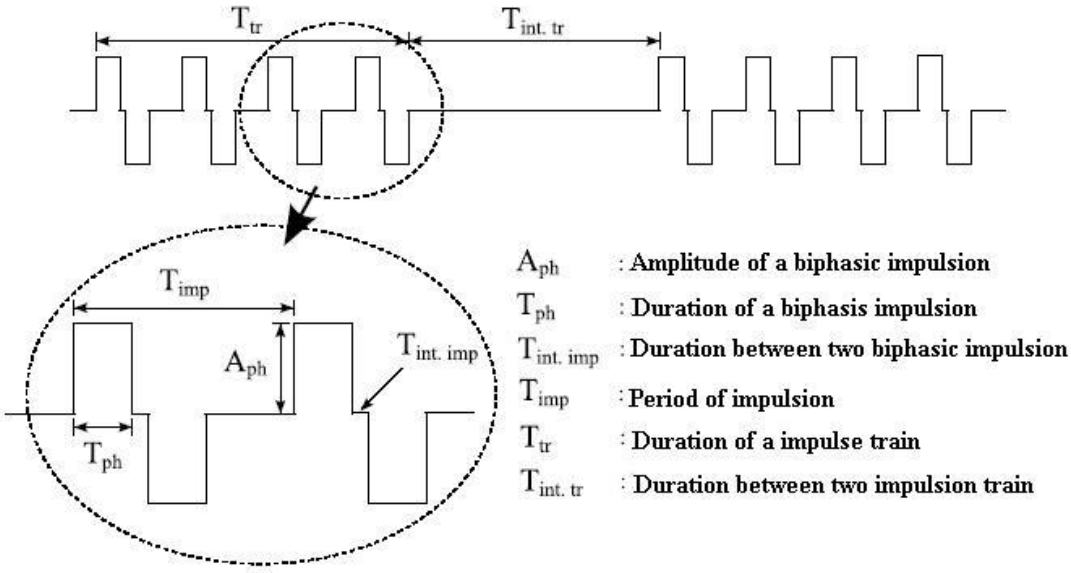


Figure 1.9: Biphasic pulse train of current with the set of parameters of stimulation (Merrill et al., 2005).

Different modes of stimulation are also possible. Indeed, biphasic pulses may be injected through a single electrode. The return current is then recovered by a reference electrode. It must have a very large contact surface to reduce its impedance and maintain approximately constant potential during stimulation. In this case, the faradaic charge transfer is limited (Merrill et al., 2005). This mode is called monopolar stimulation. Stimulation can also be between two active electrodes. First electrode stimulation current injected while the second completes the circuit by connecting to one of the supply voltages according to the polarity of the pulse. This is called bipolar stimulation.

1.5 Conclusion

Physiological concepts necessary for understanding the main topic of this master thesis were briefly summarized in this first chapter. The initiation and propagation of action potentials and detailed description of the neuron and the cell membrane has been given. Subsequently, the entire visual system was flown with a particular emphasis on the primary visual cortex. Then, as discussed, stimulation through electrodes, the electrochemical reactions at the interface with the tissues of the model and power consumption have been described. Finally, based on these concepts, certain fundamental principles of stimulation were set to ensure patient safety while promoting effectively.

CHAPTER 2

ADVANCED WORK IN THE FIELD

This second chapter aims to present the state of the art in stimulation of the visual system through a review of relevant work leading to this thesis. Electrical stimulation of the visual system is discussed according to the different possible strategies. The emphasis is on intracortical stimulation with a brief history of basic and advanced existing systems, including the implant team of Polystim. We then question the effectiveness of stimulation, as well as some other areas to improve. Then, various implementations of these circuits generating high voltage are inventoried. Finally, the last section discusses the selection of high-voltage circuits designed to be effective for biphasic current pulse generation at the electrodes and various architectures to produce such high-voltage levels.

2.1 Electrical stimulation of the visual system

The various methods of restoring functional vision depend on the site of stimulation in the visual system, which are the retina, the optic nerve and the visual cortex. In all these cases, it is possible to perceive a sensation points light called phosphenes in the visual field of the user. The idea behind any visual prosthesis is to recreate images understandable for the blind from several of these phosphenes.

2.1.1 Stimulation of the retina

A first approach is the visual prosthesis stimulation of the retina. Two types of retinal stimulator are under development: the sub-retinal implant (Shire et al., 2009) and epi-retinal implant (Weiland et al., 2008). First, the sub-retinal prosthesis is implanted under the retina and replaces the deficient photoreceptors by directly stimulating the healthy ganglion cells. It has the

advantage of being held in place by the retina. In the case of epi-retinal implant, the pacemaker is fixed on the surface of the retina and stimulates using surface electrodes.

The main advantage of stimulating the retina is the natural treatment of visual information downstream is involved. Good resolution and image quality can be hoped for. This technique is less invasive than other types of visual prostheses (Normann et al., 1999). However, the blindness of the major diseases of the retina and optic nerve cannot be treated by this method. In addition, in the case of epi-retinal implant, the prosthesis must be firmly established in the retina, which has about 500 microns thick, not to win with saccades of the eye. Finally, the ganglion cells have several roles in the encoding of visual information; it is not clear what is their response was to electrical stimulation (Normann et al., 1999).

2.1.2 Stimulation of the optic nerve

Electrical stimulation of the optic nerve using electrode cuffs provides visual perceptions (Veraart et al., 1998). This avenue is taken to achieve a visual prosthesis for the user to recognize patterns given (Veraart et al., 2003).

This approach is a better way of stimulation of the retina. In addition, compared to other techniques, the number of electrodes required to generate a given number of phosphenes is much lower. However, the control over them is much more complex. The surgery required for implantation is major and invasive. These drawbacks mean that this type of implant is uncommon and has not been successful so far.

2.1.3 Stimulation of the primary visual cortex

A final possible strategy to restore functional vision is the stimulation of the visual cortex. Having its entry point much further downstream in the flow of visual information, this method has the advantage of covering the widest variety of causes of blindness. It is possible to stimulate the surface of the cortex (cortical stimulation) or at a given depth with penetrating electrode (intracortical stimulation). Being attached to the surface of the brain, such an implant is to be

protected by the skull, but it faces from mechanical stresses among others cortex itself. (Normann et al., 1999).

2.1.3.1 History

Since the 1960s, it is known that the local electrical stimulation of the visual cortex gives rise to phosphenes. Based on this, the idea of a visual prosthesis for reading and facilitating travel for the Blind has fascinated many research teams, including Brindley and Dobelle (Brindley & Lewin, 1968; Mladejovsky & Dobelle, 1974). Their groundbreaking work, considered the genesis of this research, as a first characterization of the appearance of phosphenes by the stimulation parameters and the location of the electrodes on the occipital lobe. They also raised awareness of the major limitations of this approach, as the threshold current required for the generation of phosphenes (of the order of mA) and look diffuse and difficult to control.

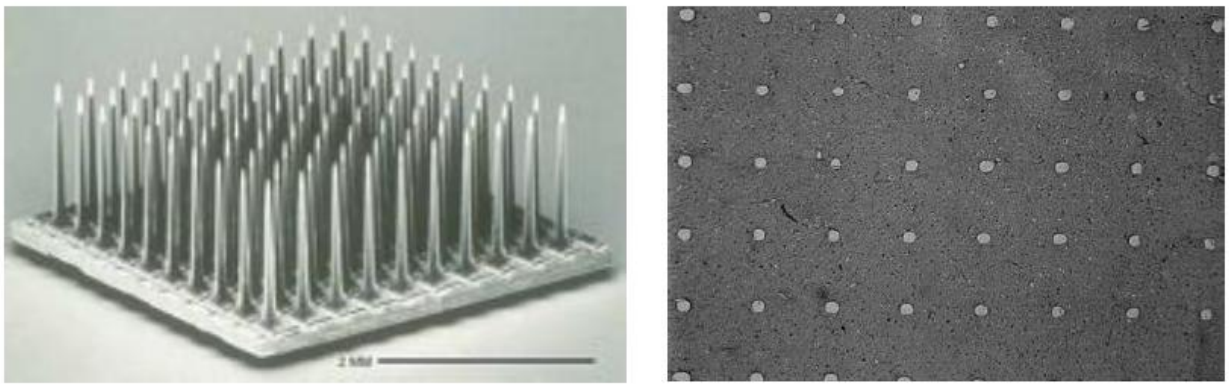
More than two decades later, other experiments on sighted subjects (Bak et al., 1990) and a blind about 22 years (Schmidt et al., 1996) took place with penetrating microelectrodes. It has been shown that the threshold current for the onset of phosphenes are then 10 to 100 times lower than with surface electrodes, a few tens of micro amps. In addition, the phosphenes are more stable and better defined.

In addition to qualitatively quantify the effect of stimulation parameters, Schmidt noted that the use of pulse trains allows for continuous phosphenes. He also established a spacing of 500 nm between two electrodes is sufficient to display two distinct phosphenes. The results presented by Schmidt (Schmidt et al., 1996) are still today a reference on the effects of stimulation parameters on perceived phosphenes in a blind human subject. They have caused a renewed interest for unprecedented visual prostheses.

2.1.3.2 Advances in physiological level

Consideration overlooked by previous work is the long-term effect of the introduction of a large amount of microelectrodes in the striate cortex. Dr. Normann's team at the University of Utah

conducted a series of experiments on cats with a matrix of 10 × 10 microelectrodes separated by a distance of 400 microns (Normann et al., 1999 , Rousche & Normann, 1999). This matrix, shown in Figure 2.1a is biocompatible since it is made of silicon and its ends are covered with platinum. After six months of implementation, analysis of the cortex of subjects showed gliosis and accumulation of fibrous tissue at all implantation sites as shown in Figure 2.1b. Tissues react to the presence of the electrodes, thus increasing the electrical impedance and generating stresses. However, the majority of electrodes of the prosthesis were still functional acquisition and stimulation after a period as long as three years (Normann et al., 1999).



(a) (b)

Figure 2.1: (a) Matrix microelectrodes Utah. From (House et al., 2006), with the authorization of JNS (b) Photograph of the surface of the visual cortex after six months of implantation. Spots are visible at the site of implantation. From (Normann et al., 1999)

For his part, Dr. Troyk of the Illinois Institute of Technology and his team focused their research to the location of phosphenes with in vivo tests on monkeys (Troyk et al., 2002; Srivastava et al. 2007). Their goal is to better understand and define the correspondence visuotopic, that is to say the relationship between stimulation sites on the primary visual cortex and the position of occurrence of phosphenes in the visual field. They were able to arrive at qualitative conclusions encouraging, but much remains to be done in this area.

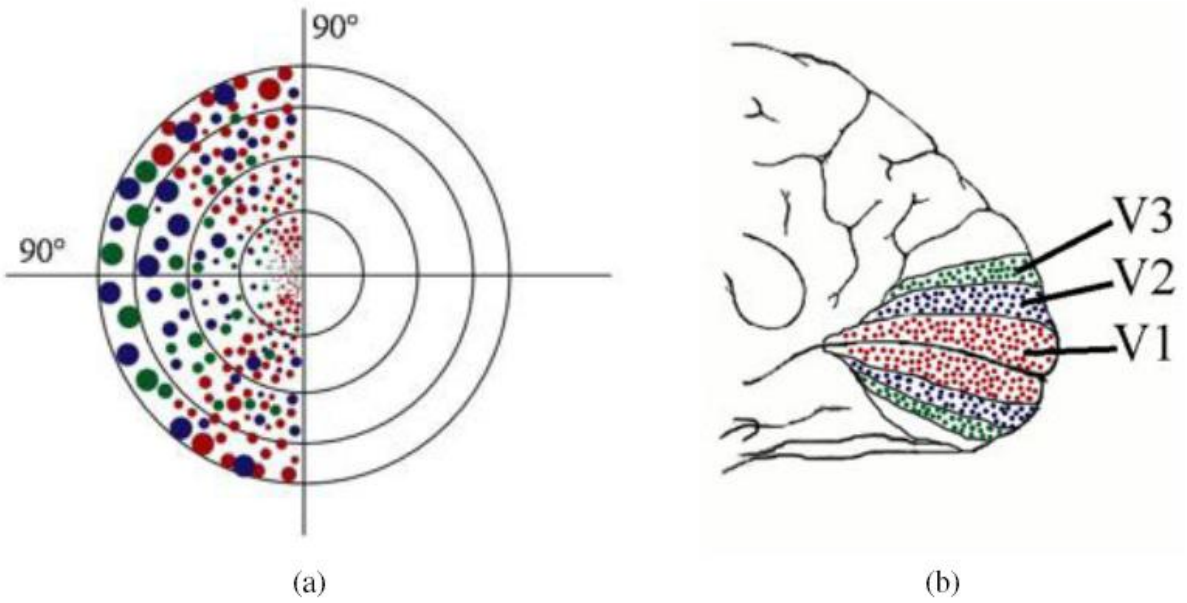


Figure 2.2: Correspondence visio-optic of V1 cortex (red), V2 (blue) and V3 (green). (a) Phosphenes in the visual field according to (b) stimulation sites in the occipital cortex. Modified from (Srivastava et al., 2007).

Despite these advances, there are significant drawbacks to the cortical visual prosthesis. Initially, a portion of the natural processing of the influx is bypassed, limiting the quality of the perceived image. In a second step, the implementation of this type of device is invasive and serious complications can occur. In a third step, a correspondence visuotopic one must first be established for each user. Finally, some studies suggest that, due to the plasticity of the brain, some areas of the occipital cortex tend to be retrieved by other senses, such as hearing, among blind people. It would be reasonable to believe that the correspondence visuotopic can be changed over time. However, this brain plasticity could be beneficial, as is the case for the cochlear implant (Fernandez et al., 2005), since some adaptation consent allowing the user to tame patterns phosphenes perceived.

2.1.3.3 Architecture of the visual cortex implant

While research continues on the medical side, several teams around the world devoted to the aspect rather microelectronics, that is to say, the design of integrated microsystems dedicated to the stimulation of the visual cortex and the basic functions such as wireless communication. If

each of these architectures has its own characteristics, it is possible to identify common elements and principles. Figure 2.3 shows the block diagram of a typical cortical visual implant.

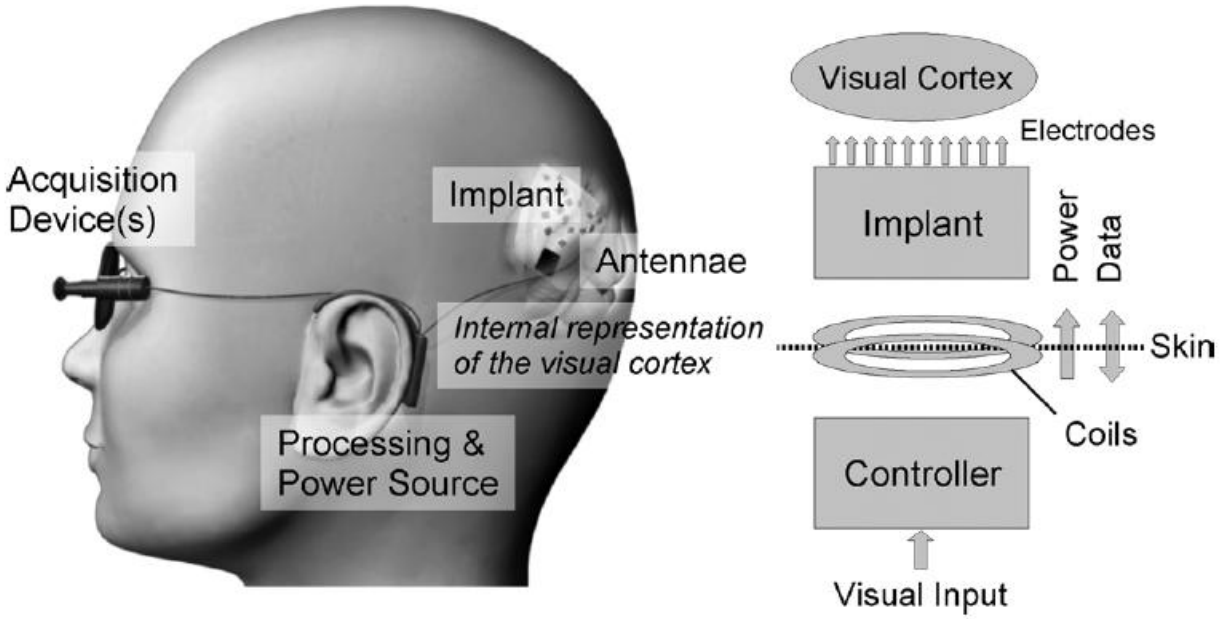


Figure 2.3: Typical architecture of a cortical visual prosthesis (Coulombe et al, 2007).

A camera captures images at a rate dependent on the subsequent processing. Acquired frames are then translated into commands stimulation by an external controller powered by a battery. Briefly, it is to simplify the image by retaining only the information relevant and understandable to the user. Several strategies for image processing are investigated. Correspondence visuotopic the user account is also held in here.

These data are modulated and transmitted to the receiver of the implant by the external transmitter via a wireless link. This transmission is usually by inductive RF waves. Parallel data, the energy powering the implanted part of the system is also transmitted via this connection. The RF link is essential to avoid wired connections which are potential sources of infection and mechanical stress to the implant. The receiver demodulates the data and retrieves the supply voltages. The data is sent to the controller, which interprets and internal control stimulators according to the instructions and parameters of stimulation received. Stimulators are responsible

for generating biphasic pulses of current and consequently inject through electrodes implanted in the primary visual cortex.

The following sections review the architectures of the most important visual prostheses in the literature.

2.1.3.4 Troyk's team at the Illinois Institute of Technology

The team of Dr. Troyk has developed a complete implant system used in conjunction with their experiments in vivo (Troyk et al., 2006; Troyk, 2009). This is shown in Figure 2.4. A total of 1024 stimulation sites is concerned, four implants of 256 microelectrodes, each composed of four sub-modules of 64 channels. The biphasic pulses are characterized by the amplitude of 0 to 64 uA and duration of 0 to 750 microseconds. Circuitry responsible for wireless communication has also been successfully implemented on separate stimulation chip.

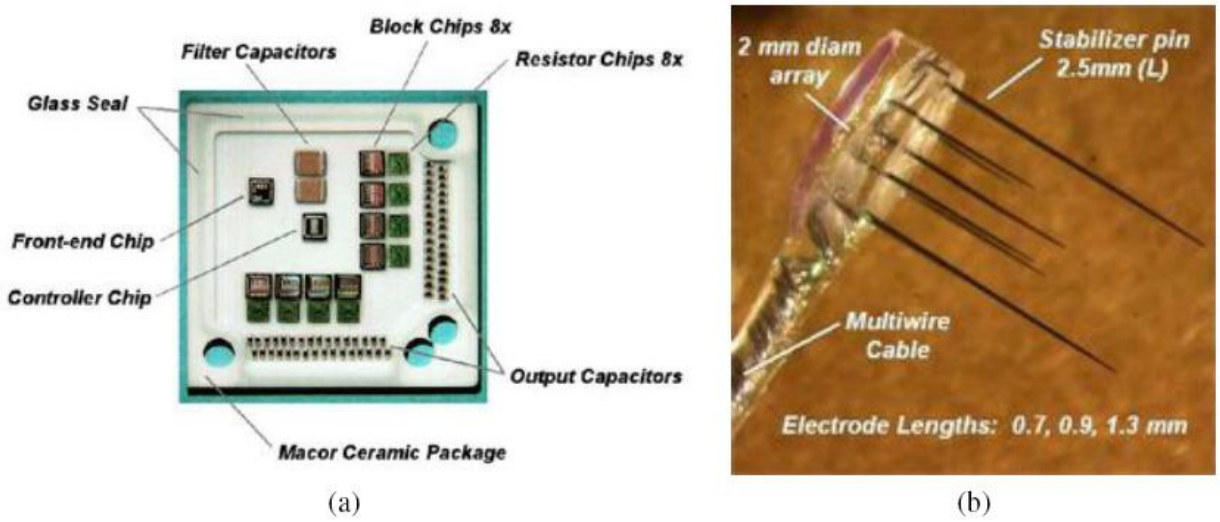


Figure 2.4: Implant of the Illinois Institute of Technology: (a) The implant modules 64 channels in its encapsulation, (b) Intracortical electrodes used in vivo tests. (Troyk, 2009).

From the point of view of architecture, team Troyk's team lags compared to other research groups. Their implant has a very large surface area and the currents generated are very limited in intensity. However, their works at the physiological stimulation of the visual cortex are fundamental references.

2.1.3.5 Wise's team at the University of Michigan

Wise and Najafi of the University of Michigan have developed a three-dimensional micro-compact capable of acquisition and stimulation (Ghovanloo et al., 2003, Yao et al., 2007). Their implant is characterized by a dense and complex assembly. First, each electrode has a plurality of stimulation points on a portion of its length to stimulation at different depths. These electrodes are grouped into eight channels probe, as they are shown in Figure 2.5a. The circuitry is integrated stimulators at this level. Biphasic pulses of maximum amplitude of 127 µA are supported with a supply of ±5 V. The implant shown in Figure 2.5b is itself composed of eight of these probes attached to a silicon platform on which there is also a chip dedicated to managing high-level implant. A total of 64 sites of stimulation is then supported. The probes are folded and assembled in a stack on the implant to minimize its thickness (Yao et al., 2007). The implant of Wise was not a telemetry system, the communication takes place using wire when tested in vivo in the guinea pig.

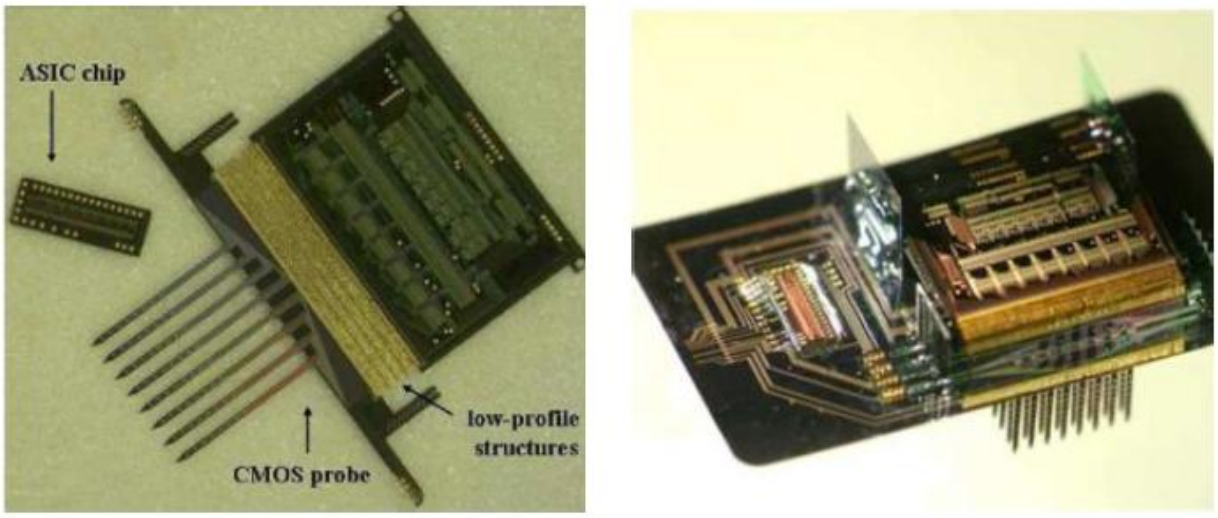


Figure 2.5: Implant of the University of Michigan. (a) Probe to eight channels. (b) Microsystem assembled. From (Yao et al., 2007)

2.1.3.6 Ghovanloo's team at the Georgia Institute of Technology

Formerly the team from the University of Michigan, where he worked with Wise and Najafi where he continued his research with Najafi, Dr. Ghovanloo focused in recent years on many aspects architecture of the visual prosthesis, such as telemetry (Bawa & Ghovanloo, 2008), the interface with the electrodes (Ghovanloo & Najafi, 2005) and the effectiveness of stimulations (Ghovanloo, 2006; Simpson & Ghovanloo, 2007). He has developed a complete prototype of the implant named Interestim-2B with which he was able to conduct experiments in vitro and in vivo in rats (Ghovanloo & Najafi, 2007). As the implant of Wise, Ghovanloo allowed stimulation at various depths. The complete system is shown in Figure 2.6. The maximum amplitude supported by the implant for biphasic stimulation is 270 µA with a power supply of 5 V. A complete implant has 64 channels while a total of 2048 stimulation sites are referred to long term.

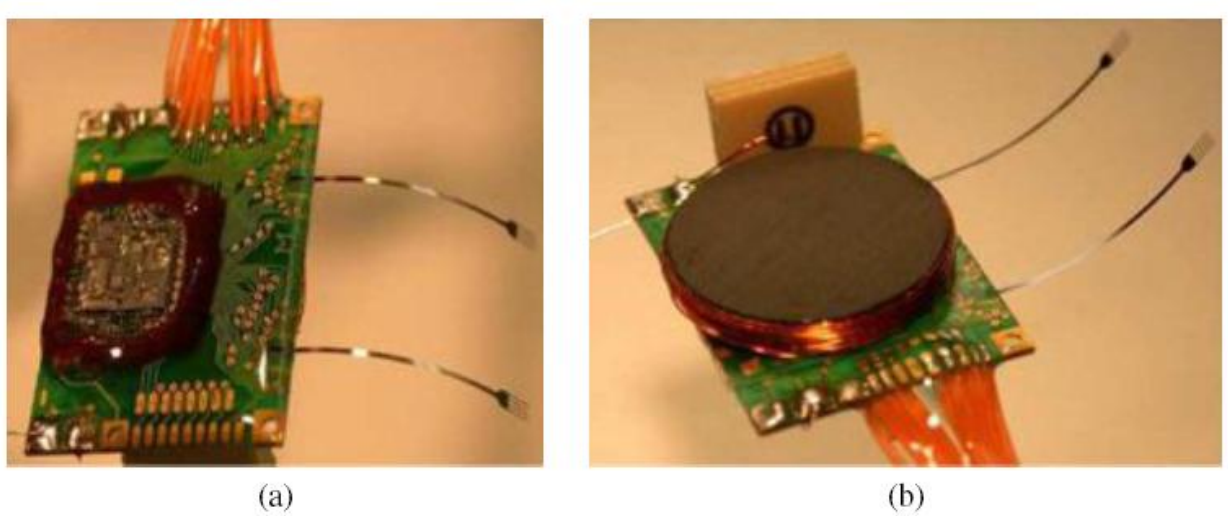


Figure 2.6: Interestim implant-2B 32 channels from North Carolina State University. (a) Top view showing the implant secured with epoxy. (b) Bottom view showing the inductance of the telemetry system. From (Ghovanloo & Najafi, 2007)

2.1.3.7 Sawan's Cortivision project of Polytechnique Montreal

This project is the visual implant performed by the Polystim laboratory, Dr. Sawan's team at Polytechnique Montreal, and is the starting point of the work done in the context of this specification. Until now, the achievements of Polystim affect not only the implantable part of the

system, including wireless (Coulombe et al., 2004), the control stimulation (Coulombe et al., 2002) and the electrodes (Ayoub, 2007), but also the non-implantable part comprises an image sensor (Sawan et al., 2006) and an external controller (Buffoni et al. 2003). A prototype has been built and in vivo experiments were conducted on rats to validate the architecture (Coulombe, 2007).

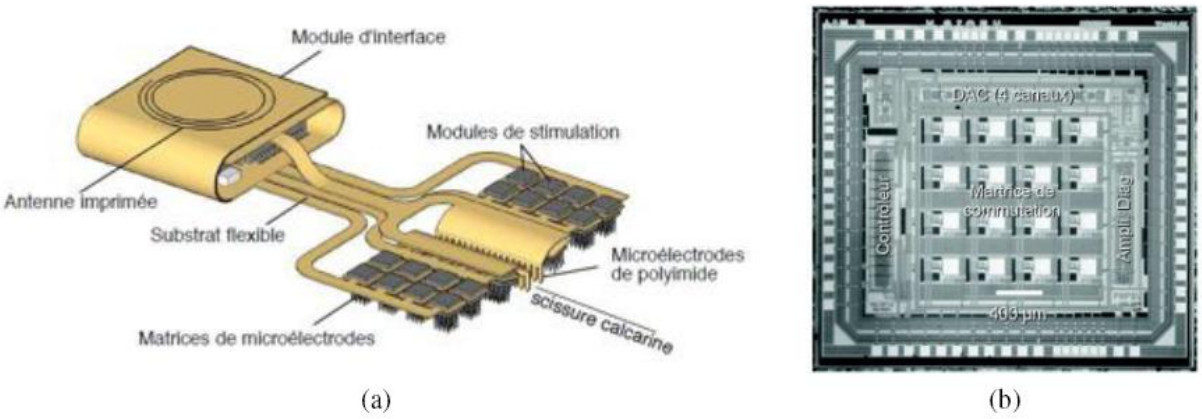


Figure 2.7: Cortivision intracortical visual implant. (a) Illustration of the complete implant. (b) Photomicrograph of stimulation module. From (Coulombe, 2007).

Figure 2.7 illustrates the architecture developed by Coulombe. This includes the wireless communication with the external unit and the recovery of the power. Stimulation at a maximum current of 140 µA is supported for biphasic pulses and power-supplies are 1.8 V and 3.3 V. Since the maximum voltage might be insufficient to interface electrodes, it was raised by 9 V external output stage during in vivo tests (Coulombe, 2007). The stimulation strategy is to set a stimulation module 16 channels on the back of a 4 × 4 matrix of microelectrodes. These channels are in fact divided into groups of four so that only four sites by stimulation module can be energized simultaneously. In the end, 64 of these modules make up the visual prosthesis for a total of 1024 sites. Each stimulation module also monitors the voltage developed by an electrode that provides flexibility and enhanced security.

2.2 Comparison of the main architectures

Summary of the main parameters of intracortical visual prosthesis is in Table 2.1. In order to compare precisely the data concerning the circuitries stimulation only, except Ghovanloo his telemetry circuitry is integrated on the same chip. This table is used to determine the order of magnitude of the specifications to be met in the design of the stimulator.

Table 2.1: Comparison summary of the main visual intracortical implants.

References	**(Troyk et al., 2006)**	**(Yao et al., 2007)**	**(Ghovanloo & Najafi, 2007)**	**(Coulombe et al., 2007)**
Process	BiCMOS 0,8-µm	CMOS 3-µm	CMOS 1,5-µm	CMOS 0,18-µm
Supply	N/A	±5 V	5 V	1,8/3,3 V
Area	2.0×2.0 mm^2	5.7×4.0 mm^2	4.6×4.6 mm^2	3.2×2.8 mm^2
Number of channels	8	64	64	16
Max. current	64 µA	127 µA	270 µA	140 µA
Output voltage	VDD – 0.5V	< 10 V	4,75 V	2,98 V
Power consumption	N/A	0.78 mW	16.5 mW	0.88 mW

2.3 Architectures of charge pump

As mentioned previously, the impedance of the microelectrode-tissue interface can reach very high values, causing problems at the voltage swing at the output of the pacemaker to maintain a constant current. The supply voltage must be high, which is not always possible for low power implantable devices. A DC-DC converter elevator (step-up) is then essential to generate a voltage higher than the nominal supply retrieved from the power source.

Whereas different classes exist for DC-DC converters, only switching converters may provide an output greater than the entry. These are divided into two types depending on how the conversion is performed: magnetic and capacitive converters. Since the integrated inductors occupy a large

area and often have a limited quality factor, only DC-DC switched-capacitor also called charge pumps are considered here.

The main purpose of this section is to describe and analyze different charge pumps and check which charge pump is right for our requirement. Because of the requirement of negative voltage generation, not all the charge pumps can be used for our specific design. A review of some charge pump architectures selected from the vast literature on the subject has been made in this section.

2.3.1 Chain Dickson charge pump

The first voltage multiplier circuit proposed by Cockcroft and Walton in 1932 was composed of a single chain capabilities interlaced switch activated an offset in two clock phases. To improve the conversion efficiency and output impedance, Dickson has developed in 1976 a new architecture based on the same principle of operation. This consists of a number of diodes in series; each node is connected to a capacitor. The other end of the building is controlled alternately by one of two clock phases; φ and φ- (Pylarinos, 2008). The modern version of the chain of Dickson, where the diodes are replaced by diode-connected MOS transistors is shown schematically in Figure 2.8. This architecture is the basis for the majority of the charge pumps today.

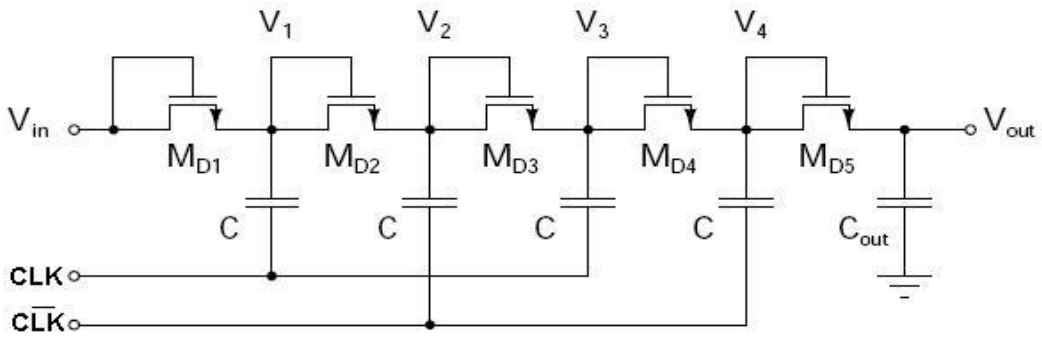


Figure 2.8: Dickson charge pump of four stages (Pylarinos, 2008).

When clock phase is high, for example φ = Vφ and φ- = 0, the corresponding capacities are the voltage at their terminals (in this case, V1 and V3) Vφ be increased. At this time, transistors series ($M_{D(2i)}$) lead the charge transfer from one floor. The next cycle (φ = 0 and φ- = Vφ), then it

is the odd transistors ($M_{D(2i-1)}$) that lead and so on. The result is a moving load always in the same direction that is to say to the output Vout. Between each stage, then there is a theoretical increase voltage $V\varphi - V_{th}$. Taking into account the parasitic capacitance Cp between each stage and present current I_{out} dissipated by the output load, the voltage generated at the output becomes:

$$V_{out} = V_{in} + N. \quad \frac{C}{C+Cp} \; .V\varphi - V_t - \frac{I_{out}}{C+Cp \; .f_{osc}} \quad - V_t \qquad \textbf{(2.1)}$$

where N is the number of stages and f_{osc} is the frequency of the clock (Pylarinos, 2008). It is then possible to determine the voltage increase A_V at each stage of the Dickson's chain:

$$A_V = \Delta V - V_t = \frac{C}{C+Cp}.V\varphi - \frac{I_{out}}{C+Cp \; .f_{osc}} - V_t \qquad \textbf{(2.2)}$$

As CMOS technologies are more miniaturized, the gap between VDD and Vt and, therefore, increased A_V is reduced. In addition, due to the body effect, Vt increases as the voltage increases at a given stage, which means that A_V decreases with N. To overcome these problems, several changes to the architecture of Dickson have been proposed over time.

2.3.2 NCP-2 Architecture

First, the diode-connected MOS transistors are added in parallel M_{Di} with another transistor M_{Si} whose gate is controlled by the output of the next stage (Wu & Chang, 1998). Thus, when the pump starts, M_{Si} is that the load is getting transferred. The threshold voltage Vt is canceled by the fact that its gate voltage is higher than its drain voltage from the previous stage. This phenomenon, however, ensure that M_{Si} is never completely closed, causing a leakage current. To solve this problem, the architecture NCP-2, where two other transistors controlling the gate voltage M_{Si} are added at each stage, has been developed (Wu & Chang, 1998) and is shown schematically in Figure 2.9.

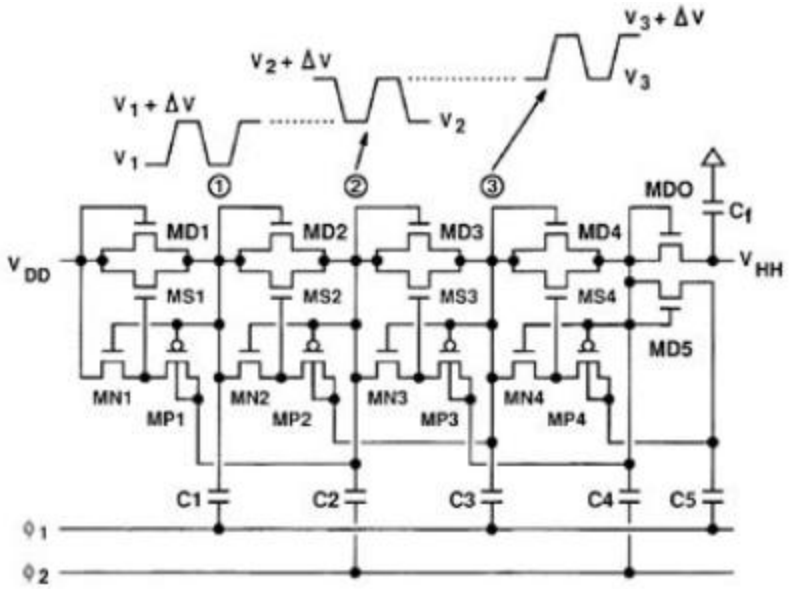


Figure 2.9: NCP-2 charge pump of four stages. From (Wu & Chang, 1998)

This circuit was used and slightly modified at the output stage through a peripheral nerve stimulator (Nadeau & Sawan, 2006). Two diode-connected transistors have been added to the end of the chain to raise the control voltage components M_{Si} of the last two stages, thus improving the transfer efficiency. In the same way, the implementation of a second pair M_D/M_S on the top can also be used for the same purpose, such as for circuits PGI-1 and PGI-3 (Hu & Chang, 2006).

2.3.3 Dynamic polarization of the substrate

Another technique improves the load transfer of architecture of Dickson is the dynamic control of the substrate voltage of diode connected MOS transistors (Shin et al., 2000). As shown in Figure 2.10, the NMOS transistors have been replaced by PMOS which are isolated from the substrate in the N-type wells. The bias voltage of the wells may then be controlled dynamically by the other two transistors according to the cycle, significantly reducing Vt by body effect and improving the voltage increase stage by the charge pump.

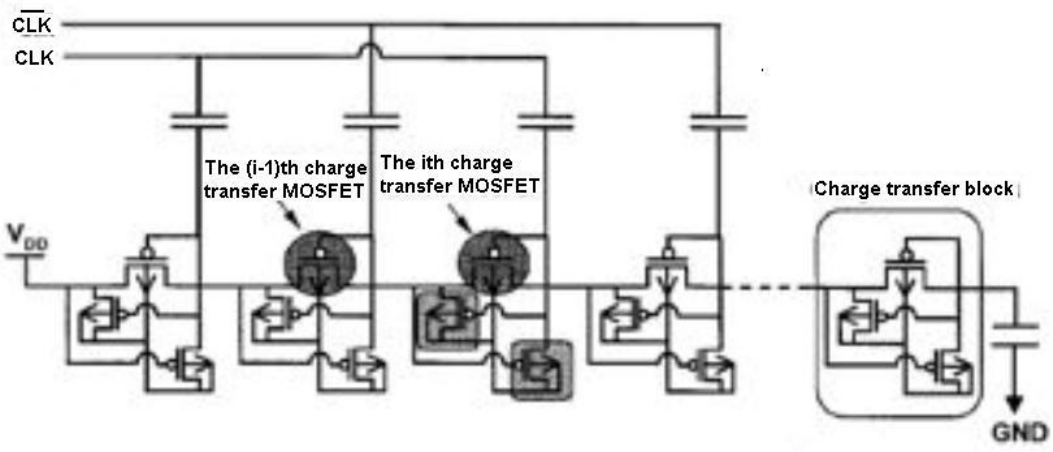


Figure 2.10: Charge pump with dynamic biasing of the substrate. From (Shin et al., 2000)

2.3.4 Dual path charge pump

It can be noticed that in the architectures presented so far, the output stage receives loads of a half-cycle. To maximize the effectiveness of voltage conversion, an implementation in two independent paths whose clocks are inversed has been implemented (Park & Chung, 2007). Thus, the output stage receives loads in each half cycle, by ensuring that its rise time is faster and that it supports larger output currents. The trade-offs to take advantage of these improvements is the duplication of circuitry.

2.3.5 Pelliconi charge pump

Pelliconi architecture, with one stage is shown in Figure 2.11, is not directly based on the chain Dickson (Pelliconi et al., 2001). Each stage consists of two NMOS and two PMOS which is actually composed of two paths controlled by two clock phases, maximizing the charge transferred per cycle. MOS transistors are used as switches here. This implementation allows you to generate high voltages despite its simplicity.

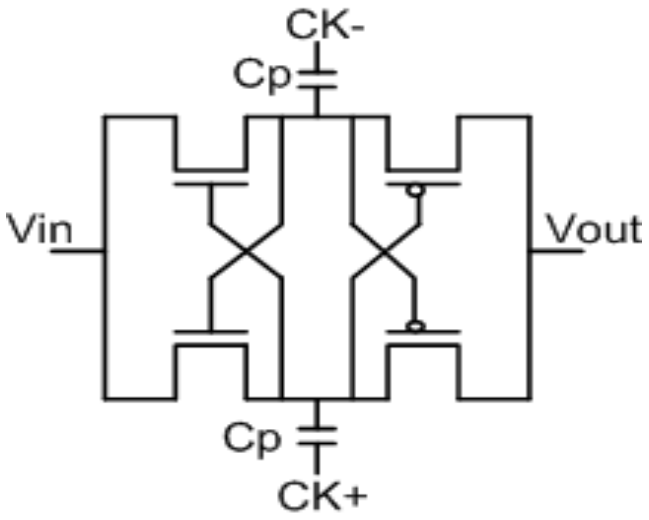


Figure 2.11: One stage of the Pelliconi charge pump. From (Pelliconi et al., 2001)

2.3.6 Clock doubler charge pump

A clock doubler circuit (Huang et al., 2008) can be introduced at each stage of a charge pump to elevate tensions clocks φ and φ-, always with the aim of eliminating Vt. This strategy has been applied to several different architectures (Yamazoe et al., 2005; Chebli & Sawan, 2007). Figure 2.12 shows the circuit that repeated cascade can also generate a clock whose voltage is very high.

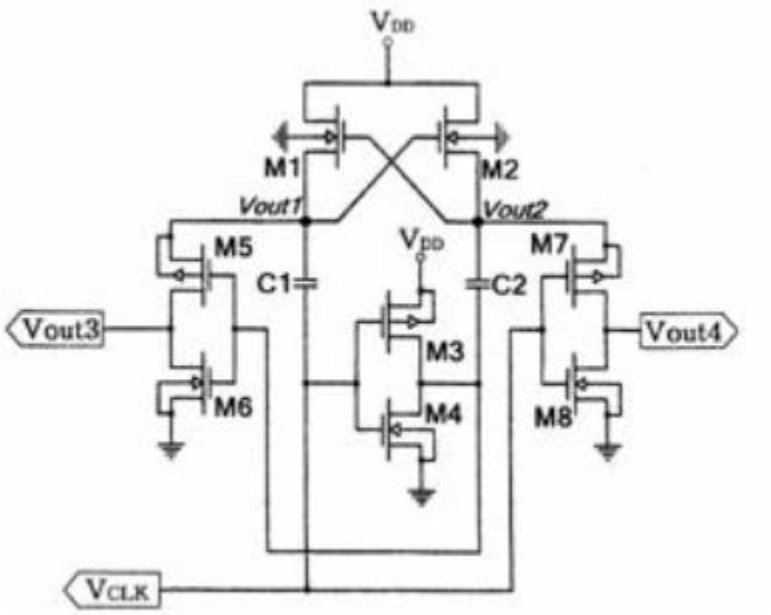


Figure 2.12: Clock doubling circuit. From (Huang et al., 2008)

2.3.7 TPVD (Two-Phase Voltage Doubler) charge pump

The TPVD charge pump is formed by four switching transistors [M0-M3], a flying capacitor Cp and a load capacitor CL (Saiz et al, 2011). Figure 2.13 shows the easiest transistor level schematic of the TPVD cell structure where one N-type MOS and three p-type MOS transistors are used as switching transistors. Two different switching stages are needed in order to make the TPVD circuits work. The problem with this design is that it cannot produce negative voltage.

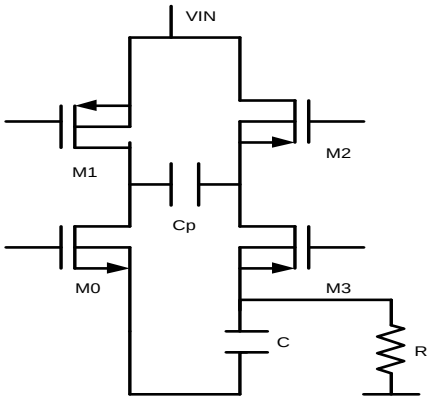


Figure 2.13: TPVD charge pump with one stage (Saiz et al, 2011)

2.4 Generation of negative voltage

As the efficiency of a charge pump decreases with the number of stages, it is preferable to have an architecture which consists of two DC-DC converters to generate a positive high voltage and a negative high voltage. Thus, each pump has fewer stages. This choice leads to the problem of supply voltage lower than the body. Using a triple-well technology supports multiple supply voltages can then be essential.

The majority of architectures in this section also supports the generation of negative voltage virtually unchanged. Usually, it suffices to reverse the input and the output of the DC-DC converter that is to say to connect the output to ground and the input to the load capacity. The direction of the flow of charges being unchanged, they are then pumped into the ground and a negative voltage is generated in the input. However, some precautions must be taken at the

connection well when drawing masks to avoid short circuits and triggering of parasitic thyristors (latch-up) (Bloch et al., 1998; Yamazoe et al., 2005).

2.5 Comparison of charge pumps

Following the listing of various architectures charge pump, a summary is required to be able to compare them. The requirements to be met in order to properly evaluate the performance of a DC-DC converter include among others the output voltage; the current that can be dissipated by the load, the efficiency of conversion, the surface and the complexity of the circuitry. These results depend on a multitude of parameters including the manufacturing process used, voltage, number of floors, the clock frequency, the pumping capacity and output capacity.

A fair comparison is not feasible in practice, because each of the circuits described above has been implemented in the context of its own to achieve a specific goal. In addition, measurements on prototypes are not all complete, each author focus on outcomes that are important. We must therefore consider the various parameters and overall results to make an informed choice.

All the charge pumps mentioned above generates only positive voltage except pelliconi charge pump design. With peliconi charge pump design, negative voltage can be achieved but it suffers from latch-up issue which destroys the chip. Also, most of the above mentioned designs cannot be used with designs that can reduce power consumption. For Chain Dickson, NCP-2 architecture and dynamic polarization of substrate designs the output stage receives loads of a half cycle. Also the effect of V_t causes significant drop of output voltage. These problems except V_t effect have been solved by introducing dual path charge pump design but for this design, the number of components increase significantly, and the output voltage reduces beyond expectation with the increase of number of stages. Repetition of Clock doubler charge pump design can also generate a clock whose voltage is very high but this clock cannot be used for the circuit itself and thus external clock is necessary. Also load driving capacity of Chain Dickson, NCP-2, dynamic polarizarion and clock doubler designs face output voltage sustainability issue while driving high load.

The purpose of this master thesis is to implement a suitable charge pump that can generate both positive and negative voltages, drives higher load so that more electrodes can be derived without output voltage deviation and consumes low power.

2.6 Conclusion

In this chapter, a brief review of the literature was performed for all subjects relevant to this thesis. First, the possible approaches to design a visual implant were presented with emphasis on cortical stimulation. Progress on the stimulation of the visual cortex have been incurred prior to the presentation of visual implants architectures most relevant. Secondly, different charge pumps have been briefly discussed and finally, various architectures pump loads were presented in order to raise the output voltage to the electrodes interface.

CHAPTER 3

LOW-POWER HIGH-VOLTAGE CHARGE PUMP

3.1 Introduction

Research has shown that micro-stimulation can produce partial vision as it can control vision characteristics (size, brightness, duration) to some extent (Schmidt et al, 1996). The general procedure is to apply electrical current pulses in programmable pattern through electrical stimulator. The impedance of nerve tissues and electrode interface is normally variable and high. This impedance magnitude depends on different factors like electrode geometry, material, frequency etc (Sawan et al, 2007). Depending on this value and the intensity of the current pulses, the required supply pulses can vary from few voltag to as high as 20 V. This is one of the most important constraints because constant current stimulation is preferred to voltage one (Merrill et al, 2005) and to provide desired constant stimulation current, the supply voltage must be above a certain level all the time. Most of the devices used nowadays employ batteries for this purpose and are used daily. So, power consumption becomes a serious issue and it is necessary to lower it by designing advanced low-power CMOS circuits.

Some solutions have been proposed over time. Yao et al (Yao et al, 2007) generated supply less than 10V (±5V) in 3µm CMOS technology with external high voltage supplies. Nadeau et al (Nadeau et al, 2006) proposed a system that generates its own high-voltage supplies from a single 3.3 V. They used two integrated circuits in different technologies to generate the required high-voltage signals for the output stage while keeping the digital part at low-voltage technology to reduce power consumption.

Unfortunately this design was paid no specific attention for the negative voltage generation which led to potential problem. To provide biphasic current pulses to the electrodes, generation of negative voltage is the most reliable way. Ethier et al (Ethier et al, 2011) generated ±9V from a 3.3V power supply and also solved the issue with negative voltage generation. They used two

positive and three negative stages to reach to that voltage, but the power consumption was reasonably high.

In the next sections, we have proposed two low-power high-voltage charge pumps to achieve more than 20 V. Both the design produce the required current but the design in high voltage technology is more reliable although it consumes more power than the design in low voltage technology. The deep N-well technology of high-voltage CMOS technology gives a simple but reliable design. Design in low-voltage technology is more complex and has more technology limitations.

3.2 Architecture of high-voltage charge pump

In this section, designs have been proposed in two different technologies (0.8µm and 0.13µm CMOS technology). The main architecture is the same for both technologies but 0.13µm design has more technological limitations when it comes to high voltage generation. Since low-voltage technologies are much preferred for implantable devices because of the target of low area and relatively low-power consumption, generally both low and high-voltage technologies are used together to have a tradeoff between high voltage, area and power consumption. Successful implementation of this design in low-voltage technologies like 0.13µm should lead us to the possibility of integrating a whole system only in low-voltage technology.

The different modules of the design are illustrated in Figure 3.1. This design comprises of non-overlapping clock generator, high-voltage level shifter, charge-pump blocks, inverter and two types of capacitors, stage capacitors and load capacitors. The non-overlapping clock generator delivers two non-overlapping clocks from the supply clock signal, which then passes through the high-voltage level shifter which shifts the voltage level of the clock signal from 0-3.3V to 0-6.6V. The level shifters also act as clock driver to provide input signals to the charge pump blocks. The first two level shifters provide 0-3.3V signals to the first positive cycle block which produces 6.6V from 3.3V power supply. This 6.6 V supply is then used as supply voltage for the rest of the level shifters. The quadruple well technology of 0.8µm CMOS process offered by TELEDYNE DALSA ensures no latch-up occurs while providing these different voltages to the

level shifters. For 0.13µm technology, T3 isolation-well has been used to isolate the NMOS transistors to have the same flexibility. T3 isolation-well is an isolation well provided by IBM which isolates the devices inside the well from the p-substrate.

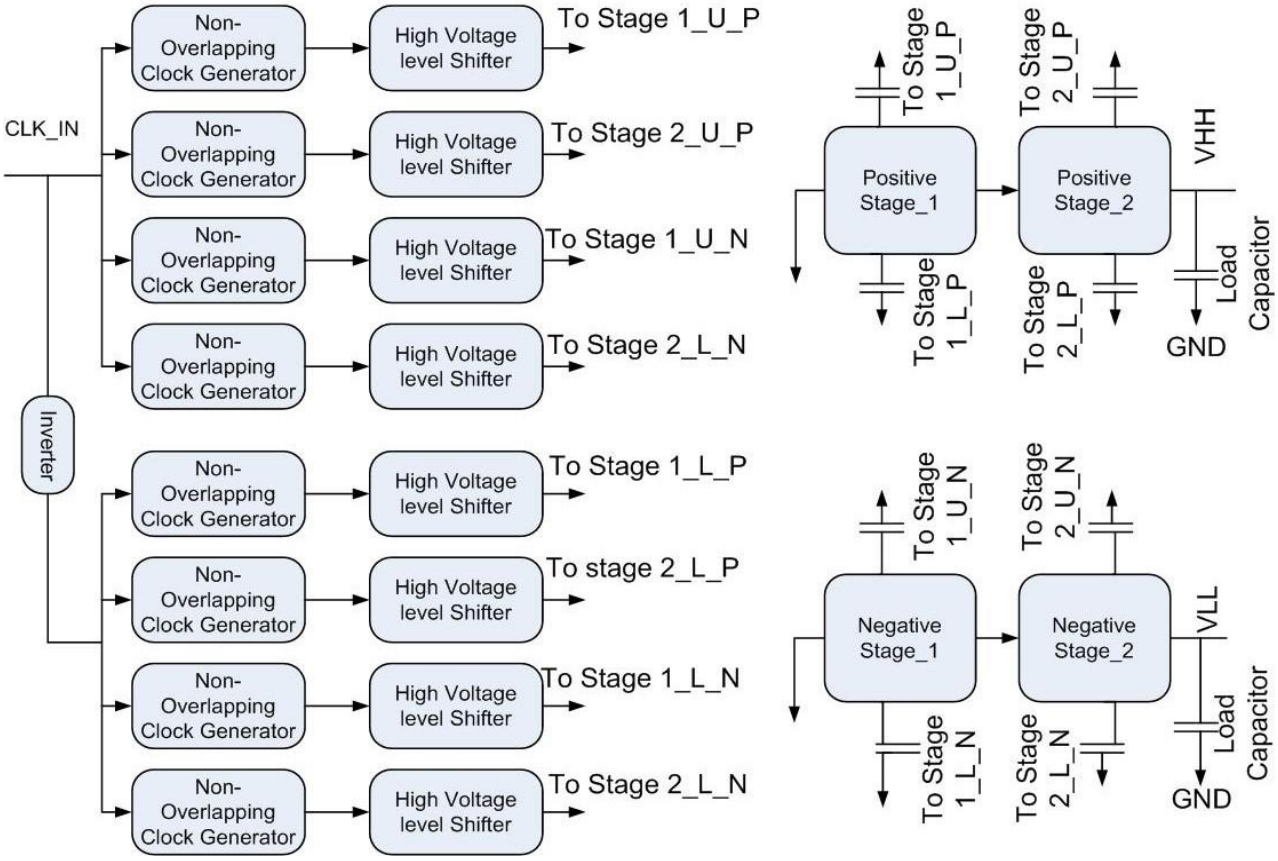


Figure 3.1: Proposed high-voltage charge pump architecture.

3.3 Non-overlapping clock generator

Research (Saiz et al, 2011) has shown that the main reason of the high power consumption of a charge pump is due to the fact that during the transition of MOSFETS to switch on and off, for each cycle, all the transistors remain switched on at the same time for a very short time. But during this transition period, there is huge power consumption happens for the charge pump circuits. Details of the process have been described later in the chapter. It has been found that if we use two separate clock pulses that don't trigger at the same time to provide the pulses to the

charge pumps, transistors of one stage turns off just before the transistors of the next stage is switched on. Non-overlapping clock pulse generator has been used for this reason in this design.

3.3.1 Selection of non-overlapping clock generators

Although there are many complex architectures and topologies of non-overlapping clock generators circuits, the easiest way to design such circuits is the combination of NAND/NOR gates with several delay cells. Using this technique the dead time between the obtained non-overlapping signals depends on the propagation delay that each delay cells adds to the primary clock source in its propagation path. Each delay cell can be formed by simple digital MOS inverters, current-starved inverters, or RC-inverters as it is explained as follows.

3.3.1.1 Gate based delay cell

A classical PMOS-NMOS inverter (Mondal et al, 2010) can be used as a simple element and different delay can be obtained by cascading a number of inverters, as illustrated in figure 3.2.

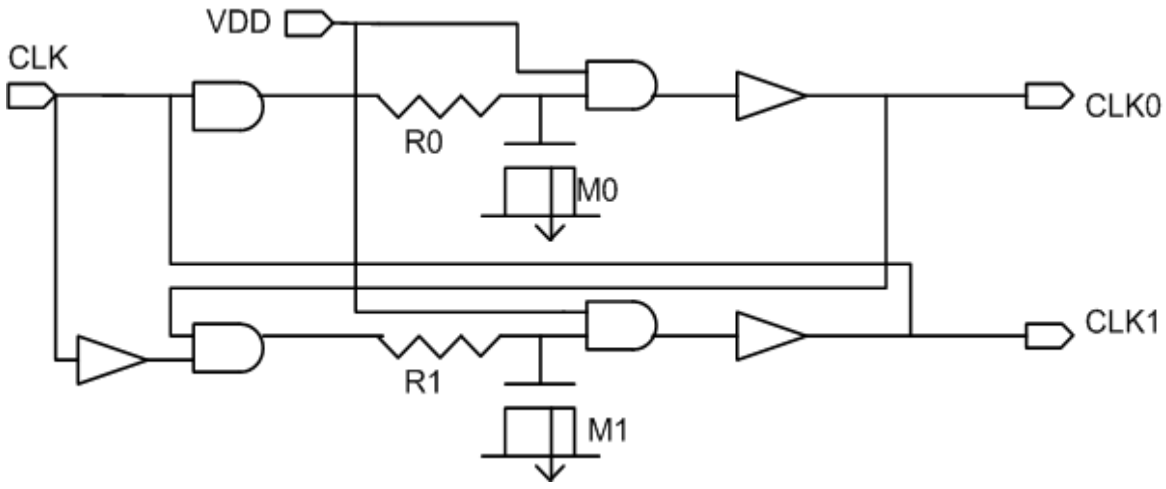


Figure 3.2: Non-overlapping clock generator circuits based on gate delay cells (Mal et. Al, 2007).

However, this type of delay elements has some major drawbacks. A great quantity of delay cell stages are needed to achieve a large dead time Δt between the non-overlapping signals if the

propagation delay t_d added by each delay cell is small. The more delay cells are needed, the more internal power consumption of the non-overlapping clock generator block is increased (basically due to the dynamic power consumption of the inverter delay cells). Increased delay cells cause increased area requirement. Also, minimum delay adjustment step that is possible in a given technology is about two inverter delays using minimum size transistors. This is often too coarse for high-precision low-jitter applications. Once fixed number of delay cell stages, it is not possible to change dynamically the achieved dead time gap Δt unless the number of delay cells are increased/decreased (Mal et. Al, 2007).

3.3.1.2 Current starved inverter based delay cell

The fundamental circuit elements generating delay in a classical PMOS/NMOS inverter based delay chain are MOSFET current sources charging MOSFET gate capacitors. If the current that charges and discharges these capacitors is restricted by current controlled transistors in series with the switching transistors in the inverters, then a delay element with adjustable delay is obtained leading to the possibility of an adjustment control of the Δt dead time interval (Saiz et al, 2011).

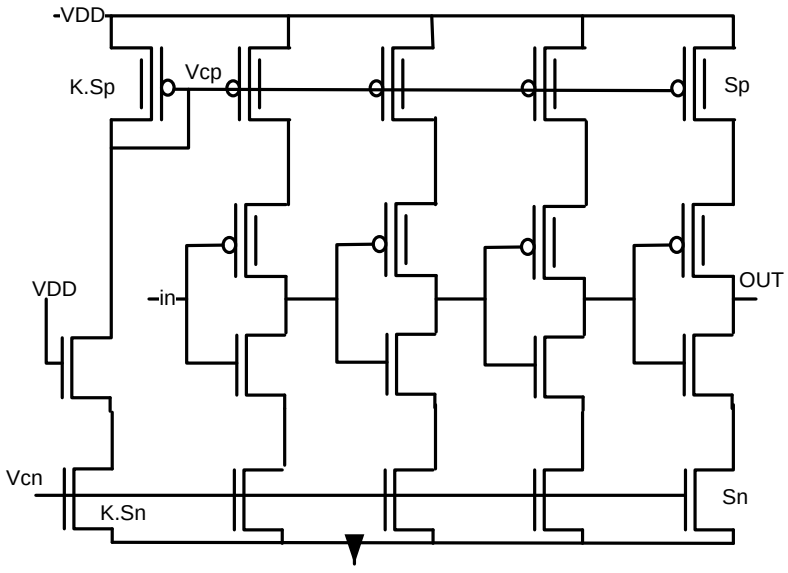


Figure 3.3: Non-overlapping clock generator circuits based on current-starved inverter delay cells (Majek at. Al, 2009).

So, theoretically using this approach would be possible to adjust the propagation delay t_d of each delay cell in order to use less gate-based delay cells. Nevertheless, the number of current starved gate-based delay cells would be very large (Majek at. Al, 2009).

3.3.1.3 RC-based delay cell

Non overlapping clock generators are used to deliver two non-overlapping clocks from the supply clock signal to ensure that two FETs are not on at the same time. In order to minimize the number of delay cells and achieve a reasonable large Δt dead time, it is possible to use the cause of propagation delay the charge and discharge time of an RC network where a MOS transistor acts as a capacitor as shown in figure 3.4. The dead time Δt between the generated non-overlapping signals depends on the values of the resistors and sizes of the capacitor-connected MOS transistors. Although Δt cannot be configured dynamically, this configuration offers lower power consumption than the inverter based topology and occupies less layout area (Saiz et al, 2011). This fact has been the main reason for using this architecture as delay cell of the non-overlapping clock generator component of the used pelliconi charge pump design.

The conceptual functionality of this circuit is very simple. The operation is based on the fact that the falling edge of the input clock signal clock passes through the input AND gate while the rising edge has first to propagate through the other input AND gate and the cascaded delay elements. Although this circuit works well for our design purposes, it has minor drawback. Note that the clock signal is propagated by two different input paths at the beginning of the non-overlapping clock generator component (Mal et al, 2007). One has an extra inverter that the other one doesn't have. So, based on the fact, what is obtained is a nonsymmetrical pulse width of the complementary clocks when the pump is operated at a very high frequency in the KHz range as the one used in this architecture. It could be a problem in a more sophisticated high-frequency charge pump designs. An easy way to overcome this issue is to use a passive matching delay element at the missing inverter input path (a PMOS-NMOS combination pass gate with the same size of the input inverter cell)

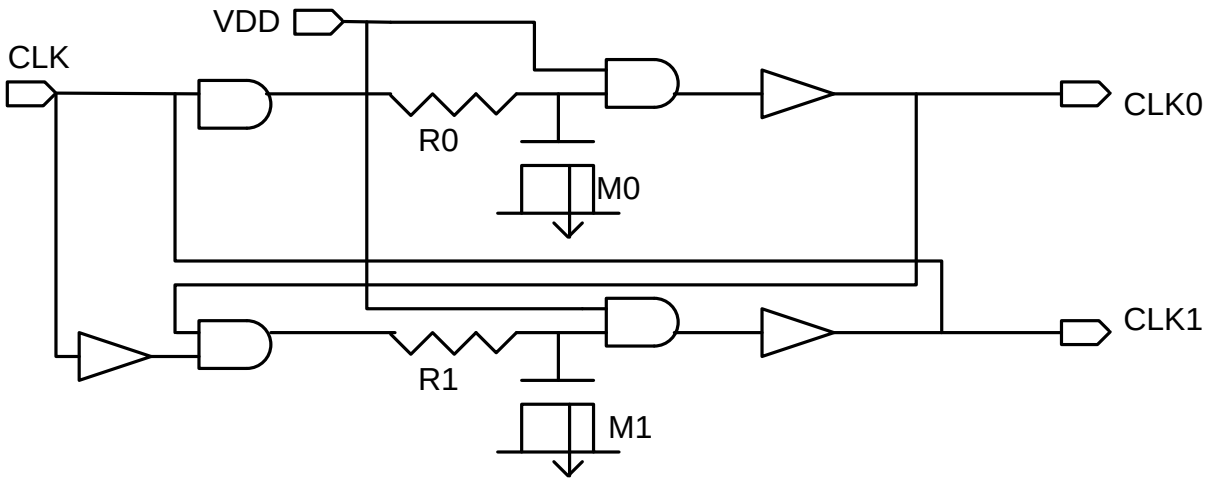


Figure 3.4: Non-overlapping clock generator circuit based on RC-based delay cells (Mal et al, 2007)

3.4 High-voltage level shifter

The maximum voltage amplitude of the non-overlapping clock generator through the presented delay cells is equal to the biasing voltage VDD of the digital gates of these cells which in this case is equal to VDD (3.3 V). The maximum voltage amplitude of the non-overlapping clock pair generated through the presented delay cells is equal to the biasing voltage VDD of the digital gates of these cells. Hence the obtained non-overlapping signals are in the pure digital domain. That means that 'high-voltage' level-shifter circuits are also needed in order to increase the amplitude of the generated CLK_k signals and fulfill the conditions for a correct switching control management of the charge pump cells. A level-shifter circuit translates an input low-voltage VDD_L signal to an output high-voltage VDD_H signal (Saiz et al, 2011).

Choosing the correct architecture of the charge pump's level-shifter circuits is also one of the key issues that must be solved if an efficient charge pump is desired. The power consumed by the level-shifter circuit should be taken into account when calculating the total power efficiently of a charge pump circuit.

The power consumption of a level-shifter circuit is formed by two terms: the static and the dynamic power consumption. Focusing on low power strategies in order to minimize the total

power consumption is one of the key issues that designer must be taken into account when using level-shifters since dynamic power consumption is inherent in such circuit and cannot be avoided when designing charge pump (due to the periodical and switched nature of the clock signals. Another big source of power dissipation is a high short circuit when the circuit is switching from one state to another. This short circuit current will be present in all level-shifters (Majek et. Al, 2009).

This section describes some of the existing level-shifter circuit topologies showing the main characteristics of each one and focusing specially on its power consumption behavior and shows the design and development process of the level-shifter architecture that has been selected to build up the High-voltage Level-shifter component.

3.4.1 Conventional cross-coupled level-shifter

Cross-coupled PMOS transistor (M1 and M2) are used in conventional level-shifters as it is illustrated in Figure 3.5. In order to implement such circuit for being used on a high-voltage environment (VDDH> 5V) high-voltage type NMOS and PMOS transistor must be used as pull-up and pull-down devices. If the input is low (0V) then M3 and M2 are switched on, M4 and M1 are switched off and the output node is equal to VDDH. If the input switch is too high VDDH then M4 and M1 are switched on M3 and M2 are switched off and the output node goes low (0V). Therefore using this configuration, the output voltage experiences a full swing ranging from 0V to VDDH. In addition, the pull-down NMOS transistor has to overcome the PMOS latch action before the input static charges. As a result, high short circuit current flows during the switching, leading to excessive power dissipation. Moreover, this conventional level-shifter has some problems when working in a high-voltage environment since the full-swing output (from 0V to VDDH) could damage the gate oxide of M1 and M2 transistor depending on the maximum breakdown voltage allow by the integration technology (Majek et. Al, 2009).

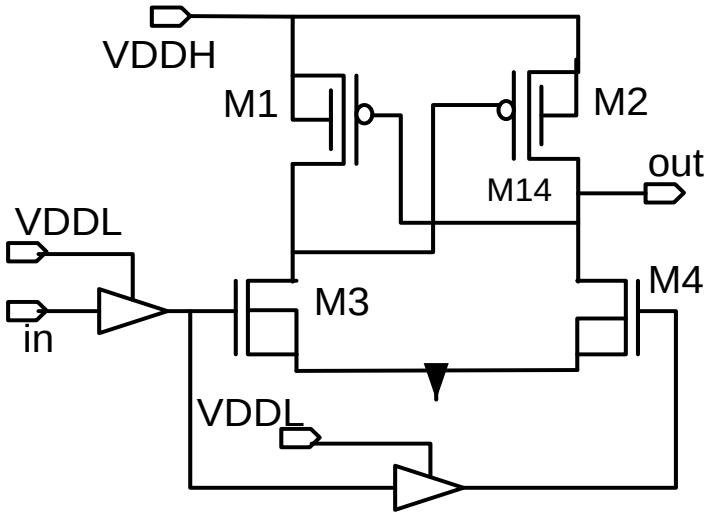


Figure 3.5: Schematic of conventional cross-coupled level shifter circuit (Majek et. Al, 2009)

3.4.2 Bootstrapping-based level-shifter

Otsuka and Horowitz proposed a novel bootstrapped gate drive of the cross-coupled PMOS transistor (Otsuka et al, 2007.) in order to increase the switching speed of the circuit and reduce the power dissipation due to the shoot through current trying to minimize the amount of time where PMOS and NMOS transistors are switched on together. However, the gate of the cross-coupled PMOS transistor still suffered a full swing voltage signal from 0V to VDDH (Saiz et al, 2011).

In order to overcome this problem Tan and Sun proposed new bootstrapped-based level-shifters (Tan et al, 2008.) as shown in Figure 3.6 that reduced the voltage swing applied on the gate of the cross coupled M1 and M2 transistors while at the same time improve the power efficiency of the level-shifter circuit since as voltage swing become smaller power consumption level decreases.

In this level-shifter circuit the pull-down NMOS transistor (MN1 and MN2) are driven by voltage signal between 0V and VDDH while the pull-up PMOS transistors (M1 and M2) are driven by signals between (VDDH and VDDL. The swing reduction is achieved using bootstrapping capacitors to create a voltage shift in the gate drive of the pull-up transistor. In this configuration, M4 is also driven by a voltage signal that swing between 0V and VDDL while M3 is controlled by a signal between (VDDH-VDDL) and VDDH (Finco et. Al, 2002).

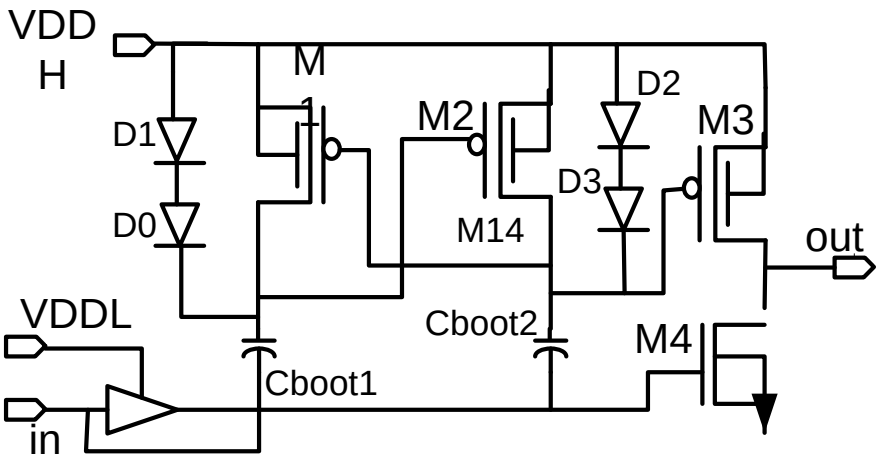


Figure 3.6: Schematic of bootstrapping-based level shifter circuit (Finco et. Al, 2002)

Initially, when the input is low (0V), M1 is off and M2 is on, Cboot2 is charged to VDDH through M2. Cboot1 is charged by diode-connected transistors (D0 and D1) to a voltage of (VDDH-2Vdiode). M4 which is driven by the component of the input turns on and pulls the output to ground. M3 remains off as node B is at VDDH. As the input changes from 0V to VDDL node A is pushed to (VDDL+ VDDH-2Vdiode) while node B is pull down to (VDDH-VDDL). M3 is turned on to source current to the output, while M4 is turned off. Subsequently node A is discharged to VDDH through M1 is restricted to swing off in a shorter time, thus minimizing the short circuit current flow that is present in all level-shifters. Part of the charge is Cboot2 is transferred to the gate of the M3 when the input goes low (0V). When the input goes high (VDDL) the charge on the gate of the M3 flows back to the capacitor. In this way, charge is conserve as it is transferred between the bootstrapping capacitor and the PMOS gate. A small fraction of charge return to VDDH in the high stage (node B is high); while in the low state,

charge on Cboot2 is replenished through the diode-connected transistors. This slight charging and discharging are necessary to ensure proper operation of the circuit (Finco et. Al, 2002).

The bootstrapping capacitors Cboot1 and Cboot2 should not be too small in the design. If they are too small, the voltage swing at nodes A and B will be reduced flowing to the charge redistribution. The reduction in voltage swing will correspondingly cause slow switching between low and high voltage states. The effect of small capacitance is more severe in pulling up the output from the low to high than from high to low. This is obvious as the potential at node B affects the current in M3 directly during charging up the loading capacitors. In addition, the raise time is very sensitive to the charging current. While pulling down the output, the gate voltage of M4 is always the same VDDL. The current flowing in M4 is relatively stable which leads to a fall time not sensitive to the bootstrapping capacitor (Saiz et al, 2011).

The present level-shifter circuit consumes much less power (Tan et al.) than the conventional one (saving as much power as 70%). However its area is larger than the conventional level-shifter because of the extra capacitors and the extra transistors (around three times larger than a conventional level-shifter).

3.4.3 Dynamically controlled HV level shifters

Although the presented level-shifters circuits explained in the previous section can work on a high voltage environment with the suitable use of a high-voltage CMOS design technology and the appropriate caution regarding transistor’s breakdown voltages they were not planned to be used on such environment.

Various methods have been proposed to minimize the static current consumption of level-shifter circuits by Doutreloigne et al. Huang et al and Khorasani et al. The architecture developed by Doutreloigne et al was full-custom designed with the same high-voltage BCD technology environment. Moreover, it was also designed focusing on having an ultra-low-power

consumption. Hence, this fact has been the main reason to choose this circuit as the main one of the level-shifters circuits designed in this thesis work and the architecture to be used for developing the HVLS cell of the charge pump architecture (Saiz et al, 2011).

The dynamically controlled high-voltage level-shifter circuit proposed by Doutreloigne et al is a highly complex evolution on the basic high-voltage level-shifter circuit shown in figure. This basic circuit exhibits a classic a complementary output stage with independent control of the gate voltage of M1 and M2 transistors. However, the gate control of M2 transistor is not optimum. When the input data line is switched from a logical "1" to ''0", the V_{GS} of M4 and M1 transistors is not entirely threshold to 0V but to a value of approximately -1 V being the threshold voltage of M1 transistor. Hence, M1 is not driven 100% into cut-off region and the lower level of the output voltage is 0.5 V instead of the ideal 0V value. This drawback can be easily solved adding a current mirror (M5 and M6 transistor) where a constant I_{bias} current source ensures that the V_{GS} of M4 and M1 transistors is pulled-down to 0V on the "1" to "0" transition leading to a rail-to-rail output voltage (Doutreloigne et al.).

Nevertheless, the improved basic level-shifter circuit of figure still has one major drawback: it shows continuous power dissipation in the current mirror independently whether a "0" or a "1" is present at the input data line. In order to overcome this drawback, Doutreloigne et al proposed the level-shifter architecture shown in figure 3.7 which is based on a dynamic control of the charge on the gate capacitance of the M1 output transistor and offers no static power consumption and a very low-power consumption in dynamic mode.

The dynamic controlled level-shifter circuit driven by a digital pulse strobe signal STR. When STR goes high, one of the two transistors M3 or M5 (according on the logical value of the input signal) carries an I_{input} current (ISTR1 for M3 and ISTR2 for M5) causing a voltage drop over M4 or M6 respectively. In this situation, when the input signal is a "0" bit and the strobe signal is high the voltage drop across M4 turns on M7 and M1 is switched off. When the input signal is a "1" bit and the strobe signal is high the voltage drop across M6 pulls down the gate potential of M1 (through M8) and consequently M1 is turned on. When the strobe signal STR goes low, M3

and M5 are switched off the voltage drop across M4 and M6 is reduced to about 1V turning off M7 and polarizing T8 inversely. Hence, M1 becomes electrically isolated from the rest of the level-shifter circuit. Using this approach the charge that was previously stored on its gate capacitance during the STR pulse remains unchanged until the next STR pulse is applied. Finally M11, M12 and M13 keep M7 transistor into a deep cut-off region (when M7 is switched off) avoiding any leakage discharge of M1 due to sub-threshold current in M7 (Doutreloigne et al.).

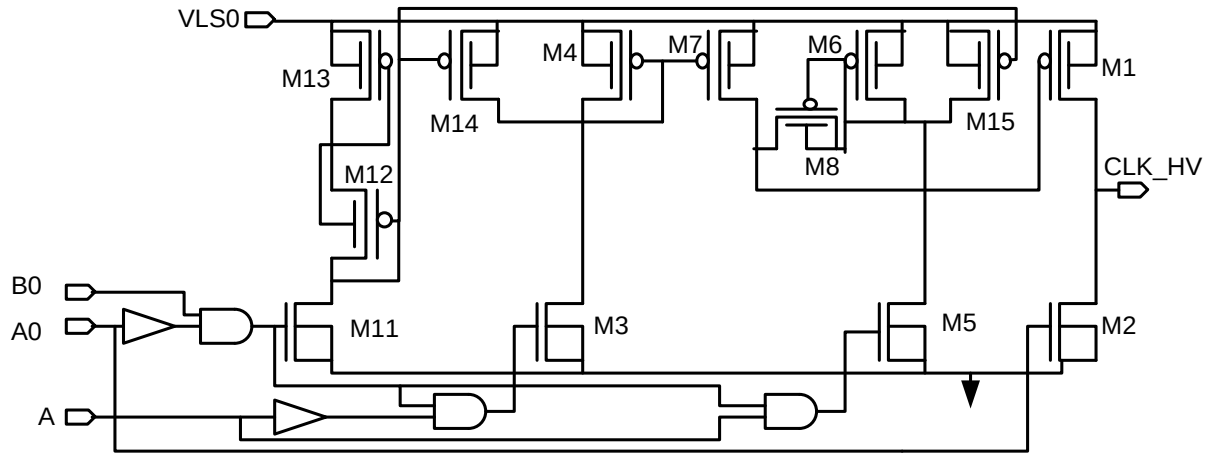


Figure 3.7: Dynamically controlled high-voltage level-shifter design (Doutreloigne et al.)

Note that this unique strategy of using the gate capacitance of M1 transistor as a storage capacitor and updating its charge at the rhythm of a strobe signal that is synchronized to the data flow yields an enormous reduction in power dissipation if the duration of the STR pulse can be kept very small compare to the duration of one bit of input data since power is consumed only during strobe pulse.

Although the dynamically controlled level shifter circuit of figure 3.7 works well, it has one drawback. It needs the generation or presence of strobe STR signal in order to drive properly the switching activity of the level shifter circuit. This means that there must be some digital control

unit or even a microcontroller dedicated to such purpose. This would increase the power consumption in the total power efficiency (Saiz et al, 2011).

In order to overcome this drawback, a simple modified version of the dynamically controlled level-shifter based on the use of the non-overlapping cells is proposed in this thesis work leading to the development of a dynamically controlled level-shifter circuit with a self-generation process of the strobe signal.

3.4.3 Self-generating STR level-shifter

The self-generating strobe signal dynamically controlled high-voltage level shifter circuit is based on the use of the developed non-overlapping clock generator cell. Using this cell, it is possible to obtain easily a none-overlapping clock pair (A_0 and B_0 signals) from a primary clock signal (A). Then using A, A_0 and B_0 signals it is very easy to generate a strobe signal STR0 by just modifying the original level-shifter circuit developed by Doutreloigne et al. in the way shown in figure 3.8 and adding some logic gates combining A, A_0 and B_0 as input signals. The sizing process of the self-generating strobe signal level-shifter schematic has been carried out taking into account that the operating switching frequencies of the developed charge pump circuits could be in the range of 100 KHz to 200 KHz (G. Kar et al, 2012).

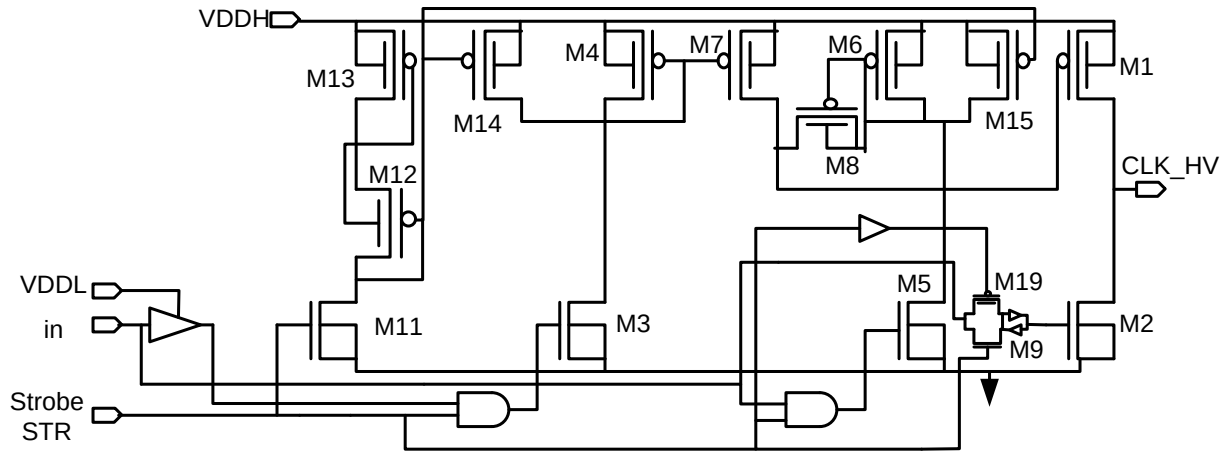


Figure 3.8: Schematic of the modified dynamically controlled high-voltage level-shifter.

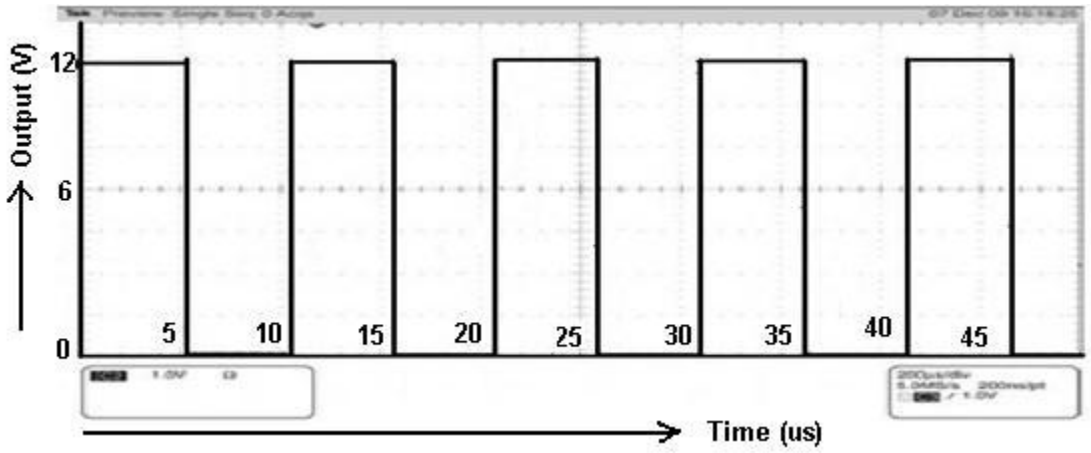


Figure 3.9: Experimental result of the modified dynamically controlled high-voltage level-shifter

3.5 Design and Implementation of Charge Pumps

Because of the high efficiency and small area, Pelliconi circuit topology (Pelliconi et al, 2001) has been used for the charge pump. Also this design has been adopted and tested by TELEDYNE DALSA high-voltage CMOS process (Ethier et al, 2009). As illustrated in Figure 3.10, MOS transistors are used as switches to transfer the charges from one capacitor to another at each cycle. The transistors are separated from the p-epitaxy substrate by deep N-well in 0.8µm technology and by T3 isolation-well in 0.13µm technology.

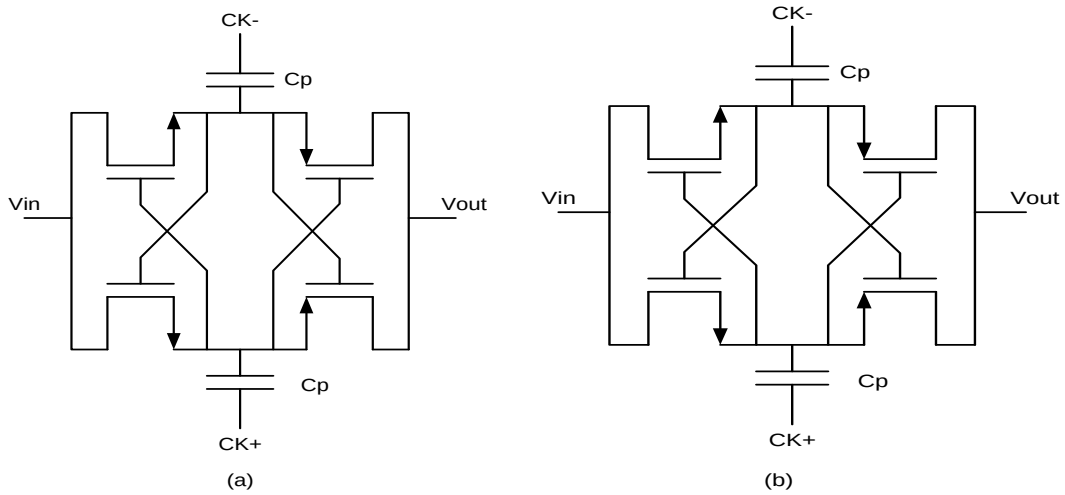


Figure 3.10: (a) Positive Charge Pump Block. (b) Negative Charge Pump Block.

For the design in 0.8 µm technology, external capacitors have been used because of the size of the capacitors (1µF). These large size capacitors have been used to facilitate large load (in the range of 1~2mA). Sizes of the transistors used are 600µm/2µm for NMOS and 1000µm/2µm for PMOS transistors. For 0.13 µm technology, the size of the capacitors used are 30pF and the transistor size used are 100µm/1µm and 200µm/1µm for NMOS and PMOS respectively.

The positive charge pump is composed of two cascaded stages with the supply voltages as 3.3V (figure 3.11). The first stage generates 6.6V from the supply voltage which is used as the supply voltage for the high voltage level shifters to generate clock signals of 6.6V amplitude. These clock pulses are then used in the second stage to produce 13.2V in the output (G. Kar et al, 2012).

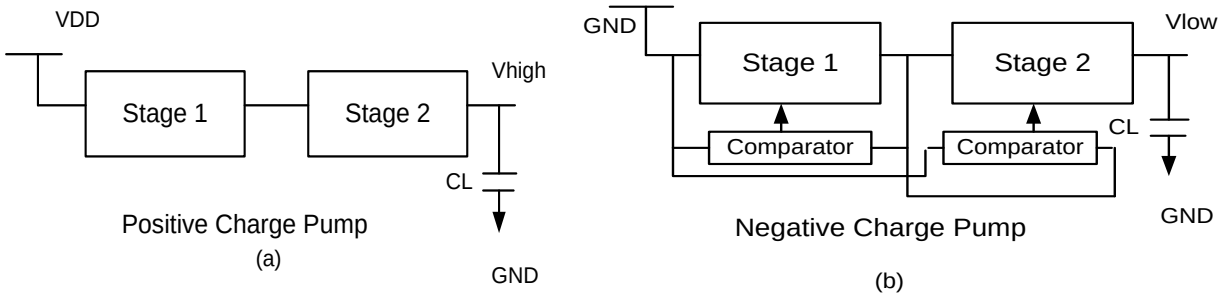


Figure 3.11: Stages for positive (a) and negative (b) charge pump (G.Kar et. Al, 2012)

According to (Ethier et all, 2009), negative voltage can be generated simply by switching the position of the P and N transistors in the design of the positive charge pump (figure 3.10) but other published experimental results of (Nadeau et al, 2006) confirmed that latch-up is triggered in negative charge pump. Ethier et al (Ethier et all, 2009) solved the latch-up problem by connecting the body of the PMOS transistors of the negative charge pumps to the ground and thereby keeping the voltage to the highest. The process has been described in figure 3.12.

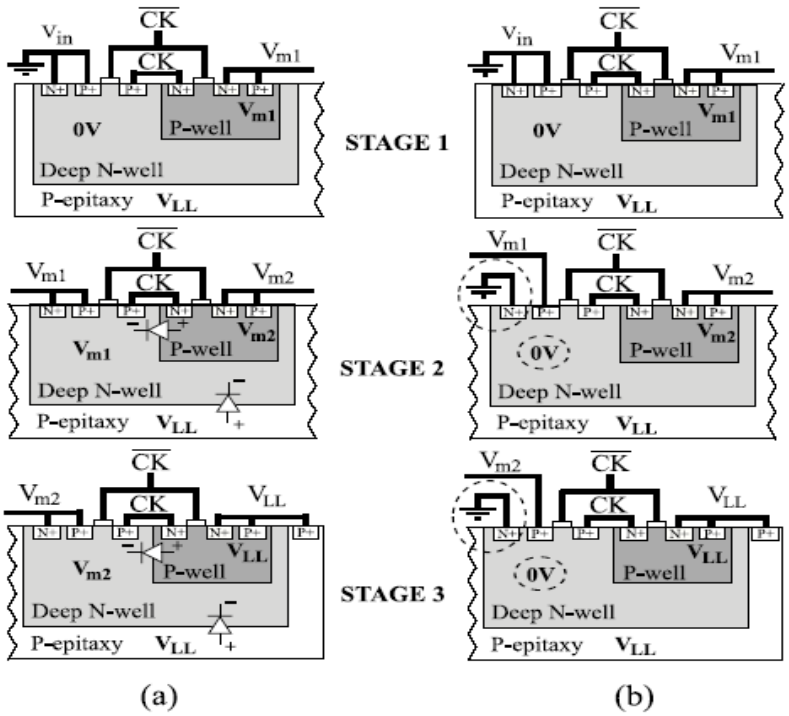


Figure 3.12: Side view of the substrate showing the well connections of the negative charge pump. (a) Deep N-wells tied to the source of the PMOS devices with the possible forward-biased PN junctions shown, (b) Deep N-wells tied to the ground (Ethier et all, 2009)

Investigations have led to the following observations. Before the negative charge pump is enabled, the P-epitaxy substrate is connected to V_{LL} which is near 0 V. During the first charge pumping cycles, there are short moments for which the interstate voltages of the negative charge pump (Vm1 and Vm2 in Fig. 3.5b) are lower than the substrate voltage VLL. This is due to the pumping mechanism that moves the charges at a rate of one stage per clock cycle. It thus takes a few cycles before the output voltage gets lower than Vm1 and Vm2. If the sources of the PMOS transistors are connected to their bulk, i.e. to the deep N-wells as it is shown in Fig. 3.5a, latch-up circuits will then be triggered at start-up. To prevent this, the deep N-wells of the negative charge pump are all tied to the ground as in figure 3.12 (G. Kar et al, 2012).

The same strategy has been adopted for the design in 0.8µm technology. But 0.13µm technology has some limitations regarding the channel breakdown voltage. The highest channel breakdown voltage for 0.8µm technology is about 25V whereas its 7.7V for 0.13µm technology. To overcome the issue of latch-up, a comparator (figure 3.13) has been used to facilitate the highest

voltage to the body of the PMOS transistors comparing the input and output voltages of that stage. When I_{out} =0, the voltage gain can be approximated by the following expression: $\Delta V = V_{dd}*C/(C+C_{par})$ which is reduced by Iout*R_{out} if $I_{out} \neq 0$. Cascading stages give:

$$V_{out} = V_{dd} + n.\ \Delta V. \qquad (3.1)$$

I_{out}=load current, V_{dd}=supply voltage, C= charging capacitor, C_{par}=parasitic capacitor and R_{out}=output load.

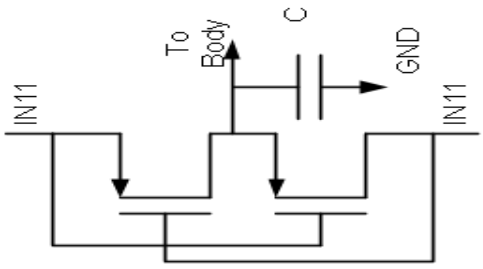


Figure 3.13: Circuit diagram of the comparator that is used in the negative cycle

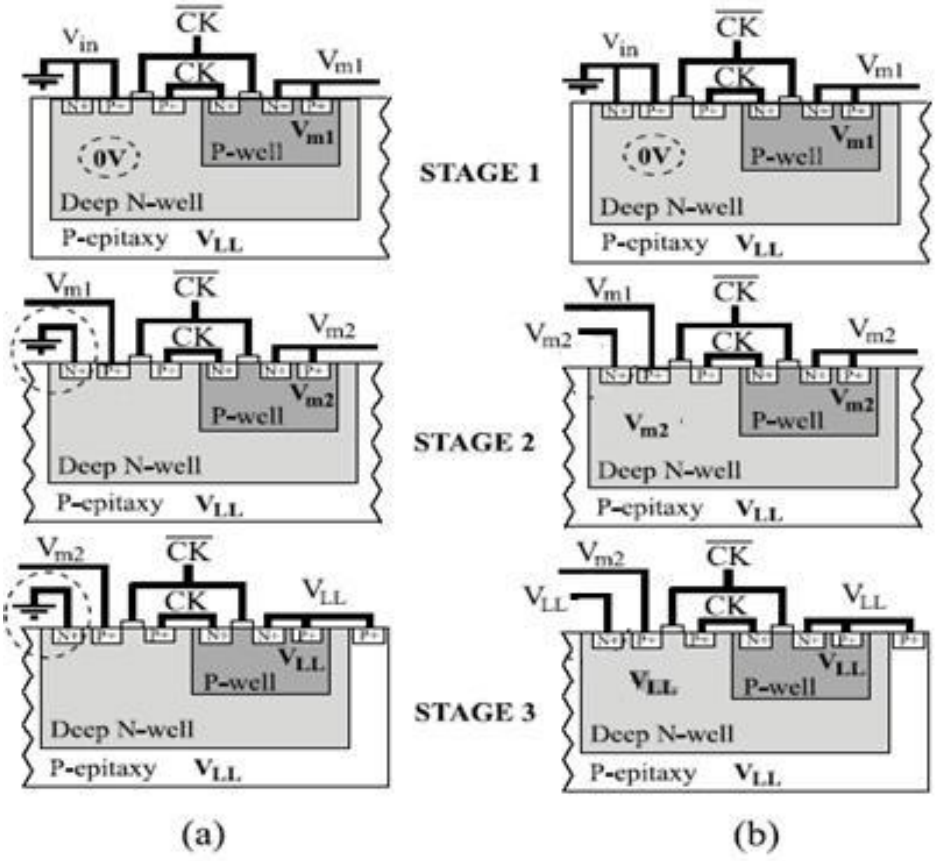


Figure 3.14: Side view of the substrate showing the well connections of the negative charge pump for 0.13µm CMOS technology.

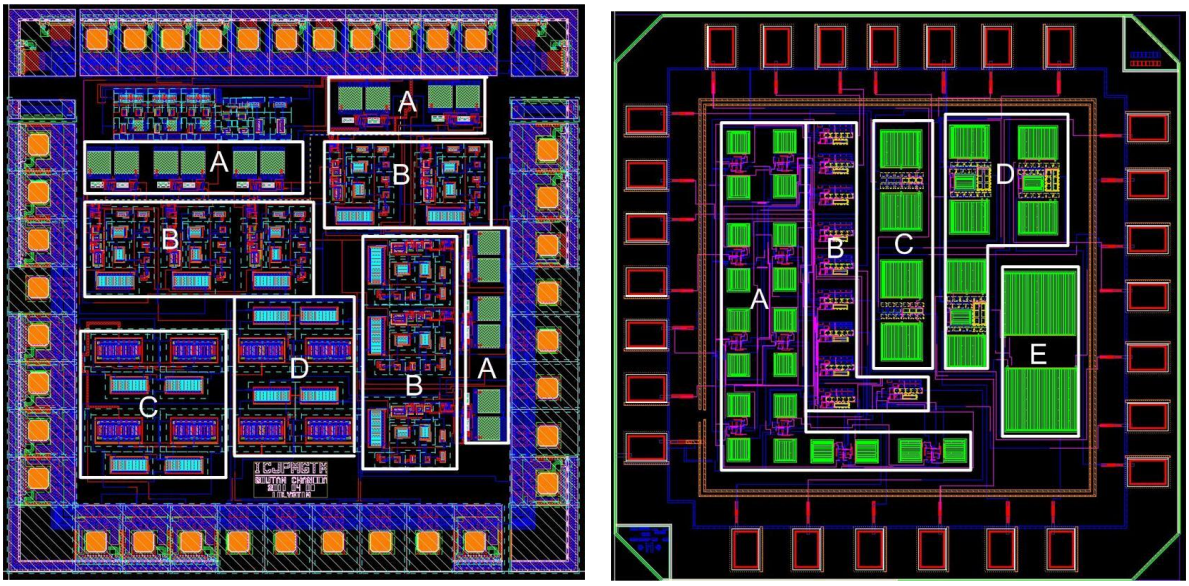
Because of the technical difficulties of 0.13 µm CMOS technology, design has been given more attention to achieve desired results. Unlike high voltage technologies, the junction breakdown voltage of this technology is very low. Even though we have used high voltage transistors for design, the theoretical junction breakdown voltage of these transistors is 7.9 V although it occurs before the junction voltage reaches the above voltage. Because ours is a voltage doubler design, the method that we applied for design in 0.8 µm technology, could not be applied here. For 0.8 µm design, the output of the first stage has been used for input of high-voltage level shifters to boost the output voltage of the level shifters before it is fed to the charge pumps. But because of the breakdown voltage issue, that method has not been used in low voltage design. Instead, one stage has been added in the negative charge pump section to compensate the output voltage. Also, a comparator has been added for every stage of the negative charge pump which compares the input and output voltage of each stage and forces to provide higher voltage to the body (G. Kar et. Al. 2012).

T3 isolation-well in this technology has been used to isolate the substrate from the body of the transistors which allowed us to vary the body voltage to overcome latch-up. The isolation-well serves the same purpose of deep N-well separation of high voltage technology and thus allow variable body voltage. As shown in figure 3.14 different stages have been controlled dynamically by using the comparator so that junction breakdown voltage doesn't occur.

Because of generating high negative voltage, the usual ESD provided by both TELEDYNE DALSA (0.8 µm) and IBM (0.13 µm) could not be used for the design. The usual ESD provides protection up to 3.3 V which is much lower than our output voltages. Also, with some modification we could increase the protection upto 7.5 V. But because the output of our chip is more than 7.5 V, we decided not to use ESD protection and take necessary caution during test phase.

3.6 Post layout simulation

The Layout of the implemented circuits in both 0.8µm and 0.13µm CMOS technology is shown in figure 3.15. The dimensions of the chips are 3mm x 3mm and 1.5mm x 1.5mm respectively.



ICJPMGTM (0.8µm) ICGPMGPT(0.13µm)

Figure 3.15: Layouts of the proposed charge pumps. ICJPMGTM (design in 0.8µm CMOS technology, A= Non-overlapping clock generator, B=High voltage level shifter, C=Positive charge pump, D=Negative Charge pump) and ICGPMGPT (design in 0.13µm CMOS technology, A=Non-overlapping clock generator, B=High voltage level shifter, C=Positive charge pump, D=Negative charge pump and Comparator, E=Load Capacitors for positive and negative charge pumps)

Charge pump output voltages of the simulated and experimental results are shown in figure 3.16 and 3.17 respectively for the design in 0.8µm technology. The output for the design of 0.13 µm technology has been shown in Appendix. The pumping clock frequency used is 100 kHz. For simulation result output voltages with no load are 12.91V and -12.87V and with 1mA load are 11.81V and -11.71V for positive and negative charge pumps respectively.

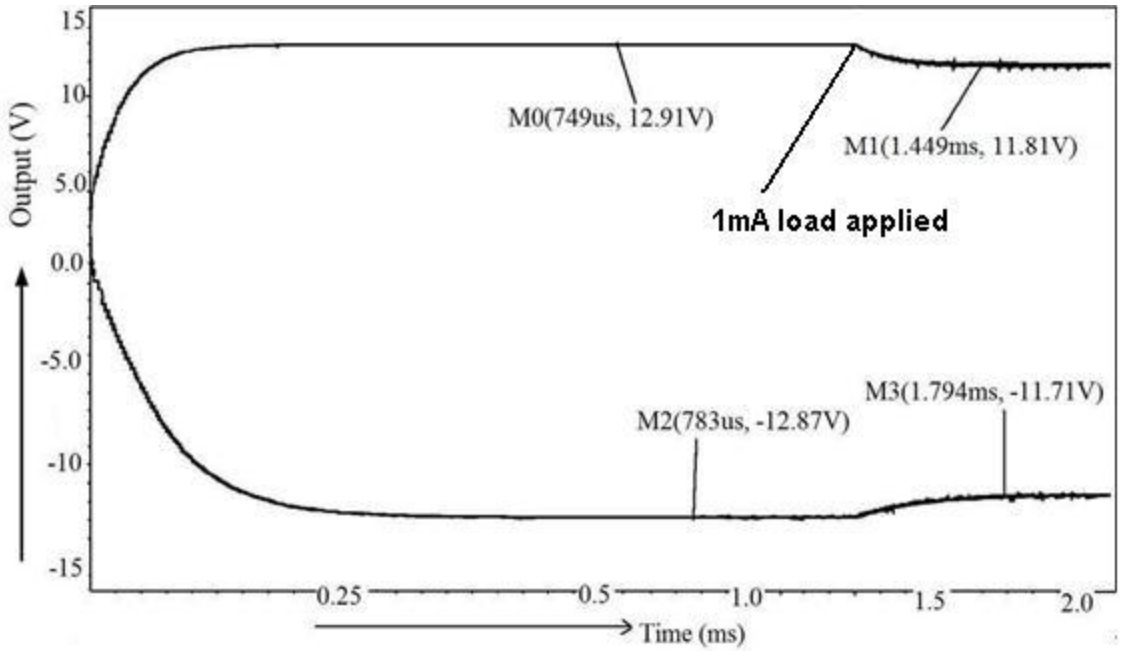


Figure 3.16: Simulation result of the output voltage with no load and 1 mA load.

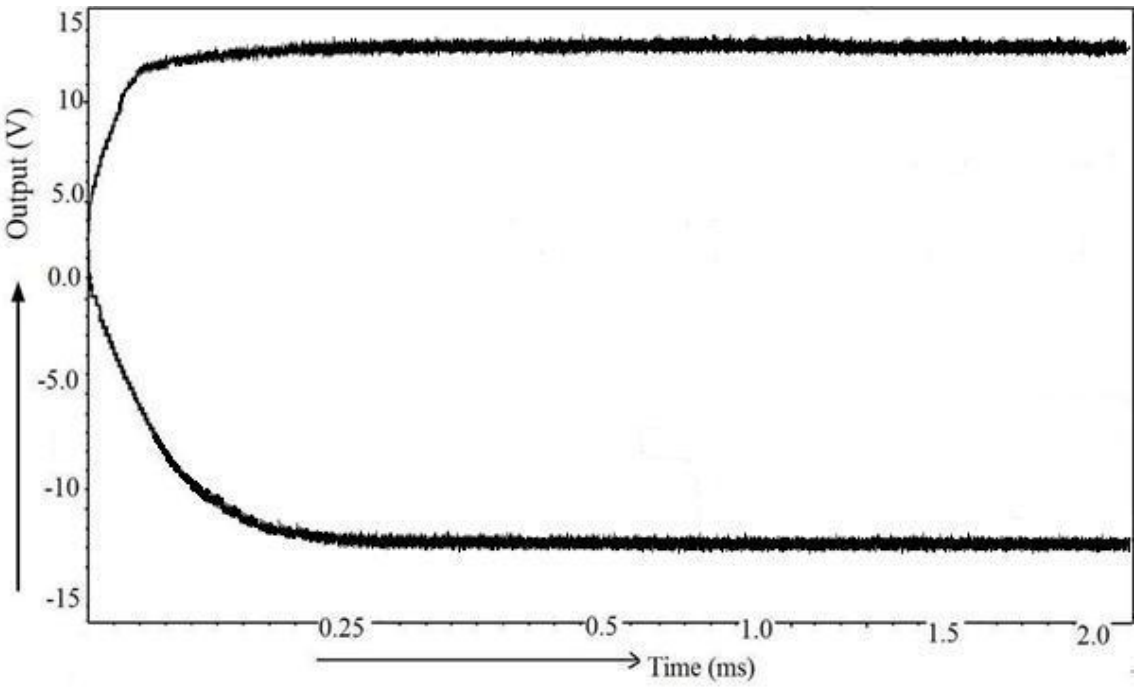


Figure 3.17: Experimental result of the output voltage with no load.

Output ripple with 1mA load is 311mV for positive and 332mV for negative charge pump. Output voltage and efficiency with different load is shown in figure 3.18 and figure 3.19.

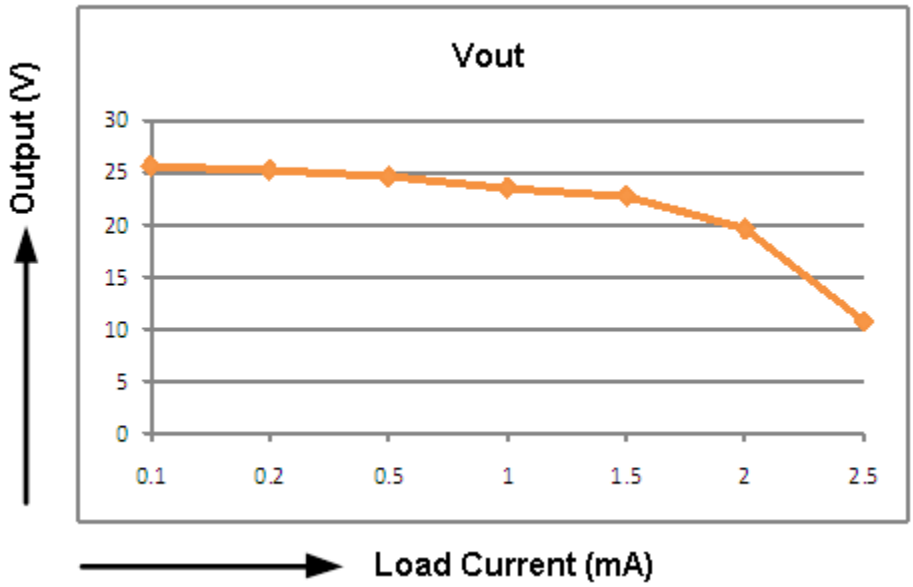


Figure 3.18: Output voltage drop with the increase of load current

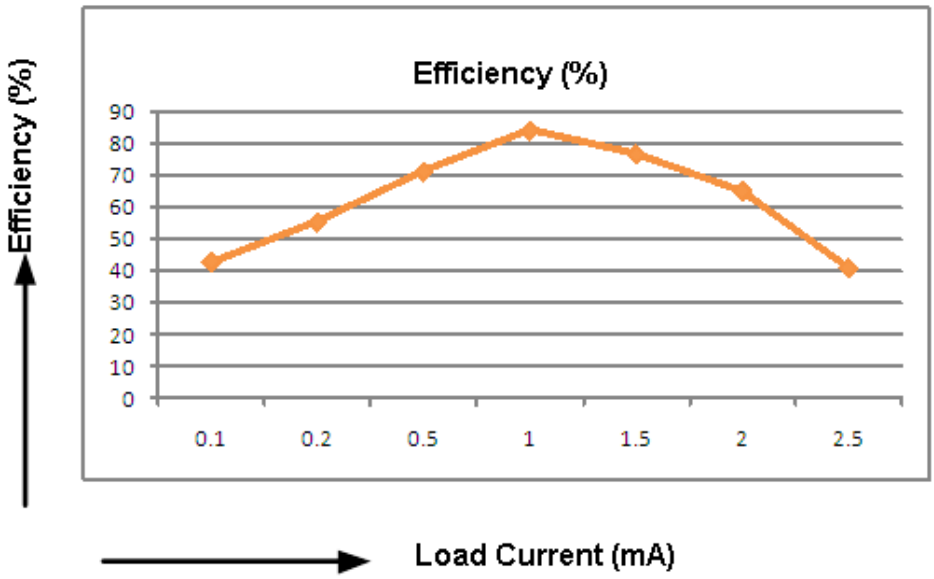


Figure 3.19: Efficiency of the charge pump with respect to load current increase.

For the design in 0.13µm with no load, outputs are 10.11V for positive and -10.34V for negative charge pump, whereas with 250µA load these output become 9.4V and -9.56V respectively. Static power consumption for design in 0.8µm has been found equal to 3.73mW, whereas for the design in 0.13µm it is 0.8976mW. This is to note that the designs have different transistor sizes

and different load capacities. For the design in 0.8µm CMOS technology, PMOS and NMOS transistors are much larger to drive the load of more than 1mA. On the other hand for 0.13µm design, the transistor sizes are smaller because this charge pump drives only 250µA load current. The load capacities for both designs have been measured. For the design in 0.8µm, the maximum load capacity is 2mA and for 0.13µm, the maximum load capacity is 500uA. Maximum efficiency for 0.8 and 0.13µm design has been measured as 84.32% and 85.2% respectively. Figure 3.9 shows the output of 0.8 µm CMOS technology. All the related outputs of 0.13 µm CMOS technology have been included in the Appendix.

3.7 Comparison of results

Comparison between the two designs implemented in 0.13 µm and 0.8 µm CMOS technologies are presented in this section (Table 3.1). Also the comparison with other works have been presented in Table 3.2

Table 3.1: Simulated features for both charge pump designs

CMOS Technology	Design 1(ICJPMGTM)	Design 2 (ICGPMGPT)
No load output voltage	25.78 V (+12.91 V to -12.87 V)	20.45 V (+10.11 V to -10.34 V)
Load for best performance	1mA to 1.2 mA	200µA to 300µA
Maximum load	2mA	500 µA
Output ripple	Average 300mV	Average 100mV
Maximum efficiency	84.32%	85.2%
Static power consumption	3.373mW	0.8976mW

Table 3.2: Parameters and result comparison.

Reference	Nadeau et al, 2006	Ethier et al, 2009	Wen et al, 2011	This work (ICJPMGTM)	This work (ICGPMGPT)
Process	3 µm	0.8 µm	0.35 µm	0.8 µm	0.13 µm
Generated Voltage	±5 V	±9 V	+10.3 V (3 stages)	±13 V	±10 V
Maxm Stim. Current	127 µA	200µA	N/A	1mA	250µA
Output Swing	<10 V	17.56 V	10.3 V	24.52 V	18.96V
Static Power	N/A	27.2 mW	N/A	3.73 mW	0.897mW
Result type	Experi-mental	Post Lay-out	Simulation result	Experimental	Experimental
Integration	External supply	Fully Integrated	N/A	External Capacitor	Fully Integrated
Size (mmXmm)	N/A	2.87 X 2.93	N/A	3 X 3	1.5 X 1.5

The comparison result clearly shows that the designed charge pumps takes relatively low area and generate much higher voltages than any other works. The power consumption has very low and it is lower for 0.13 µm technology understandably.

3.8 Conclusion

The proposed designs are intended to be used for intracortical microstimulation for visual prosthesis but it can be used for other implantable devices also depending on the voltage and load. One of the designs is fully integrated and the other has external capacitors to ensure the granted silicon area. Clock generators have not been used inside the chip to ensure low power consumption because it continues to run even when the charge pumps are not enabled and thereby consumes static power. This clock signals should be external to be able to have the control and low-power consumption. The chip designed in high voltage technology is intended to be used in a visual prosthesis system and the one designed in low-voltage technology is designed to ensure the possibility of using low- voltage technology for the whole system and thereby using only one chip for the whole implantable device. Although the high-voltage switch design in this technology is yet to be done to ensure full compatibility which is yet a challenge. If any system needs very low ripple in the output, regulators can be used to ensure low output ripple.

CHAPTER 4

GENERAL DISCUSSION

A discussion forging links between the different chapters of this master thesis is briefly made here. In addition, imperfections observed during tests of chips manufactured and have not been treated in Chapter 3 are also detailed.

4.1 Discussion on the whole system

The primary goal of this thesis is the implementation of a high-voltage generation to provide supply voltage for visual prostheses applications. These voltages, that is to say would trigger the excitation when current pulses are provided to the visual cortex nerve tissue of cortical tissue that while requiring less energy. Circuits made to produce such stimuli were designed following a critical review of the literature. Pulse generators have subsequently not been integrated into a chip in order to reduce their power consumption and make implantable. Given the deadlines for the manufacture of integrated circuit, the regulator design has been omitted, but it has still been designed and simulated. The results show that the output voltages produced by the chip generates voltage satisfactorily to the theoretical forms described in the literature. The energy required to produce these voltages are much smaller than that found in other literature.

In order to inject the current pulses described above through the high impedance of the interface electrode-tissue, an output stage to a high-voltage has also been designed and built. The core of the chip is composed of two charge pumps based on the design proposed by Pelliconi, one of several architectures found in the literature. The experimental measurements show that the voltage excursion reached a level to stimulate the tissues with a high level of current through high impedances. The power consumption is a bit higher than expected. However, it is much lower than all other designed proposed before. The following section discusses defects noticed

during the experimental tests of two integrated circuits. This discussion is intended as a supplement to Chapter 3.

4.2 Imperfections in chips manufactured

During laboratory validation circuits manufactured, some defects were observed without compromising the proper functioning of the chip and the achievement of results.

First, transient pulses (glitches) can be noticed in the output of the stimuli, as was shown in Figure 3.10. These current peaks are a result of the charge injection caused by the many switches present in the integrated circuit, particularly in the non-overlapping clock generators and the high-voltage level shifters. They can reach considerable amplitudes depending on the intensity of stimulation, we have used 3.3 V as supply voltage but we can use the usual 2.5 or 1.8 V also but the amplitude of the generated voltage will be lower than that we receive when we apply larger supply voltage. The design is a voltage doubler in general and it normally doubles the input voltage. So, the more the input voltage will be, the more will be the output voltage. If the glitch creating circuits are not totally eliminated, these transient pulses are typically reduced by adding a dummy switch in series in order to absorb a fraction of the charge released. Another possible solution is the use of more complex switches comprising circuitry eliminating glitches (Song et al., 2005).

A second abnormal stimulus generator is the reduced load bearing capacity with respect to what has been obtained by simulation. At full scale, the maximum load measured experimentally is only 1.5 mA. Several reasons may explain this imperfection and it is difficult to identify with certainty the true cause. By cons, depending on the results, it can be said that the fault is probably in the chip that has been manufactured. According to CMC Microsystem, when the chip was fabricated, for a whole batch, there were some imperfection found with respect to the Vth value and the doping. Because in the experimental result, we found reasonable good result, the chip was not fabricated for the second time.

Then, it was observed that the output voltages are highly unstable in amplitude. Indeed, for fixed stimulation parameters, we found good result for the first two experiments for 4 out of 6 chips that had been tested, but after a certain number of tests, the output voltage started getting low and we found almost 0 voltage output. This is due to the fact that to generate high voltage, we encounter an issue with the ESD protection. Because of the voltage tolerance capability of the ESD design provided by CMC, we decided to design the chip without any ESD protection in the output stages. This resulted in great difficulties while we performed the testing and found different results in different testing phase. To get rid of the issue, we need to look for a solution to design an ESD for our purposes and check if this issue can be solved or not.

On the output stage, the activation of the clock signal by triggering charge pumps causing undesirable behavior. Indeed, when it goes from 0 to 1 while the circuit is powered, the DC-DC converters do not work, that is to say, the VHH and VLL tensions are maintained at their resting value. Worse, a substantial increase in power consumption is measured, it reached about 230 mW. This behavior suggests a problem of non-destructive parasitic thyristor is triggered. This phenomenon is characterized by the junctions between different regions of N and P, thus forming two BJT. According DALSA ridges 600 mV is sufficient to trigger (TELEDYNE DALSA Semiconductor, 2005). When enabled, this circuit parasite forms a positive feedback that generates a large leakage current in integrated circuit substrate. In this state, the clock generator is indeed functional, since noise whose frequency corresponds to that of the oscillation is about 5 KHz, measured at the output of the charge pump. To start properly generating high voltages, just feed the output stage while the signal is already active. The behavior of the chip corresponds to what is expected. Triggering thyristors parasites affects the output stage in a specific case and does not preclude the taking of experimental measurements.

In the same vein, during normal operation of the charge pumps, the power consumption of the output stage is a bit larger than what is expected. Experimentally, the integrated circuit dissipates 3.96 mW, nearly 6.1% more than measurements obtained in simulation which stood at 3.73 mW. In this context, a decrease in the effectiveness of DC-DC converters up to 6% is expected compared to simulations. This efficiency, which is impossible to calculate in the laboratory since there is no power supply pin dedicated to charge pumps to measure its specific power

consumption. The weakness of these values is due to the fact that the design of charge pump was instead focused on maximizing VHH and VLL tensions. In addition, the pump capacitors converters are fully integrated, low-value, corresponding parasitic capacitances have a major impact on the loss of efficiency.

Finally, experimental measurements have shown the presence of noise in the whole circuit, but mainly on the supply voltages. This noise comes from several sources. First, the development platform for Xilinx Spartan-3E, which is implemented on the digital interface for programming the stimuli generator, significantly contaminates the circuit ground. Indeed, despite capacitive decoupling insulation, considerable noise, caused inter alia by the clocks of 5 KHz and 50 present on the platform, is inserted into the test rig. Then, despite efforts in the design of the masks of the stimulus generator, it seems that the controller injects noise stimulation in the analog part of the chip whose frequency corresponds to that of its clock. The same phenomenon can be measured in the output stage, where the clock generator 5 KHz is integrated in the circuit. Amplifiers clock, some transistors have a few hundred microns wide, are the main source of noise at this level.

CHAPTER 5

CONCLUSION

This final chapter summarizes the completed work and corresponding results. In addition, based on the experience gained in this work, recommendations on the next steps to be performed are specified.

5.1 Summary of work

The project discussed in this study is a microstimulator dedicated to a visual intracortical prosthesis. In this context where the level of parallelism is considerable, the power dissipated by the stimuli represents a major contribution to energy consumption of the entire system. Few studies have focused specifically on the effectiveness of stimulation to excite biological tissues, but the results have been validated in simulation of neural models. The main objective of this master thesis is to implement a charge pump that can produce enough voltage so that constant current stimulation can be provided to the visual cortex. On the other hand, the second objective of this project is to produce that required output stage with as low power consumption as possible. It is thus possible to stimulate tissue through tissue-electrode interfaces whose impedance is very high. This integrated circuit will be joined together with a microstimulation system for functional experiments in vivo.

The charge pump chips will be a separate part of a complete microstimulation system. It will produce required voltage required to provide constant stimuli current to the nerve tissues. Because constant current stimulation is much desirable than constant voltage stimulation, it is required to provide sufficient voltage to maintain the constant current to the nerve tissues. Also, because of the mature of nerve tissues and the system being fully integrated, the power consumption of the system has to be in a desired level. Because the charge pump is the part that consumes most power than any other parts of the system, the power consumption of the charge

pump has to be as low as possible. The designed chips in both technologies consumes very small amount of power compared to any other previous work, this can be a suitable design to be integrated in the visual prosthesis system.

5.2 Recommendation for future work

This section lists recommendations for the next steps to take in the short or medium term for the realization of an implantable system next full meeting the objectives of departure.

Despite power consumption lower than other works and the chip developed in this project is fully functional, there is still room for improvement with respect to power consumption in the initial stage when the transition occurs from 0 to 1 in the clock generator. Applying RC delay circuits the consumption has been reduced significantly but still there is need of investigation to reduce or eliminate the initial power consumption. These tests should be carried out as a priority, because they are essential to the continuation of the project. The results obtained give indications on the direction to be followed by the project.

The glitches measured in the output stage are high compared to other works in the past. Although the glitches don’t affect in this project because the output voltage produced is higher than required, there are option for this charge pump circuit design to be used in other system where output glitch might cause issues. In those cases, a regulator can be used in the output stage to reduce the output glitches. This has not been attempted in this project but is recommended for future work for the design to be used in other systems. In the output stage, optimizations are required to improve the efficiency of the conversion of tension that has been neglected in this paper. In addition, it is essential to adjust some parameters such as pumping capacity and load, and clock frequency in order to increase the output current to support the increase in the number of channels. Given the significant variation of the current demand, architecture of adaptive charge pump could be interesting. In this type of circuit, the pump frequency is controlled in dependence of the load current so as to maximize the efficiency of charge transfer.

Finally because one of the main issues faced during testing is due to the fact that there was no ESD protection for the chip, it is necessary to design an ESD that can meet the requirement of the chip.

The design contained in this paper supports the generation of biphasic current without any modification in the current pulse generator because of the positive and negative output voltages. To avoid the release of toxic ions in faradaic electrochemical reactions, the two phases of stimulation must be equivalent load, which is usually done by paying attention to the matching of complementary circuits generating positive and negative currents. A more precise and therefore safer would be to close the loop by controlling the generation of the second phase with the aid of a measure of the charge injected by the first phase.

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Appendix

SCHEMATIC AND LAYOUT OF CHARGE PUMP IN 0.8 µm CMOS TECHNOLOGY (ICJPMGTM)

A-1 Top view of the chip ICJPMGTM

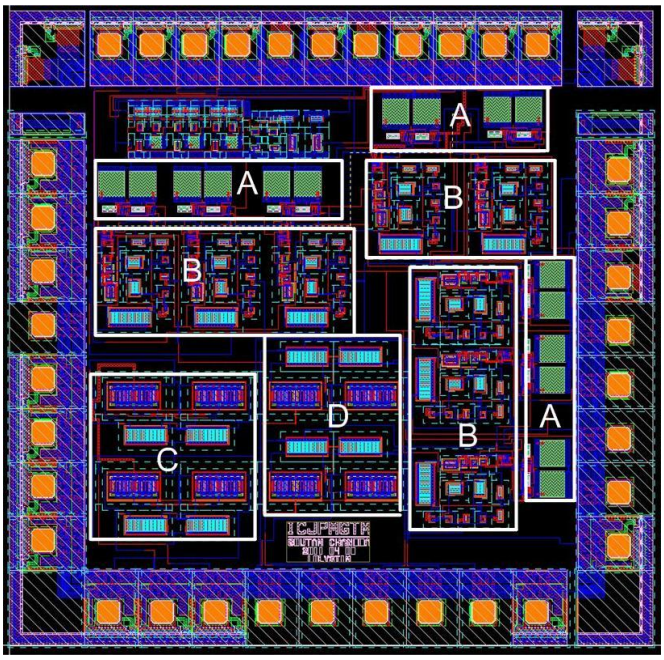

Figure A.1: Top view layout design of charge pump in 0.8 µm CMOS technology (ICJPMGTM)

A-2 Design Level (ICJPMGTM)

A-2.1 High-voltage level shifter

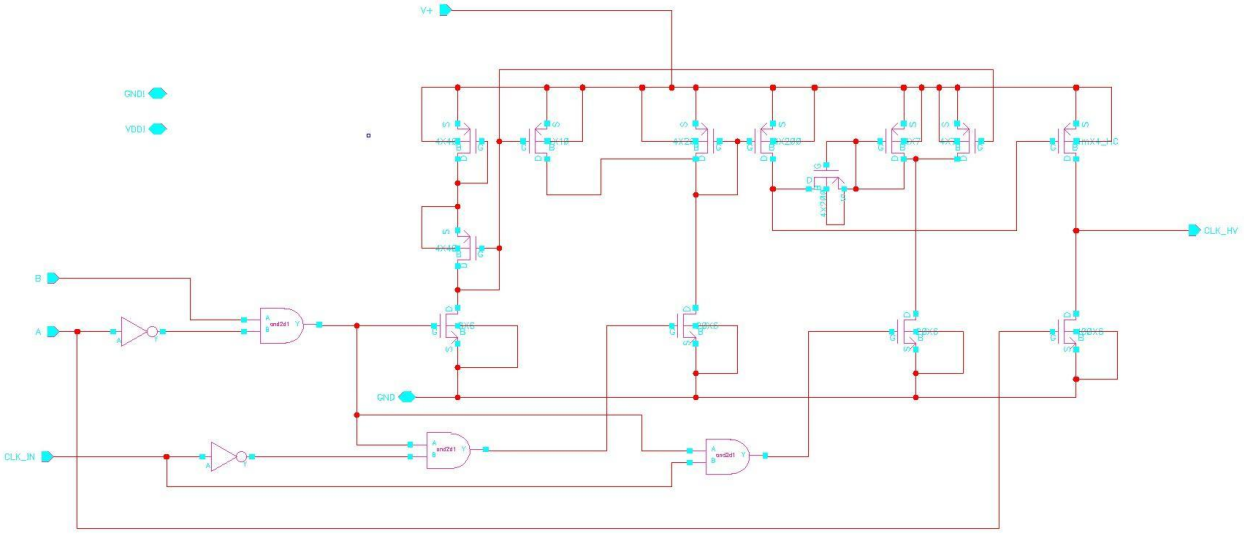

Figure A.2: Schematic of the high-voltage level shifter

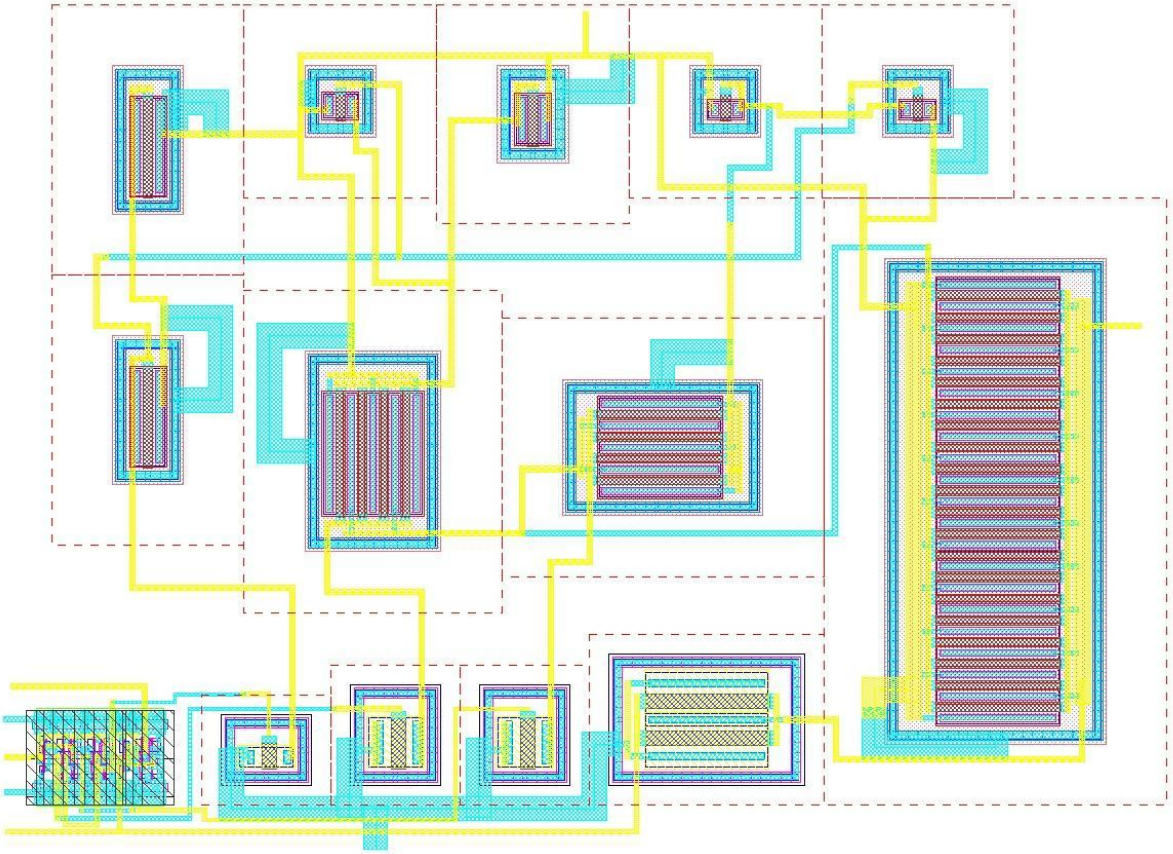

Figure A.3: Layout of the high-voltage level shifter

A-2.1 Non-overlapping clock generator

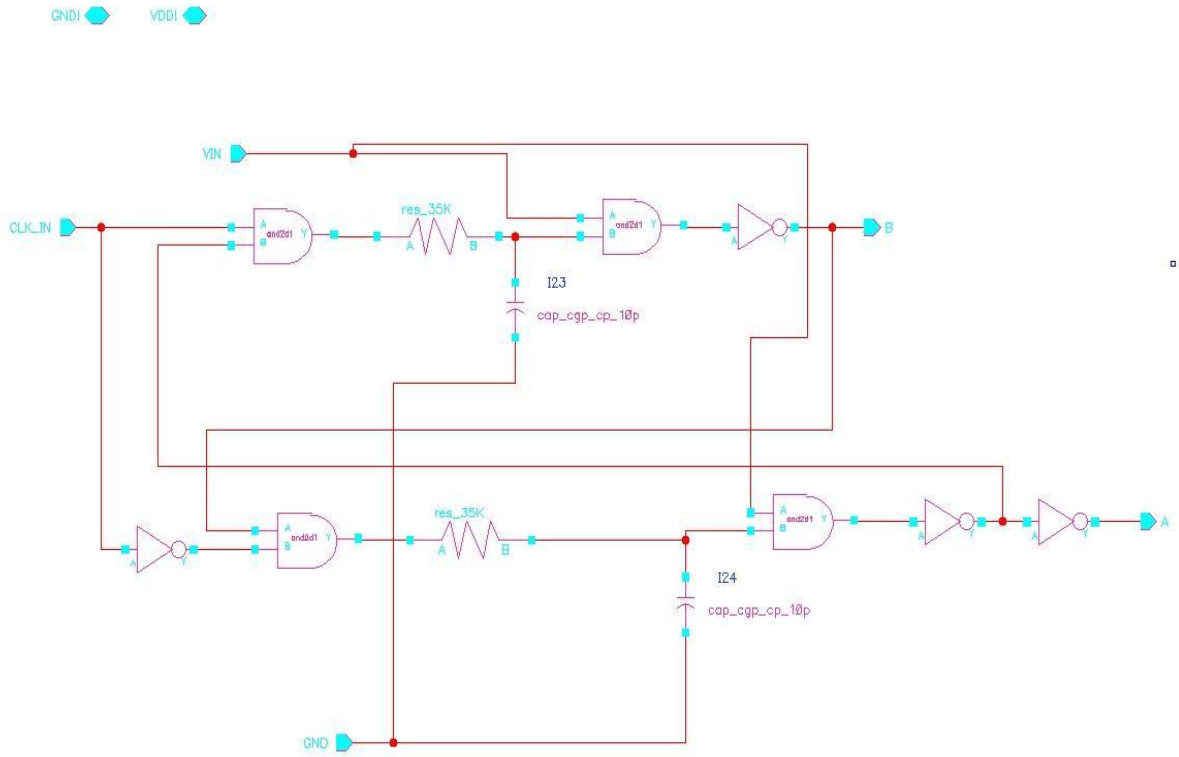

Figure A.4: Schematic of the non-overlapping clock generator

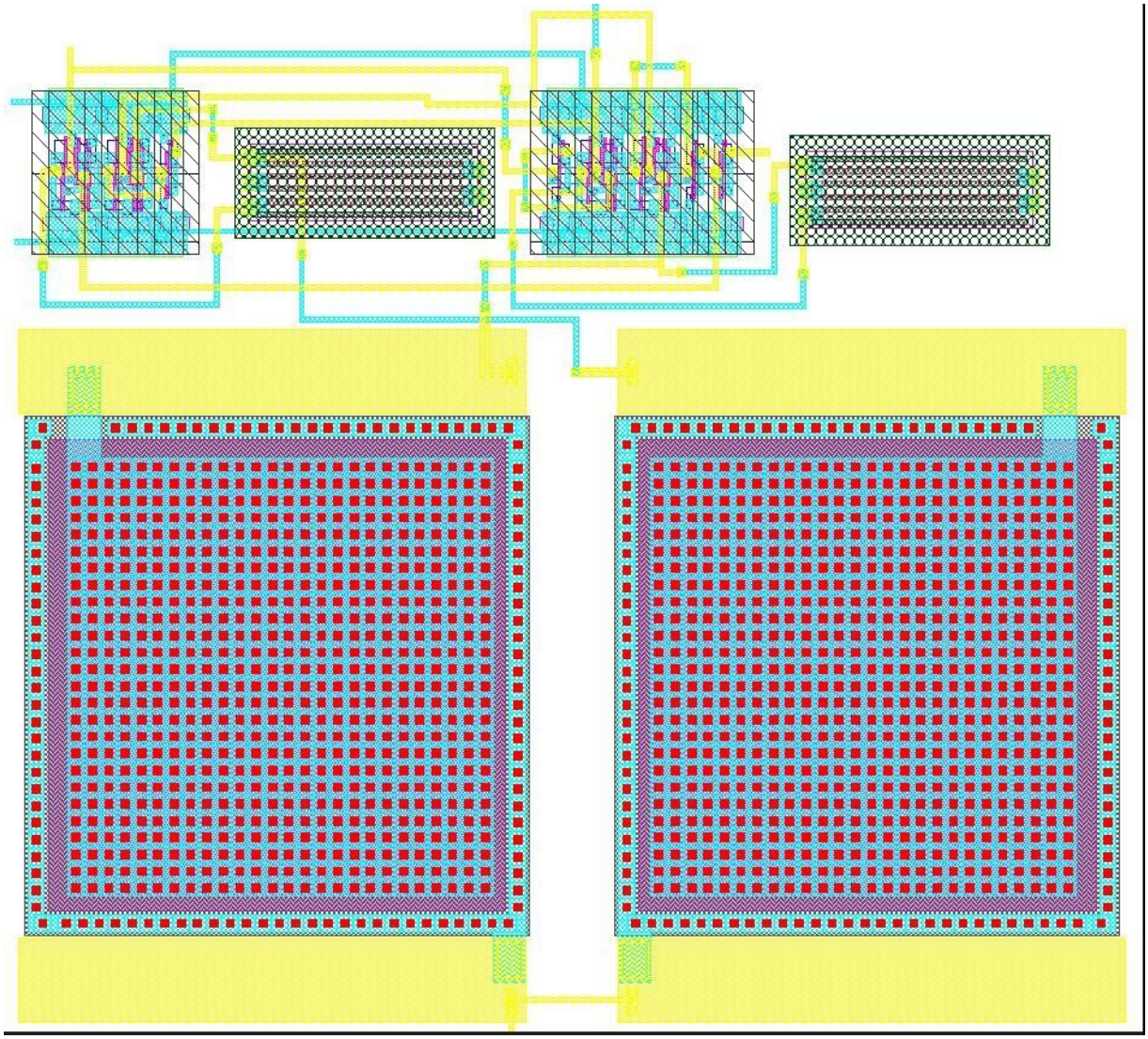

Figure A.5: Layout of the non-overlapping clock generator

A-2.1 Positive stage of the charge pump

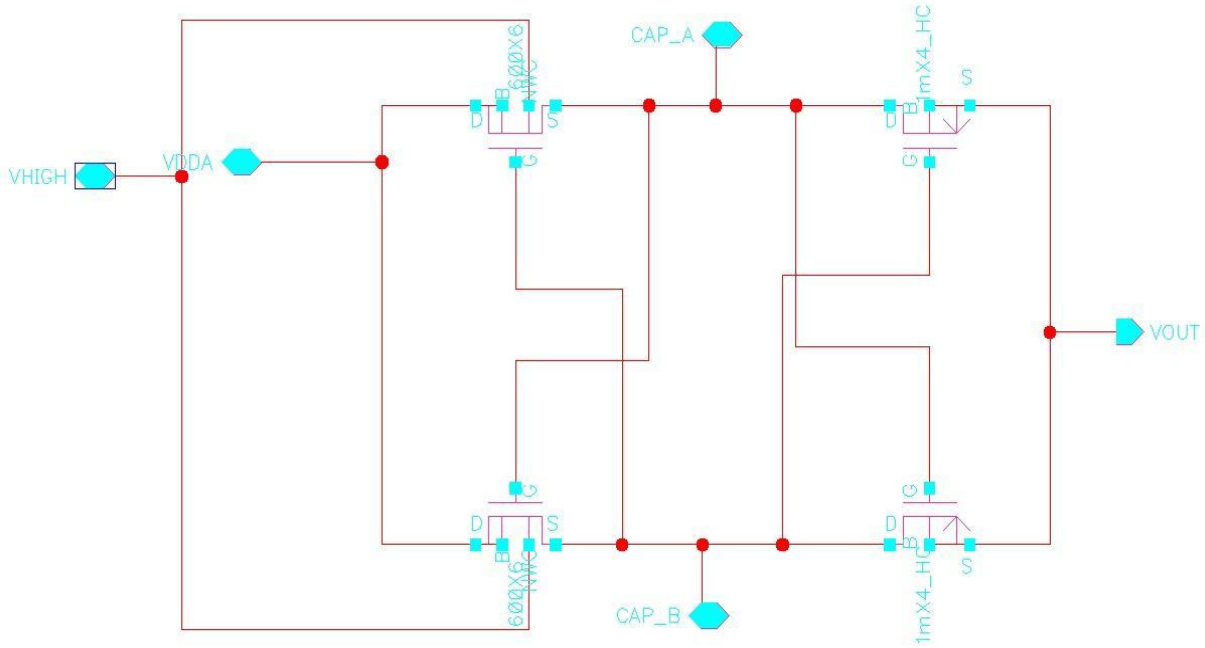

Figure A.6: Schematic of the positive stage of the charge pump

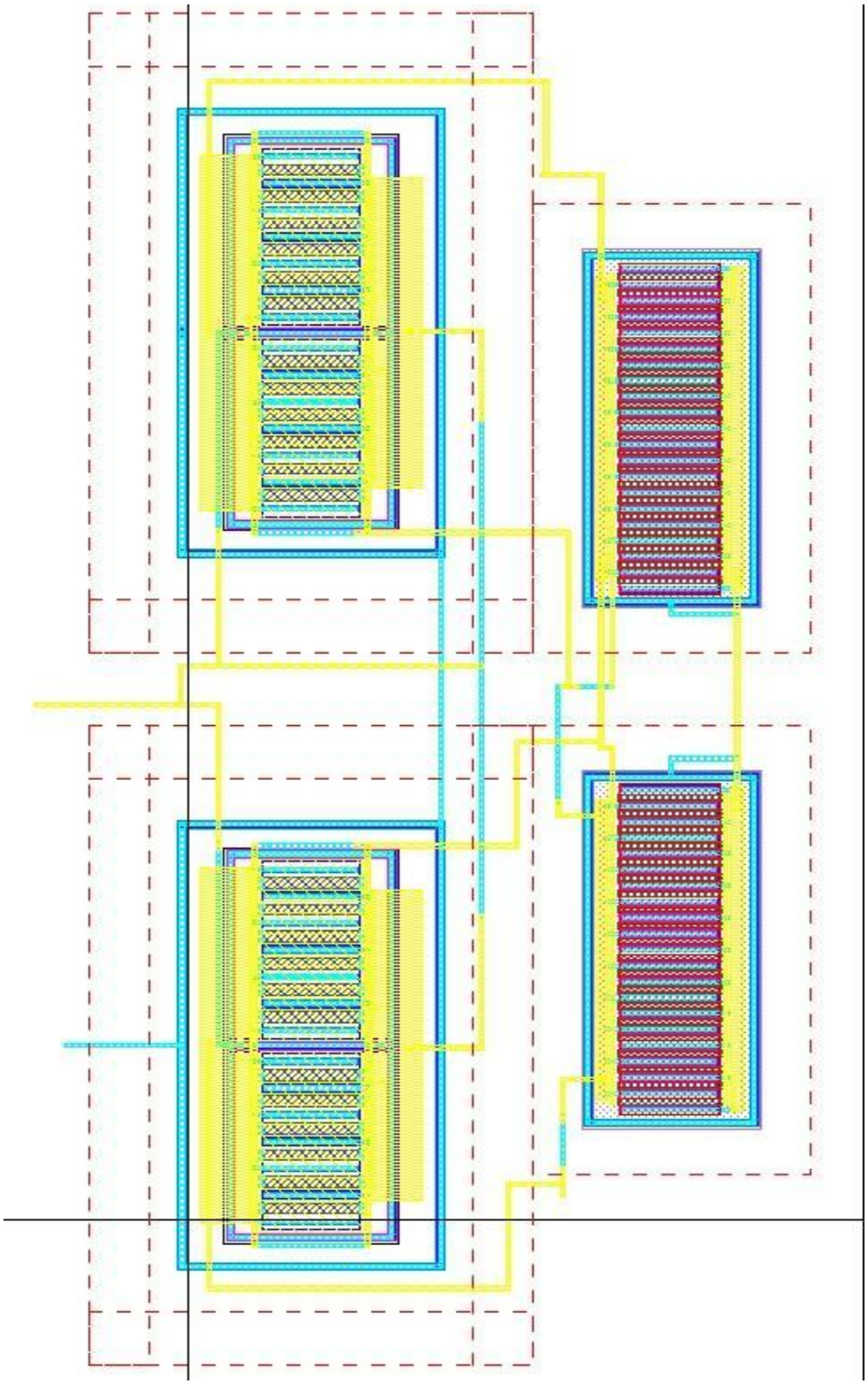

Figure A.7: Layout of the positive stage of the charge pump

A-2.1 Negative stage of the charge pump

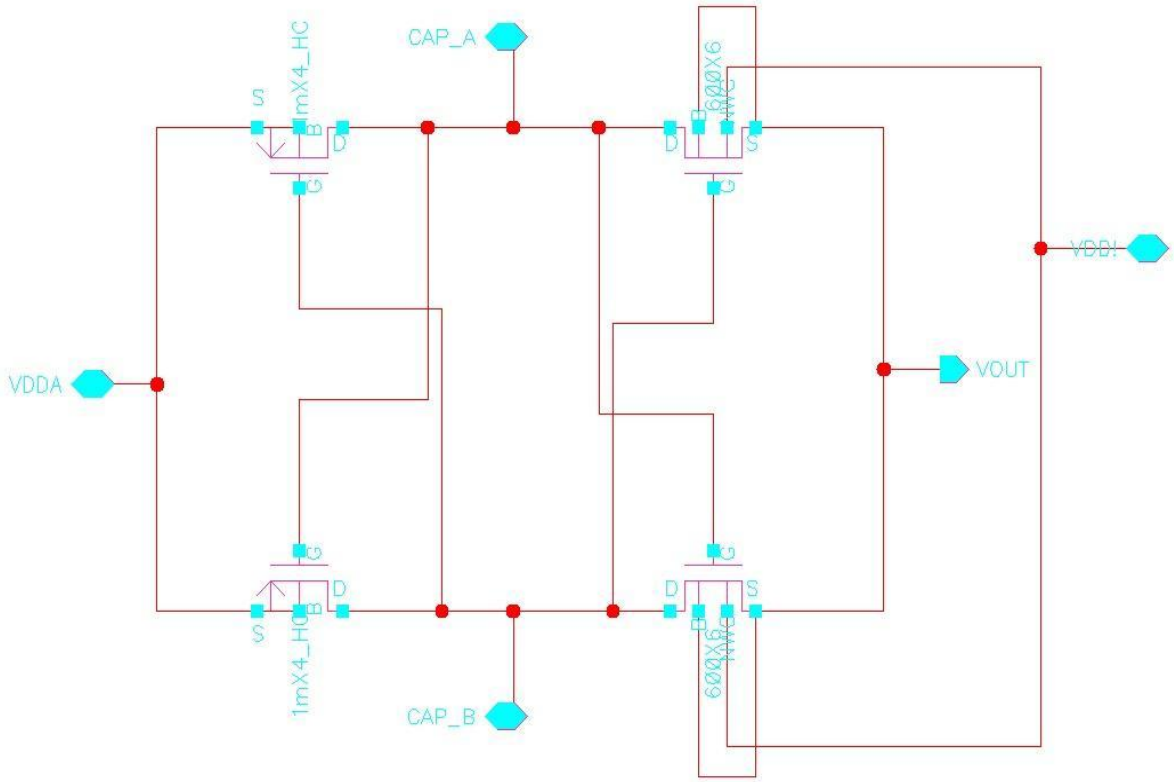

Figure A.8: Schematic of the negative stage of the charge pump

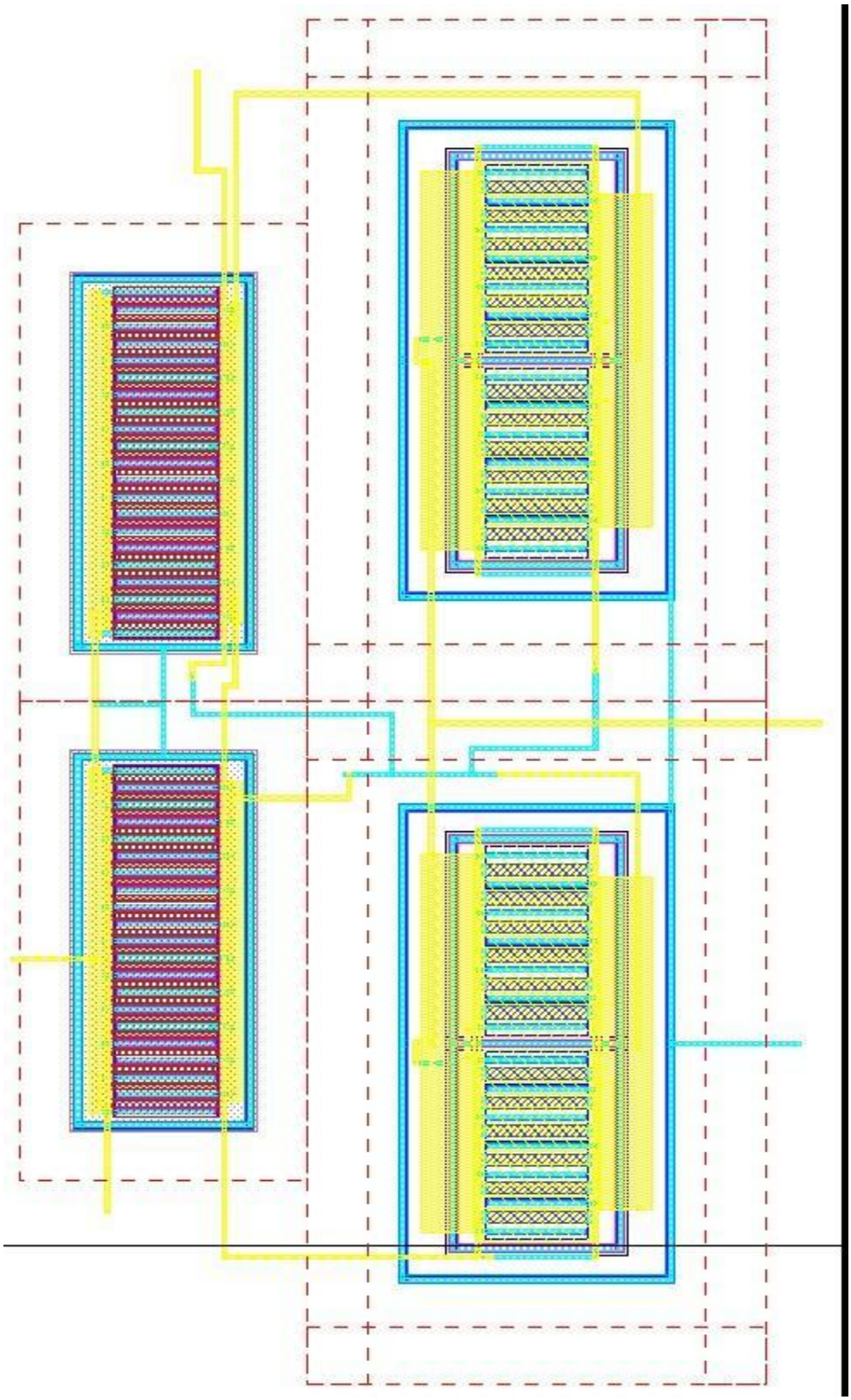

Figure A.9: Layout of the negative stage of the charge pump.

A-3 Top view of the chip ICJPMGPT

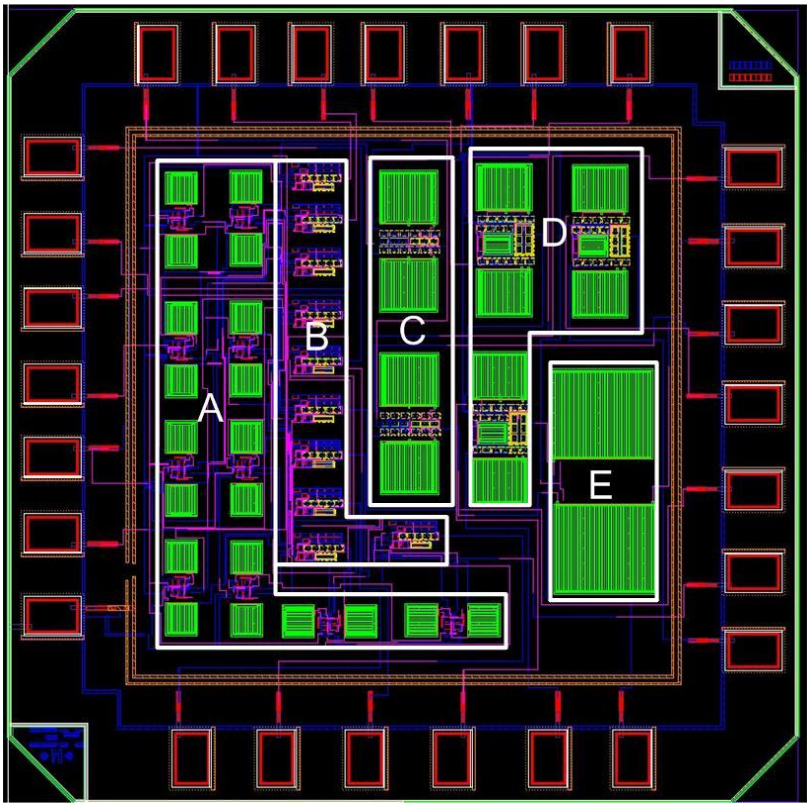

Figure A.10: Top view of the chip ICJPMGPT

A-4 Design Level (ICJPMGPT)

A-4.1 High voltage level shifter

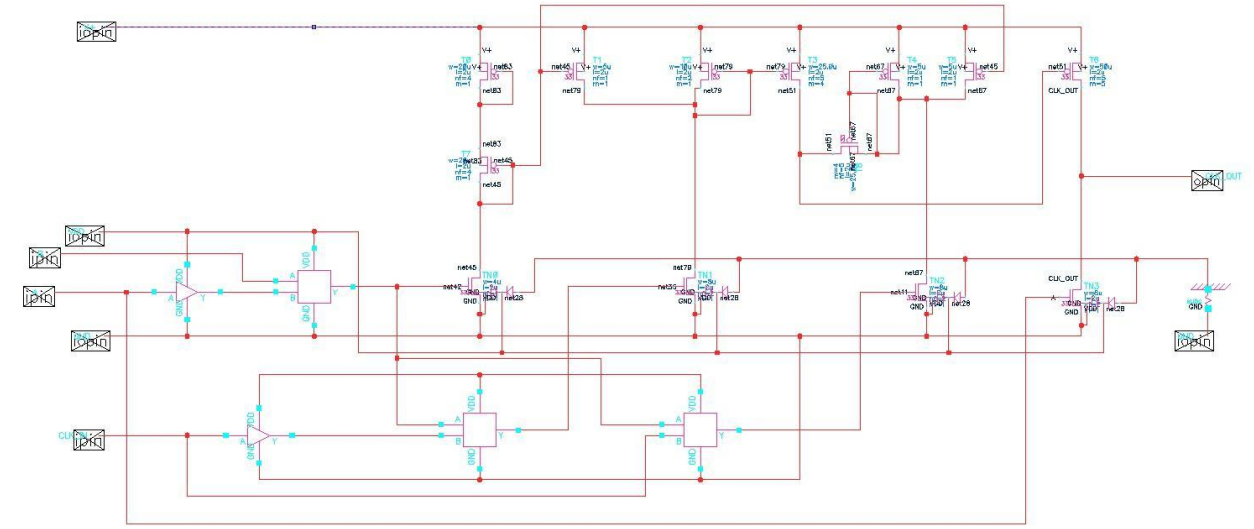

Figure A.11: Schematic of the high voltage level shifter

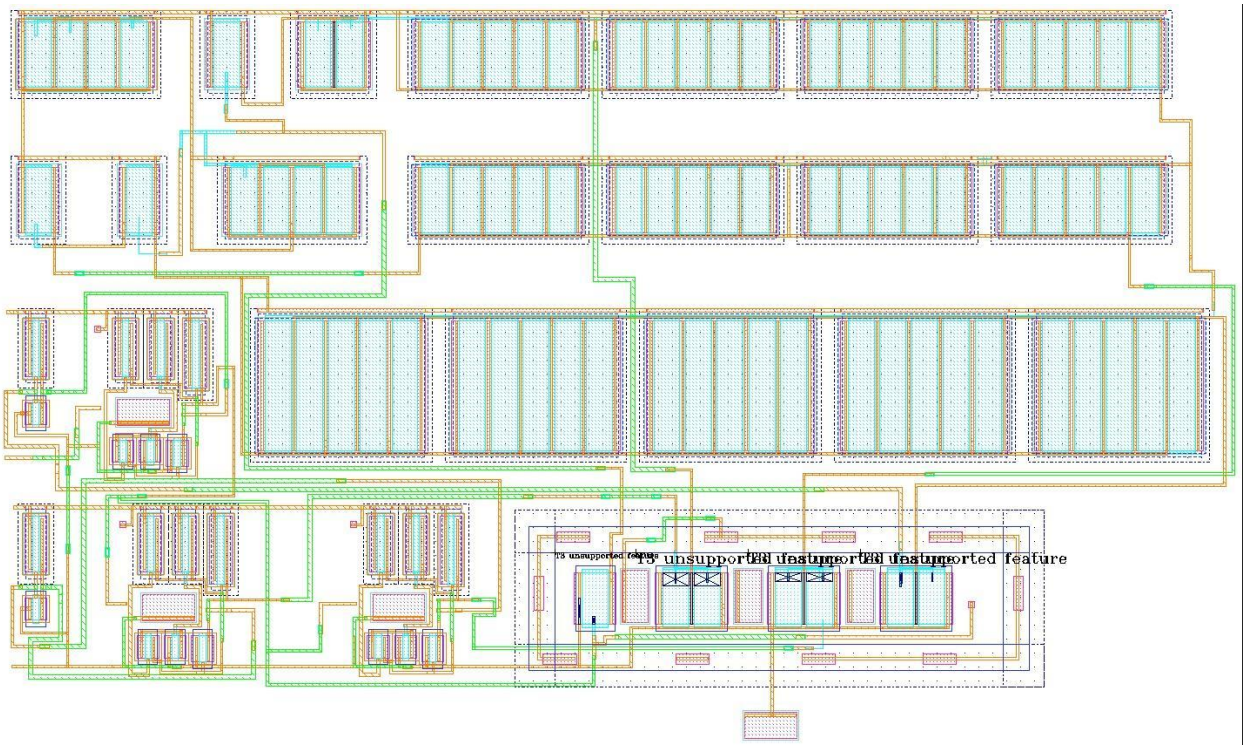

Figure A.12: Layout of the high voltage level shifter

A-4.1 Non-overlapping clock generator

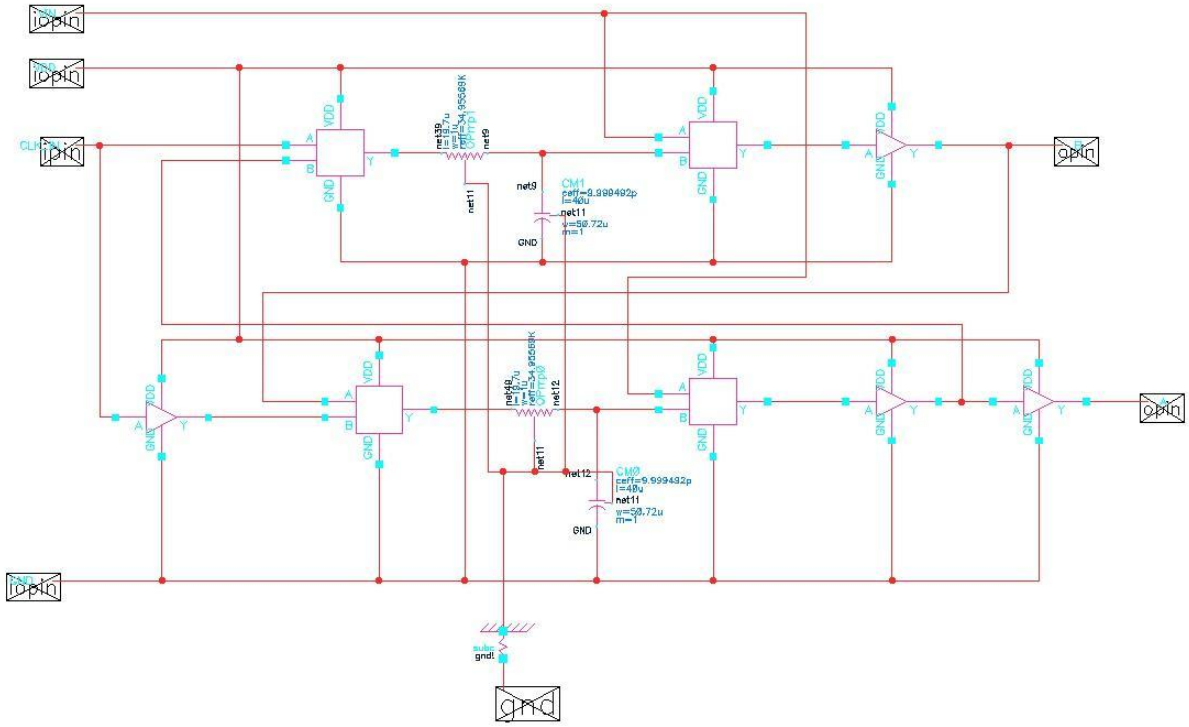

Figure A.13: Schematic of the non-overlapping clock generator

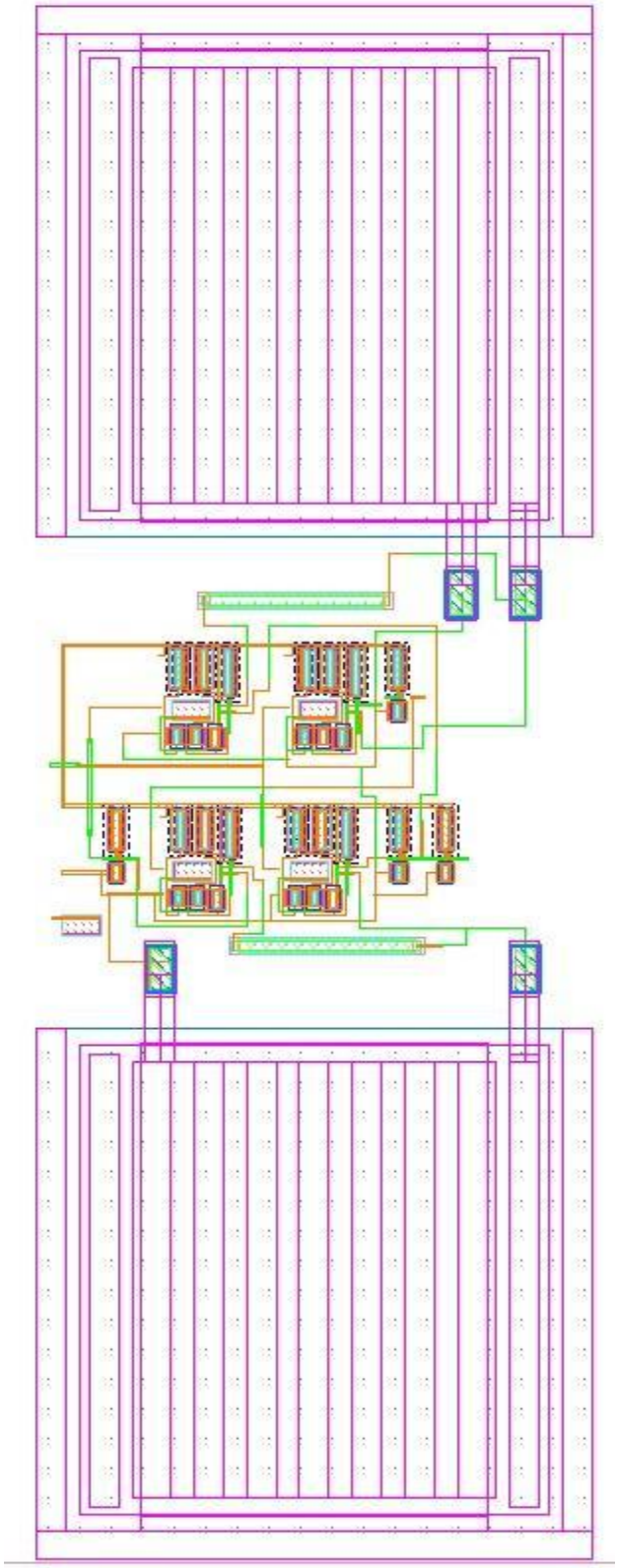

Figure A.14: Layout of the non-overlapping clock generator

A-4.1 Positive stage of the charge pump

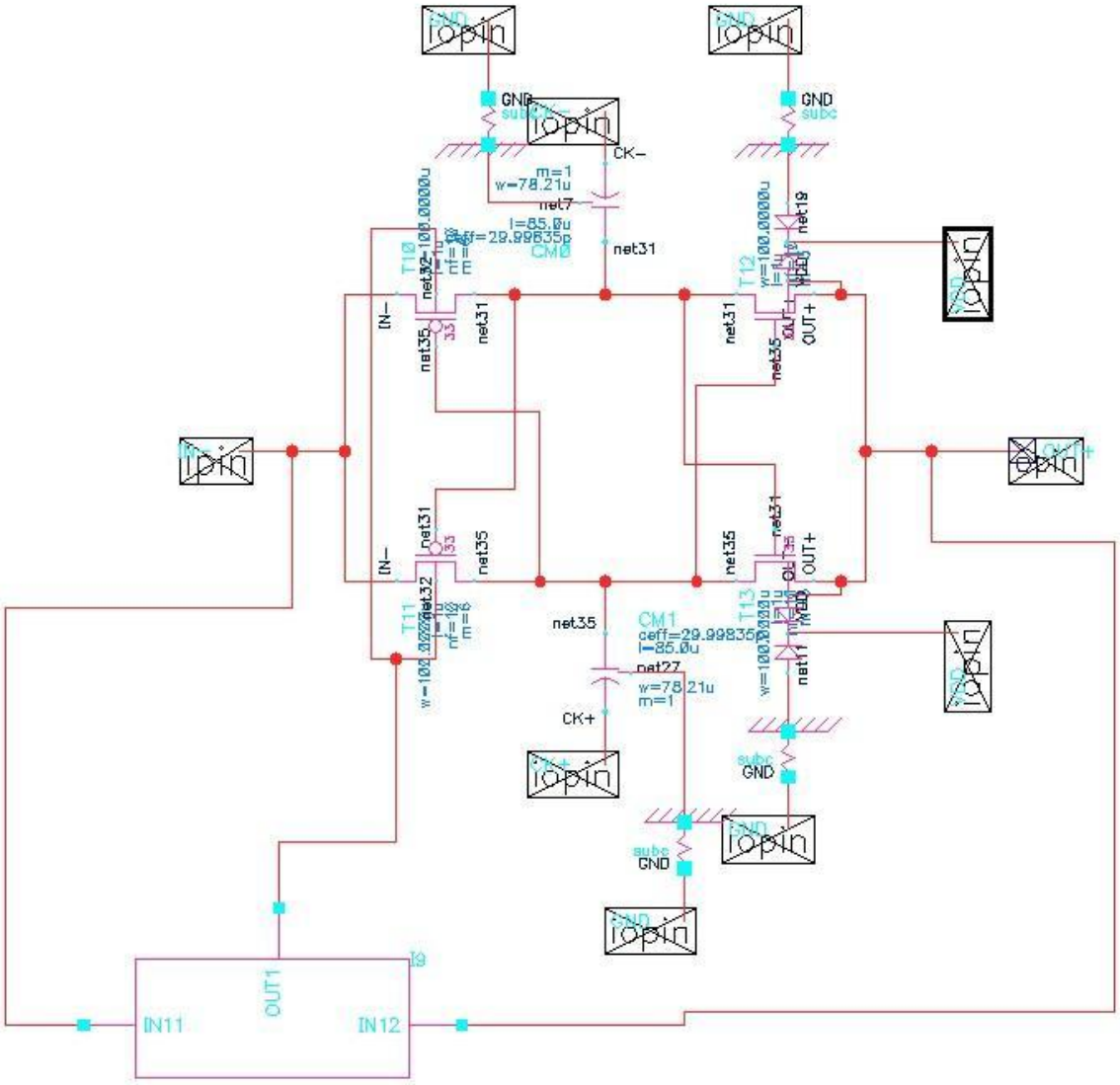

Figure A.15: Schematic of the positive stage of the charge pump

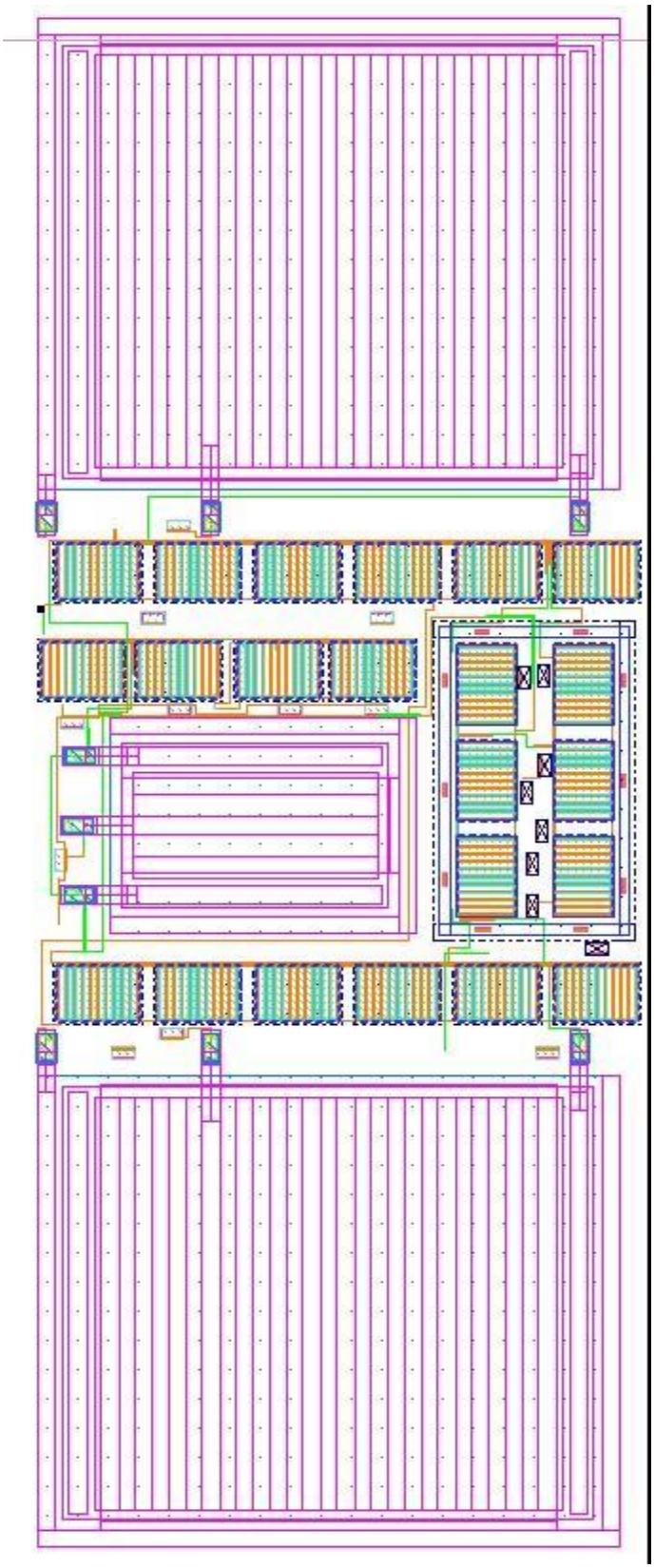

Figure A.16: Layout of the positive stage of the charge pump

A-4.1 Negative stage of the charge pump

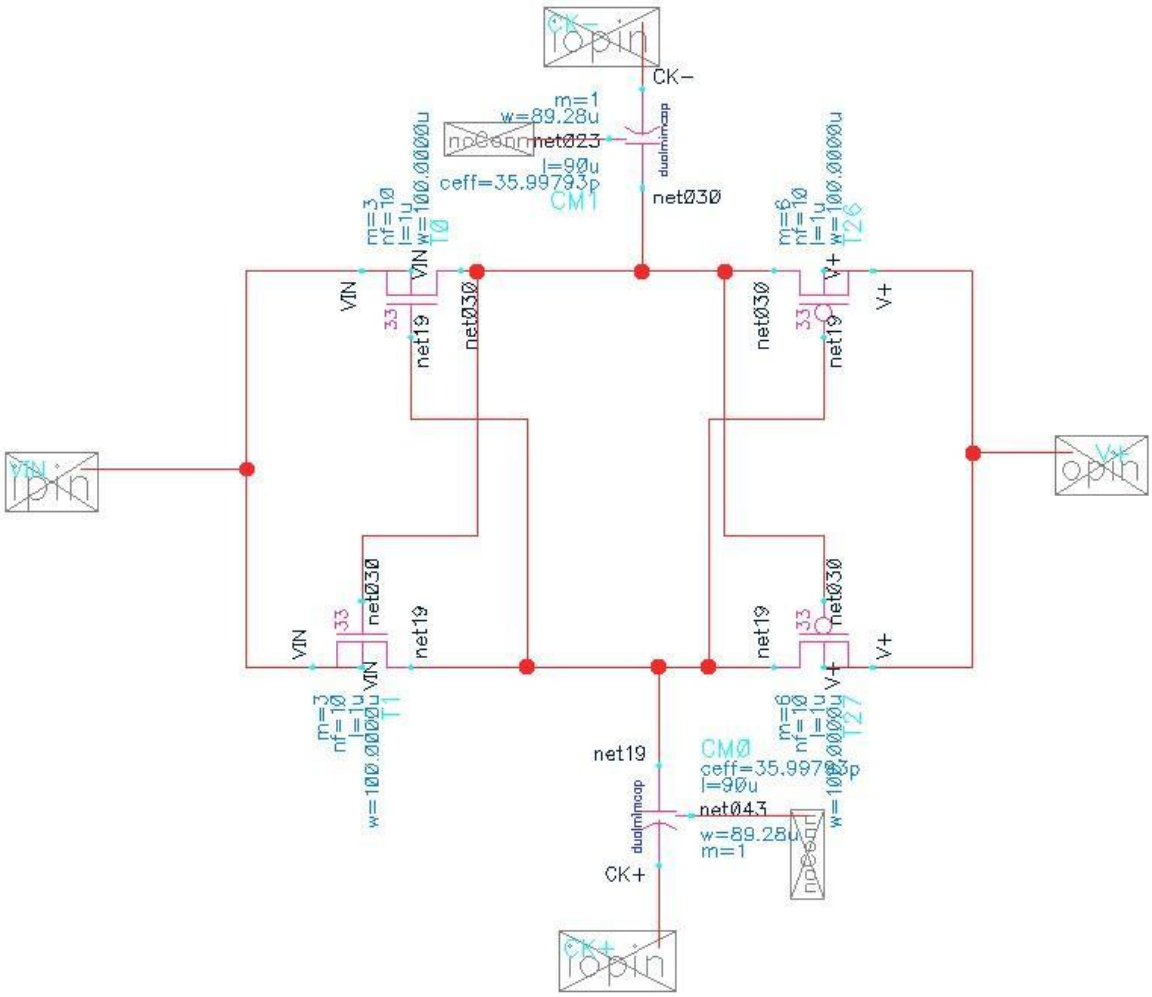

Figure A.17: Schematic of the negative stage of the charge pump

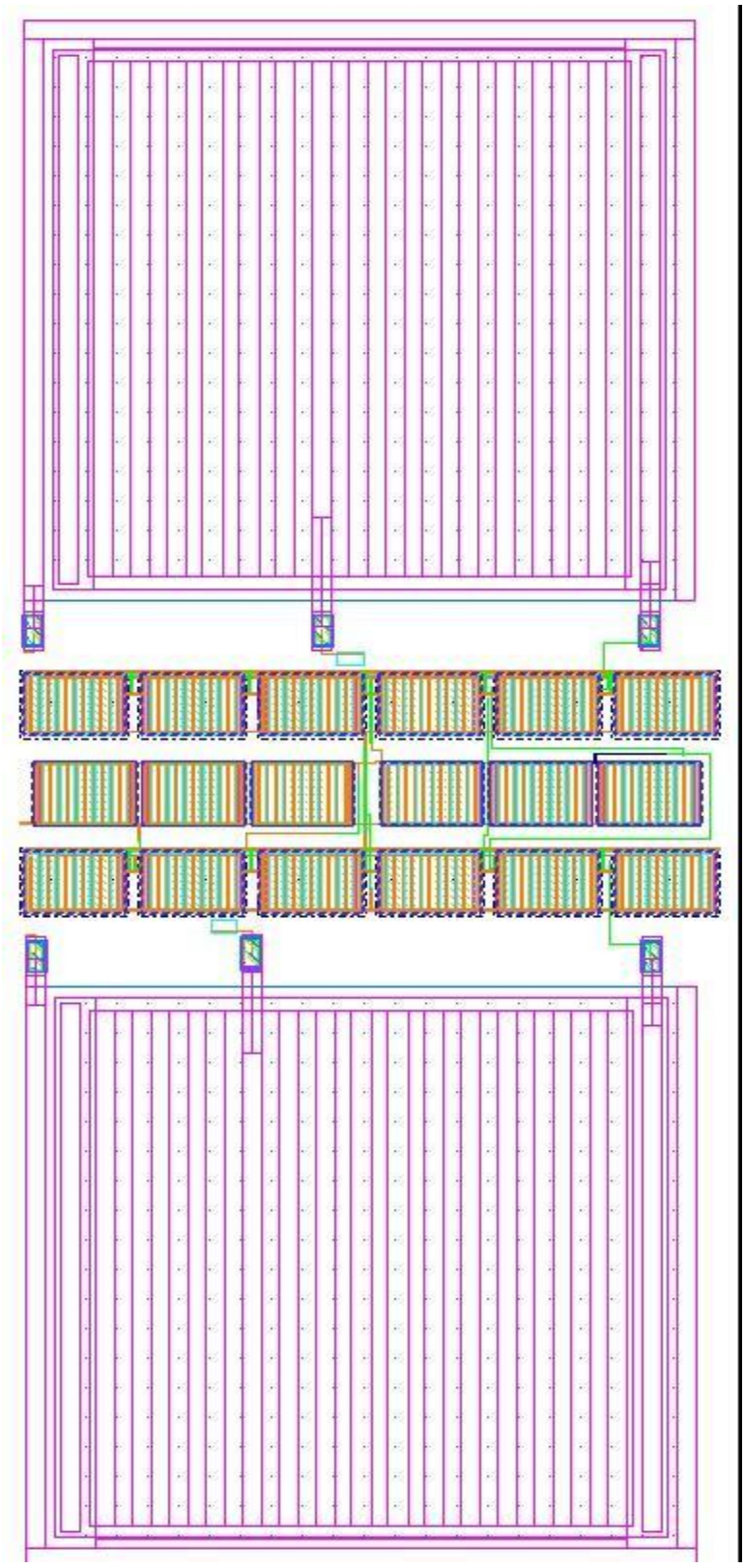

Figure A.18: Layout of the negative stage of the charge pump

A-4.1 Comparator

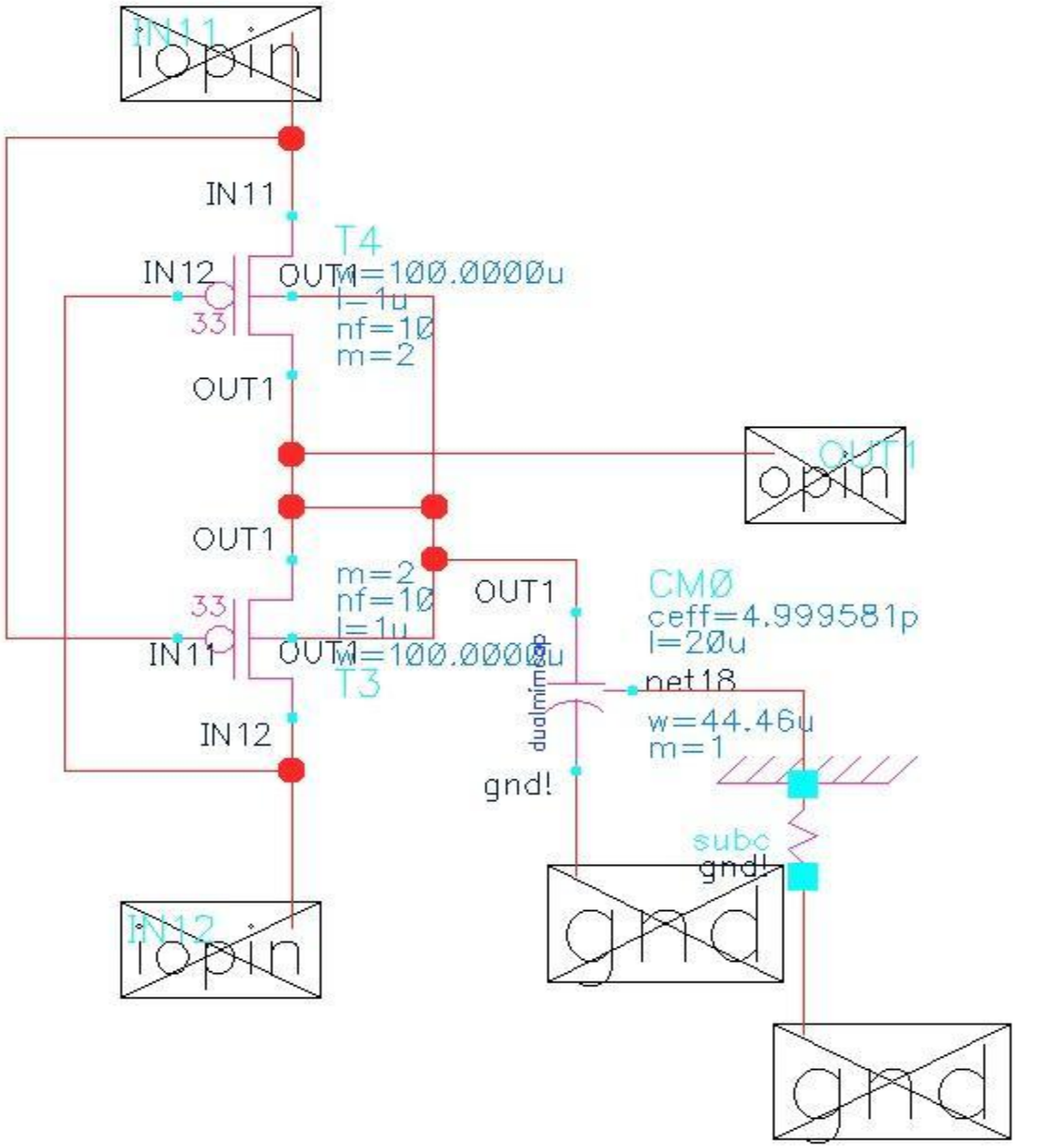

Figure A.19: Schematic of the comparator

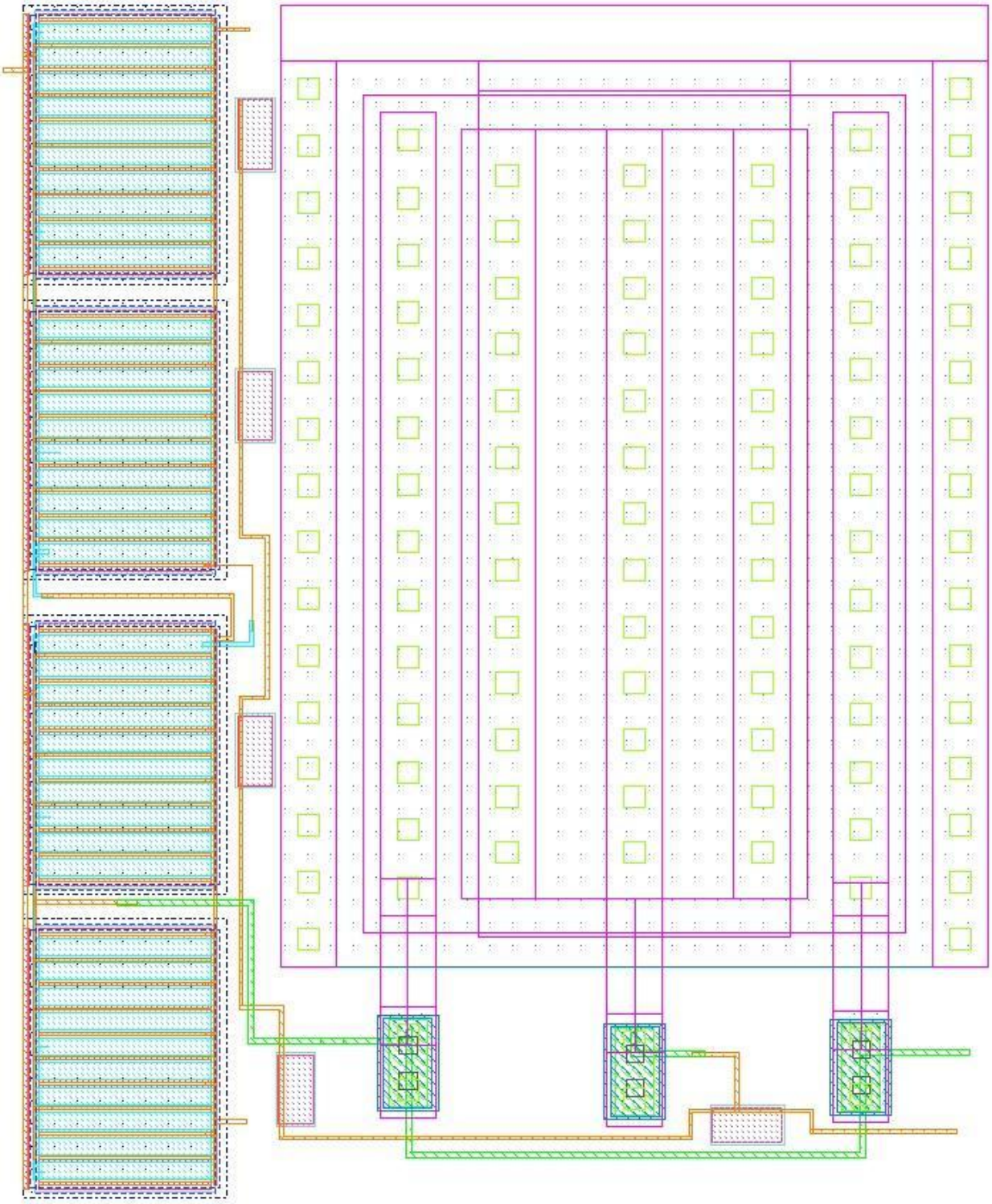

Figure A.20: Layout of the comparator

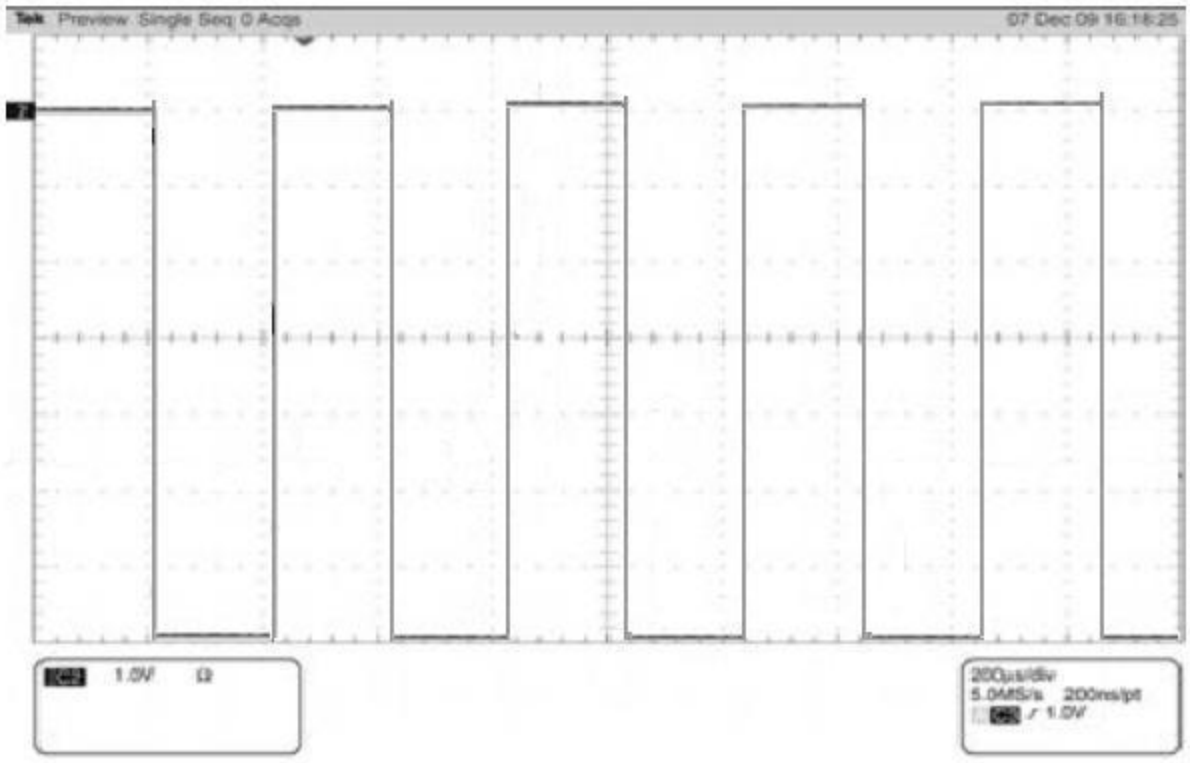

Figure A.21: Output of high voltage level shifter (experimental result)

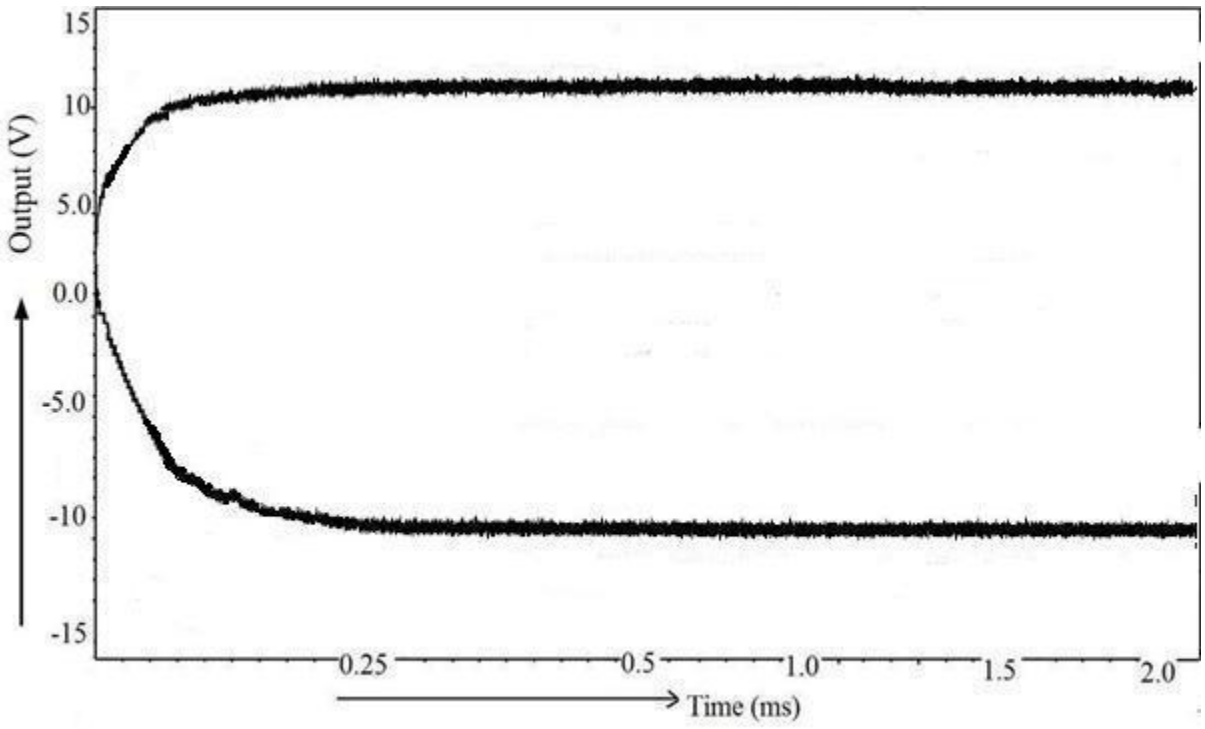

Figure A.22: Experimental output of 0.13 µm Chip (ICJPMGPT)