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Time-mode circuit techniques for high-performance readout interfaces

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Thèse présentée en vue de l'obtention du diplôme de *Philosophiæ Doctor*

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Time-mode circuit techniques for high-performance readout interfaces

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DEDICATION

*To my love, Hamed,
To my beloved parents,
To the loving memory of my M.I.Ls,
To my siblings, Ahad, Hooman, Fatemeh, & Amirhosein . . .*

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RÉSUMÉ

Les interfaces de lecture font partie intégrante des communications entre systèmes électroniques. Elles sont utilisés pour détecter et prétraiter les signaux d'entrée provenant des capteurs et interrupteurs avant de les acheminer à l'étage suivant. Depuis plusieurs années, l'industrie des semiconducteurs a produit des technologies comportant des géométries de plus en plus fines, augmentant ainsi de beaucoup la performance des circuits numériques. D'un point de vue analogique, ces avancées engendrent des difficultés considérant la réduction des tensions de seuil à un rythme moins rapide que l'alimentation, la dégradation des propriétés intrinsèques des transistors, le défi de l'appariement et le plus grand niveau de bruit. Conséquemment, les architectures temporelles et numériques ont gagné en popularité au niveau de la recherche. Cependant, leur performance est limitée par le bruit de phase, la non-linéarité des conversions temps-fréquence, l'intervalle de détection de phase limité, la vitesse réduite et un décalage (IRO) et un bruit (IRN) d'entrée équivalent élevés.

La contribution de cette thèse consiste en plusieurs circuits à base temporelle. Les structures proposées sont conçues, fabriquées et vérifiées à partir d'un procédé CMOS standard 0.35 μm . Tout d'abord, la conception d'un comparateur à faible décalage à base temporelle (TD) de faible bruit, de haute résolution, de grande vitesse et de faible surface à partir d'un VCO est décrite. Afin de convertir deux tensions d'entrée en fréquence, deux VCO identiques sont utilisés, suivi d'un détecteur fréquence/phase innovant pour comparer la durée des signaux numérique du VCO. Les VCO linéaires proposés possèdent de larges intervalles de synchronisation. Ils montrent un faible bruit de phase de -147.57 dBc/Hz à 1 MHz de décalage fréquentiel à une fréquence maximale d'oscillation de 9.37 MHz. Aussi le nouveau détecteur phase/fréquence à bas bruit et basse puissance présente une zone morte (DZ) et une zone-aveugle (BZ) minimale de 12 et 22.7 ps respectivement et ce sans pulsation et glissement. En incorporant les caractéristiques exceptionnelles de ces circuits, le comparateur TD développé dans cette thèse surpasse plusieurs limitations observées de l'état de l'art existant. Entre autres, il présente un taux de conversion de 2.7 MHz avec un bruit équivalent à l'entrée de 148 μV_{rms} et un écart-type de 81.14 μV . De plus, la conception d'un générateur de pulsation à palier ajustable à partir d'un circuit thyristor (THDE) CMOS est abordée. Le THDE basse puissance proposé affiche un large intervalle de délai allant de 26ns à 5 msec avec une sensibilité allant de 240 jusqu'à 2710 ppm/oC respectivement.

Finalement, il a été démontré que les circuits à base temporelle développés peuvent être utilisés pour l'interface de lecture d'un interrupteur de charge industrielle. Dans l'architecture

proposée, l'interface est directement connectée à l'élément interrupteur dans le but d'exécuter le procédé de détection. Grâce au comparateur temporel, l'état de l'interrupteur de charge est constamment surveillé de sorte qu'un signal de rétroaction peut être fourni à un microprocesseur ou à une machine à état. Ce signal de rétroaction permet également l'ajout de circuits de protection industriels via un système de détection de pannes incorporé au générateur d'impulsion. Le circuit d'interface de lecture proposé surpasse les limites des approches conventionnelles du fait qu'il permet l'intégration dans un système sur puce offrant un grand débit de conversion, une grande précision, une basse consommation d'énergie et une haute résolution, en plus d'occuper une aire de silicium réduite.

ABSTRACT

Readout interfaces have become an integral part of communication and interaction between many electronic systems. These interfacing circuits are utilized to detect and pre-process input signals originating from sensors or switches prior to feeding them to subsequent devices. In recent decades, the semiconductor industry has evolved to smaller technologies that are highly effective in digital circuits. A purely analog scheme, however, may face some difficulties at scaled down nodes due to a less reduction of threshold voltages compared to supply voltages, weak intrinsic properties of transistors, and matching challenges, as well as a higher level of noise. As a result, time-based and digitally intensive structures have become widely prevalent among electronic research trends. A time-based readout interface provides significant advantages in terms of power efficiency and chip area. However, the system's performance is restricted by the imperfections of its components, such as phase noise and nonlinearity in the voltage to time/frequency conversion, a limited range of phase detection, low speed, poor input-referred offset (IRO) and input-referred noise (IRN).

To contribute to this topic, several time-based circuit techniques are proposed that form the highlights of this thesis. The proposed structures were implemented, fabricated, and tested in 0.35- μm standard CMOS process. Firstly, the design of an ultra-low offset, high resolution, and high speed voltage-controlled oscillator (VCO)-based time-domain (TD) comparator has been outlined. To convert the input voltage difference into time/frequency information, two identical ring VCOs are used, followed by a novel phase frequency detector (PFD) to compare the output duration. The proposed linear wide-tuning range VCO exhibits a low phase noise of -147.57 dBc/Hz at 1 MHz offset frequency with a maximum oscillation frequency of 9.37 MHz. Also, the proposed innovative low noise PFD features a minimal dead-zone (DZ) and blind-zone (BZ) of less than 12 and 22.7 ps, respectively, free of glitches and undesired one-shot pulses. The TD-comparator prototype outperforms the prior-art designs with an IRO standard deviation of 81.14 μV , an IRN of 148 μV_{rms} , and a conversion rate of 2.7 MHz. Secondly, the design of a duty-cycle adjustable pulse generator based on a proposed CMOS thyristor-based delay element (THDE) is investigated. The proposed low power THDE shows a wide delay range of 26 ns to 5 ms, with a temperature sensitivity ranging from 240 to 2710 ppm/ $^{\circ}\text{C}$, respectively.

Finally, we have integrated and evaluated these time-based circuit designs into a complete time-domain readout interface for an industrial load switch application. In the proposed platform, the interface is directly connected to the switch element in order to execute the

sensing process. Through the use of the proposed TD-comparator, it monitors switching state and provides signal conditioning necessary to derive feedback output for a processor or a state machine. To enable circuit protection in industrial environment, a copy of the feedback signal will be transmitted to an embedded fault detection control system incorporating the proposed pulse generator. The designed readout interface has overcome the limitations of conventional approaches by providing system on chip (SoC) capability, high speed performance, high accuracy, low energy consumption, high resolution, and a small silicon footprint.

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LIST OF SYMBOLS AND ABBREVIATIONS

ADC	Analog-to-Digital Converter
ASIC	Application-Specific Integrated Circuit
BBPLL	Bang-Bang Phase-Locked Loop
BoM	Bill of Materials
BZ	Blind-Zone
DZ	Dead-Zone
DAC	Digital-to-Analog Converter
DCO	Digitally-Controlled Oscillator
ESD	Electrostatic Discharge
FoM	Figure of Merit
FPGA	Field-Programmable Gate Array
IC	Integrated Circuit
I/O	Input/Output
IoT	Internet of Things
IRN	Input-Referred Noise
IRO	Input-Referred Offset
MCU	Micro-Controller Unit
NOC	Number of Oscillation Cycle
OTA	Operational Transconductance Amplifier
PFD	Phase-Frequency Detector
PWM	Pulse-Width Modulation
PLC	Programmable Logic Controller
PLL	Phase-Locked Loop
SoC	System-on-Chip
SiP	System-in-Package
SDC	Sensor-to-Digital Converters
SCO	Sensor-Controlled Oscillator
SNR	Signal-to-Noise Ratio
SNDR	Signal-to-Noise and Distortion Ratio
SWaP-C	Size, Weight, Power, and Cost
TD	Time-Domain
TDC	Time-to-Digital Converter
UVLO	Under Voltage Locked-Out

VCO	Voltage-Controlled Oscillator
VCDL	Voltage-controlled Delay Line
V2F	Voltage-to-Frequency
V2T	Voltage-to-Time
VTC	Voltage-to-Time Conversion
VCR	Voltage Controlled Resistor
WSN	Wireless Sensor Network

CHAPTER 1 INTRODUCTION

1.1 Motivation

The evolution of electronic interfaces has become a vital factor in communication advances between various types of electronics systems dealing with analog or digital signals from sensors, switches, antennas, etc, in the real world [1]. Electronic readout interfaces are widely used in numerous application domains, such as Wireless Sensor Network (WSN), the Internet of Things (IoT), embedded industrial monitoring, biomedical microsystems, and actuator control in avionic systems. Over the past decades, we have seen a growing appeal on compact and low-cost systems with limited power budget as well as an increased need for advanced integration methods, such as System-on-Chip (SoC) and System-in-Package (SiP) modules. Likewise, the semiconductor industry is directed to smaller technologies so as to improve cost, energy consumption, speed, and achieve a high-level integration of devices. Therefore, it is imperative to develop a fully integrated and scalable electronic interface techniques.

Traditionally, high-performance analog interface methods were based on conventional fully analog signals and building blocks, operating in the voltage amplitude domain. However, technology scaling is especially effective for digital circuits, but it introduces some difficulties in designing analog systems [2,3]. Supply voltage reduction, weak intrinsic transistor properties (e.g., lower gain, mismatch), large power and chip area results in poor portability of purely analog solutions to other technology nodes [4]. Therefore, time-based and digitally-oriented structures became increasingly popular. The aim of this thesis is to develop a fully integrated, time-domain circuit technique for an electronic interface framework and to test it with an industrial load switch that can be used at micro scales for power management in industrial application. This thesis proposes several innovative time-domain circuit designs that improve overall system performance by overcoming prior art circuit-level limitations.

1.2 Background and Concept Definition

1.2.1 CMOS Electronic Interface

By and large, there is little debate in the modern world that physical reality is becoming increasingly interconnected with electronics to improve the quality of life in many aspects, such as environmental, industrial, health care, etc. With the growing need for inter-system communication, electronic interfaces have been developed to support various high-

performance mixed-signal Integrated Circuits (ICs) for a wide array of applications [5]. Interfacing is a technique used to link two electronic devices, enabling the adjustment of their Input/Output (I/O) setups to realize cooperative operation. Thus, the interface circuit is responsible for acquiring, conditioning, and transforming input signal alterations into equivalent output signals.

Typically, an industrial readout interface is an I/O module that connects a sensing element, such as a sensor, switch, or transducer, to a specific controller, such as Field-Programmable Gate Array (FPGA), Micro-Controller Unit (MCU), or Programmable Logic Controller (PLC). Therefore, the electronic interface circuits can be classified into two categories: 1) the input interface, and 2) the output interface. The input interfaces monitor the state of a signal received from a sensor or switch as input information, and process it so that a controller can interpret it reliably. The detected signal may be binary, such as from ON/OFF pushbutton switches and transducers, or analog, such as from capacitive and resistive microsensors. The output interfaces are usually designed to communicate between a low-voltage MCU or FPGA and a relatively high-voltage device, such as an actuator, motor, power supply switch, relay, LED, etc. In this interface, a digital or analog output signal can be used to control or drive a load.

The most widespread examples of such interfacing mechanisms are the sensor interface, the I/O interface, and the load switch interface.

1.2.2 Sensor Interface

Sensor systems have become increasingly important because of their integral role in ensuring the cost and performance benefits in many industrial applications [6, 7]. The sensors can be simple or complex, analog or digital, single or multi-functional, and passive or active. The most common passive sensor is a switch, as it is essentially a variable resistor that has two states: infinite and zero. Besides, microsensors can be classified according to their transduction mechanism, such as piezoelectric, resistive, capacitive, optical, etc [8–10]. These sensors usually convert physical, chemical, or biological signals from the surrounding environment into electrical signals. Therefore, the sensor signal, which may represent physical quantities such as temperature, pressure, or position, must be pre-processed before being fed to a higher system level through a sensor readout interface.

Interfacing methods and reading circuits can differ depending on the type of sensor and the type of system being interfaced with. Most often, an interface circuit converts the collected data into a format that can be easily processed by the employed controller and, in many cases, digitized. Thus, the most conventional readout interfaces comprise of two main components:

conditioning circuitry (for signal filtering, amplifying, etc) and the information-to-digital converter. As the accuracy, reliability, and functionality of the overall sensing system are directly influenced by the readout circuit, special consideration must be given to its sub-blocks design, as well as the challenges associated with the integration and the technology scaling.

1.2.3 Load Switch Interface

Power management, by temporarily shutting down unwanted functions, is a prevalent method and a standard system design technique in many industrial sectors [11]. Accordingly, many ICs have this opportunity to use a hardware pin or software control to force the device into low-power, idle, quiescent, or sleep modes with varying degrees of power. However, a quiescent or similar mode only shuts down the IC, and not the associated circuitry, such as resistors, I/O ports, or even discrete transistors that may continue to consume power. Additionally, while it may be possible to turn off the power supply via an enable control line to reduce the idle-mode power consumption of the load sub-circuit, its leakage current in the shutdown state is still considerable. Thus, the power savings may not be sufficient [12].

Therefore, in order to fully realize the power-down concept, an alternative approach is required to gate the power system and shut down the entire sub-sections. A promising solution to extend power system life is using load switches. A load switch connects or disconnects the supply voltage to the load, as commanded by the system. And, by turning off unused circuitry, it improves the operation efficiency of the whole system [13]. Also, the use of load switches can be extended beyond the manipulation of electrical power. Fig. 1.1 illustrates how multiple subsystems can be powered on a single large power supply by using an array of load switches. Multiple digital outputs are used to control the up/down power to these subsystems in accordance with a prescribed sequence and timing. In this manner, the load switches act as gating elements in a broader and a more effective power management framework. As a result, a load switch is an electronic I/O device used to control (enable/disable) the power of a DC rail to an IC, group of ICs, or the sub-circuit of a system.

Basically, a load switch consists of two main elements: a pass transistor and an ON/OFF control unit. Due to the development of CMOS process technologies, MOSFETs are rapidly gaining traction in the switch market. Thus, the MOSFET can be used to implement a pass transistor, allowing the integration of power semiconductor devices [14]. MOSFET switches may be either N- or P-channel, with appropriate control circuits on the gate in each case. The choice between PMOS and NMOS switches ultimately depends on the specific requirements of the load switch application and the trade-offs between different factors such as on-resistance,

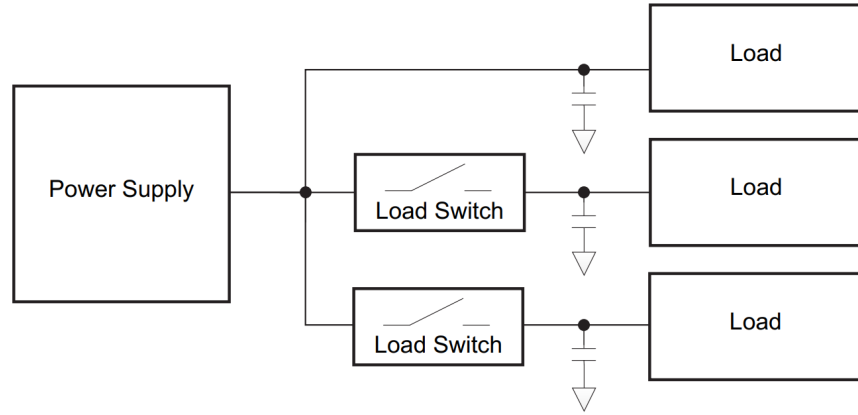


Figure 1.1 Power Distribution Block Diagram [12]

voltage tolerance, and biasing circuitry.

Clearly, when the MOSFET is in conducting mode (on state), the rail current flows and the voltage supply is passed to the load. Also, it is essential to provide a suitable MOSFET driver in the gate's control block for sourcing/sinking the current and ensuring that the pass transistor is turned ON/OFF correctly for the specified voltage [15]. Although a properly sized MOSFET and a single driver can be used for power-rail switching, their capabilities and functions are limited, and insufficient for all ON/OFF switching requirements. As a result, in order to provide an "all-in-one" solution for load switches operation, a readout interface circuit.

On the other hand, until recently, many industrial sectors used wired interconnections for connecting field I/O devices to programmable controllers. This approach could be complex, require extended installation time, and create systemic problems. The larger the system, the more multicore cables and wires are required, which adds weight and space concerns, as well as increasing cost and complexity in design, manufacturing, error tracking and debugging. Long wires stand from an I/O device, sensor, or switch to a programmable controller act as antennas for electrical noise. In such circumstances, sensing devices may collect a great deal of unwanted information in addition to the desired environmental data. Therefore, a small spike in the system could damage or destroy an unprotected controller. Likewise, electrical noise can result in sensor blindness or erroneous data reporting.

Consequently, the traditional method has been replaced by electronic signal routing, which allows an I/O device to be connected to a specific controller without requiring physical modifications. For instance, the load switch readout interface is a promising approach for this purpose. It provides an interface between the programmable network and the switch

sensor while providing control and protection modules located closer to loads. This could reduce the length of cable runs and the size of conductors, thereby eliminating the cost and the weight of electrical wiring harnesses.

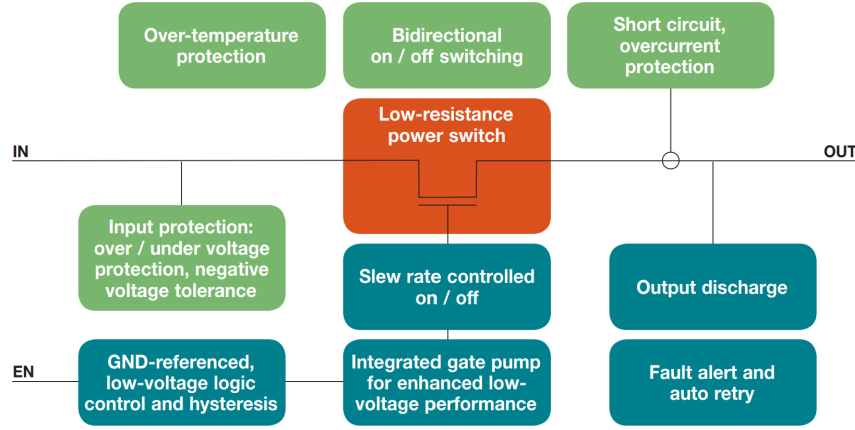


Figure 1.2 Enhanced load switch system including function circuits [16]

Figure 1.2 illustrates overall building blocks of a load switch interface including additional power management functions such as discharge control, slew rate control, various forms of protection, and fault monitoring [16]. Compared to a single MOSFET for switching the power rail, adding these features and capabilities reduces operation time, the Bill of Materials (BoM), and space requirements. In conclusion, this alternative method of reading sensors and actuators is advantageous in industrial settings due to its simplicity, flexibility, cost effectiveness, extra I/O installation capacity, and ability to be widely distributed.

1.3 Problem Statement

In recent decades, increasing interest in low Size, Weight, Power, and Cost (SWaP-C) solutions has broadened integration methods on many platforms. Electronic interface ICs combine all the functions of an interface circuit on a single chip, improving design efficiency while reducing SWaP-C qualifications. Therefore, the target load switch readout interface IC is of vital importance in industrial systems, as it is necessary to ensure the proper execution of command input and eliminate the disadvantages of the previous discrete models. Since the performance of sensing systems is greatly influenced by reading electronic circuits, special consideration should be given to readout interface circuits and systems configuration, as well as the technical limitations associated with technology scaling and integration.

The continual miniaturization of device fabrication technologies poses a serious challenge to the design of readout ICs. Conventional readout interface architectures are primarily

constructed from analog components, such as operational amplifiers, and highly-matched capacitive Digital-to-Analog Converters (DACs) in a feedback loop. Despite the advantages of technology scaling for digital circuits, it severely limits the potential for designing analog blocks due to lowered supply voltage, which affects transistors' intrinsic properties, mismatches, gain, etc [2–4]. Moreover, these analog architectures do not follow the same power reduction and area scaling as digital circuitry, resulting in large power and chip area in scaled CMOS technologies. Consequently, analog solutions are not easily transferable to other technology nodes [17]. As a result, time-based interfaces have become more popular recently due to their highly-digital implementation, offering a small footprint, high energy efficiency, and scalability, leveraging the capabilities of advanced technologies [6, 18].

Time-based solutions can utilize various types of time-domain processing to process signals in the time domain instead of voltage domain. A voltage-controlled oscillator (VCO) is one of the most commonly used structures in time-based designs for converting voltage-domain signals to a signal with time (frequency)-domain information. The reason is that VCOs have the advantage of being highly digital, energy-efficient, scalable, relatively simple to configure, and possess an inherent first-order noise-shaping capability [19]. Therefore, VCOs are key components in various time-based building blocks of sensor interfaces, including time-domain (or VCO-based) comparator, Analog-to-Digital Converter (ADC), Phase-Locked Loop (PLL), and Time-to-Digital Converter (TDC).

However, there are several issues that limit the performance of VCO-based readout circuits, such as limited resolution, nonlinearity, low speed, limited dynamic range, inefficient energy and area consumption. These limitations may result from different circuit-level criteria depending on the structure used to readout, condition, and manipulate the input data. Fundamentally, the intersection of all of the aforementioned architectures for a time-based sensor interface is the VCO, the Time-Domain (TD)-comparator, and the Phase-Frequency Detector (PFD). The circuit characteristics of these components play a critical role in the performance of the entire system, as outlined in the following.

In ring VCOs, nonlinear Voltage-to-Frequency (V2F) conversion and poor phase noise are the principal concerns. In particular, the nonlinear nature of Voltage-to-Time (V2T) conversion provokes a linearity issue in a TD-comparator [19, 20]. Enhancements in the linearity and constant gain of the VCO greatly affect the performance stability of the TD-comparator regarding offset, noise, and energy per comparison. It is due to the fact that in a TD-comparator, two VCOs are usually involved to perform a pseudo differential VCOs structure followed by a PFD. Therefore, with a nonlinear VCO, the resultant frequency difference (Δf) between the outputs of the VCOs in response to a fixed input voltage difference will change with variations

in common mode voltages (or reference input voltages). This results in different operating conditions for the following sub-blocks, leading to inconsistent behavior. Further, an inadequate Δf may lead to non-functionality of the PFD and a consequent reduction in the input dynamic range of the comparator. Likewise, the performance of VCO-based ADCs is severely distortion limited by VCO gain variations (tuning nonlinearity) that causes an inter-stage gain error and Signal-to-Noise and Distortion Ratio (SNDR) reduction [6, 17]. Similarly, in an open-loop VCO-based sensor interface, the VCO's nonlinearity leads to the appearance of harmonic spurs in the output spectrum and limits the overall system Signal-to-Noise Ratio (SNR) [21, 22]. On the other hand, TD-comparator's resolution is adversely affected by VCO phase noise, since it negatively affects the comparator's Input-Referred Noise (IRN) performance. Also, VCO phase noise is the main limiting factor in closed-loop time-based interfaces, as it has a detrimental effect on the SNR and achievable resolution [23]. In the case of a PLL-based interface circuit, phase noise of the VCO may result in random rotation of received signals, amplitude variations, and channel interference.

In PFDs, the presence of a Dead-Zone (DZ) and Blind-Zone (BZ), which correspond to the time slots of missed phase error detection near 0° , and 360° , respectively, is one of the most prevalent shortcomings [24–26]. As a result of DZ, the PFD cannot detect the phase error between its two inputs when an infinitesimal phase difference exists. The BZ also prevents the PFD from responding properly to any changes in input signals [27]. Due to this, the PFD's linear range of phase characteristics is reduced to less than the ideal linear phase range of $\pm 2\pi$. These demerits adversely impact the operation of constituent blocks in the readout interface, thereby impairing its overall performance. For instance, DZ introduces phase noise into a PLL system, and BZ aggravates cycle slips, lengthens the frequency acquisition process and reduces the range of phase-locking [27]. In a TD-comparator, the probable jitter at the VCO outputs leads to phase fluctuation, which makes it difficult for a PFD to make fast decisions due to available DZ. Therefore, the DZ determines the noise level and the delay time of the comparator. Also, inevitable non-zero setup time of prior-art PFD designs is a critical factor in PFDs, and subsequently in overall system speed constraints. In high-frequency operation, BZ becomes more crucial, while both the DZ and the BZ contribute to resolution of the comparator. In addition, most PFD designs contain some small glitches at the outputs, that cause the output signals to be at high potentials simultaneously. This results in leakage currents, increasing reference spurs, and a wrong decision at the output of the comparator [28].

TD-comparators play an essential role in many types of sensor readout interfaces, particularly for data conversion, quantization error shaping, and process monitoring. However, employing low-performance circuits for the main blocks of the TD-comparator, such as the

V2T converter and the diversion detection unit, resulted in low speed (long comparison time) and poor jitter behavior in prior-art designs. Particularly, in the case of non-zero DZ performance of the PFD, if the input voltage difference of the comparator is too small, the pulse time difference at the output of the VCOs may not be sufficient and within the DZ. So, the VCOs must oscillate until the phase difference gets out of the DZ. Thus, considerable power must be consumed since the number of oscillations and decision time are influenced by the voltage level of the input. Also, due to closed loop operation of VCO-based TD-comparator, the output jitter caused by PFD's DZ may be added to random Input-Referred Offset (IRO) of the comparator [29]. In addition, the IRN of the comparator is directly related to the noise behavior of the VCO. The IRO and IRN mainly determine the comparator resolution. Recent highly miniaturized devices usually yield very small output signals with a range of nonidealities. Therefore, there is a persistent need for a high resolution TD-comparator capable of detecting and sensing such small signal changes. As a result, the importance of the VCO and PFD performance, which have a significant influence on the standard resolution via the DZ/BZ and comparison duration time, for a TD-comparator cannot be overstated. As a matter of fact, the time taken by a comparator to resolve a small input difference determines the clock frequency, sampling rate, and convergence speed in ADCs and readout interfaces.

Additionally, noise, line impedance, Electrostatic Discharge (ESD), surges in power or a combination of all these factors can cause signal levels to fluctuate during transmission, resulting in a variety of errors and faults in the system. In this regard, the configuration of an internal control stage for the purpose of fault detection is an essential part of a load switch interfacing system. In order realize a robust fault detection stage, fully integrated and highly accurate sub-blocks are required. The pulse generators and delay elements are usually the main components of these control schemes. Usually, these circuits are limited by relatively narrow operation range, the high sensitivity to process and temperature variations, the jitter, the high power consumption, and the large area due to the use of passive components, all of which have a strong effect on the fault detection efficiency.

Consequently, overcoming all of the aforementioned circuit-level limitations is fundamental in readout interface applications, where high resolution and high linearity, low energy, and high speed are required, along with small area and high robustness.

1.4 Research Objectives

To tackle the problem mentioned in Section 1.3, we propose in this thesis several time-based circuit techniques, designs, and analyses intended for the proposed time-domain load switch readout interface. The main objectives of this thesis are listed as follows:

- General Objective:

The general objective of this research is to develop a readout interface for the load switch application to overcome the imperfections of conventional discrete methods while enabling a reconfigurable integrated topology. Meanwhile, time-mode techniques and digitally-oriented circuit designs are envisioned as an alternative and effective solution to the drawbacks of traditional analog methods.

- Specific Objectives:

1. The first objective seeks to propose an on-chip VCO design with improved linearity correction, less gain variations, low phase noise, and full-swing. Also, the aim is to study the phase noise of the VCO based on theoretical analysis considering the impact of intrinsic and extrinsic sources of noise.
2. The second objective aims to provide an improved low-noise PFD, with minimized DZ and BZ, free of glitches and undesired one-shot pulses. This strategy requires to overcome the prior art's shortcomings that limit the achievement of the general and the third objectives.
3. The third objective benefits from the advantages of the first and second objectives to exploit a high accuracy VCO-based TD-comparator as a fundamental component of electronic interfaces. The aim is to improve resolution, offset, noise, speed and power/area efficiency to meet the needs of high-performance readout interface applications. Therefore, the linear low phase noise VCO is employed along with a minimal DZ/BZ, a glitch-free PFD and a power reduction technique.
4. The fourth objective is to develop a tunable, current-controlled, compact, wide-range, improved temperature and process sensitivities, and low-power CMOS thyristor-based delay element. To this end, two different current sources are needed to be employed to cover different ranges of reference current while maintaining the tunability of the design and offering low sensitivity to temperature and process variations.
5. The fourth objective is to design an internal control module for fault detection purposes as a complementary requirement of the interfacing systems. This strategy prevents failure of the overall system in the event of feasible interference occurring in a noisy, harsh industrial environment. The target is to propose a pulse generator that can generate a pulse with a stable width and convert a noisy, digital/analog input signal into a stable pulse pattern regardless of the signal amplitude to meet

the needs of reliable fault detection scheme. Also, it benefits from the fourth objective solution to enhance the achievable operating range, accuracy, and power efficiency.

1.5 Claimed Contributions

In pursuit of the aforementioned objectives, the following six publications propose time-based circuit design techniques as components of the load switch readout interface.

1. M. Esmailzadeh, Y. Audet, M. Ali and M. Sawan, "A Low-Phase-Noise CMOS Ring Voltage-Controlled Oscillator Intended for Time-Based Sensor Interfaces," in *IEEE Access*, vol. 10, pp. 101186-101197, 2022, doi: 10.1109/ACCESS.2022.3208273.
2. M. Esmailzadeh, Y. Audet, M. Ali and M. Sawan, "A Low-offset VCO-based Time-domain Comparator Using a Phase Frequency Detector with Reduced Dead and Blind Zones," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2022, Early Access, doi: 10.1109/TCSI.2022.3227802.
3. Mahin Esmailzadeh, Yves Audet, and Mohamad Sawan, "TIME-DOMAIN COMPARATOR AND PHASE FREQUENCY DETECTOR," U.S. Patent, No. US 63/228,245, 2 Aug 2021.
4. M. Esmailzadeh, M. Ali, A. Hassan, Y. Audet and M. Sawan, "Low-Power High-Accuracy VCO-Based Comparator for Sensor Interface Applications," 2020 18th IEEE International New Circuits and Systems Conference (NEWCAS), 2020, pp. 254-258, doi: 10.1109/NEWCAS49341.2020.9159801.
5. M. Esmailzadeh, Y. Audet, M. Ali and M. Sawan, "A Wide-range Low-power Thyristor-based Delay Element with Improved Temperature Sensitivity," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2023, Early Access, doi: 10.1109/TC-SII.2023.3245562.
6. M. Esmailzadeh, M. Ali, A. Hassan, M. Nabavi, B. Gosselin and M. Sawan, "A Tunable CMOS Thyristor-Based Pulse Generator for Integrated Sensor Interface Applications," 2020 IEEE International Symposium on Circuits and Systems (ISCAS), 2020, pp. 1-5, doi: 10.1109/ISCAS45731.2020.9180572.

The first publication, i.e., an IEEE Access journal paper, contribute toward meeting the first objective. The purpose of this study is to propose a straightforward VCO structure while

considering the trade-offs intended for a given specification. In the proposed VCO, a single-ended delay cell with a full-swing, controlled and moderate gain is designed to ameliorate the phase noise. As a result of the biasing circuit configuration of this delay cell, the $f - V$ characteristics linearity has been improved and the frequency tuning range has been greatly extended. The phase noise behavior of the proposed VCO is thoroughly investigated using an analytical model, which has good agreement with the measurement results. According to the experimental results compared to prior-art works, the proposed VCO has the lowest phase noise performance, the widest linear tuning range, and the smallest area. Also, two Figure of Merits (FoMs) has been utilized to allow a fair comparison of phase noise in terms of the oscillation frequency, the power consumption and the tuning range. The proposed VCO exhibits significantly better FoMs performance than previous studies. In addition, the characteristics of the presented VCO in a PLL-based sensor interface have been discussed via a MATLAB/SIMULINK model. The behavioral results confirm that the VCO's phase noise is the major limiting factor for the SNR performance of the targeted application.

The second and third publications, i.e., a TCAS-I journal paper and a patent, propose high-performance PFD and TD-comparator architectures to achieve the second and third objectives. As a first step in achieving these objectives, the preliminary findings of our research have been reported in the fourth publication, i.e., a peer-reviewed NEWCAS conference paper. This paper presents a primary proposal model for the VCO-based comparator and its building blocks. In the first version of the proposed PFD, a NOR-based reset technique is employed that limits the BZ, power consumption, and operating phase range aspects. In the journal papers (publications #1 and #2), the shortcomings of the initial version of the VCO and PFD designs have been addressed. In the IEEE Access journal, the VCO has been optimized to achieve a low phase noise level and improved linearity. Likewise, the TCAS-I journal paper proposes an innovative PFD architecture that improves the DZ, the BZ, phase characteristics, and power consumption. Incorporating the exceptional characteristics of these sub-blocks, the second proposed model of VCO-based TD-comparator in this journal paper shows significantly improved performance. Also, a feedback control unit in this comparator prevents further power loss by disabling VCOs with a controlling signal after the comparison has been completed. A comparison of the measurement results with those of state-of-the-art TD-comparators indicates that the proposed design achieved the lowest IRO, highest normalized speed, comparable normalized energy and IRN. Also, it can attain excellent resolution without requiring large numbers of oscillation cycles and increasing the comparison time and power usage. On the other hand, several analytical models are extracted resulting in closed-form expressions for resolution, comparison time, and gain of the TD-comparator. These analysis as well as the measurement results indicate that the DZ and

BZ of the employed PFD are dominant factors that determine offset, resolution, speed, and energy consumption of the comparator. Furthermore, due to the gain stability of the VCO, the proposed comparator can operate over a wide range of input common-mode voltages.

The fifth publication, i.e., a TCAS-II journal paper, proposes a delay element architecture in order to meet the fourth objective. It is intended to design a wide-range, adjustable, accurate delay element with low temperature and process sensitivities. This study employs a CMOS thyristor-based approach to suppress the common drawbacks of conventional delay elements such as static power dissipation, temperature and process instability and erratic delays. These advantageous features have been extended over a wide delay range by reducing subthreshold currents, utilizing on-chip source degeneration resistors, and employing two robust control current sources. The experimental results demonstrate its superiority over prior-art THDEs.

The sixth publication, i.e., a peer-reviewed ISCAS conference paper, along with the CHAPTER 6 of this thesis containing the unpublished material related to the proposed prototype implementation, contribute to fulfilling the fifth and general objectives. The design and performance of a square-wave generator capable of producing an output pulse train with a tunable stable width have been explored. It comprises the proposed THDE structure (in publication #5) to realize a pulse generator that is capable of controlling the pulse width with minimal energy loss, as well as being persistent over temperature and process variations. In CHAPTER 6, an I/O interface has been proposed to provide access to the state of a load switch in an industrial power electronic application. It has a versatile functionality through its configurable output stage, combined with a dual-mode gate driver that adapts the command signal for the operation of the load switch. Further, it consists of a monitoring stage that is based on the novel TD-comparator design presented in publication #2. This stage reads the switching state of the load switch and conditions it for processing. In addition, a fault detection stage is used to control the vulnerability of the interface network to environmental hazards. The idea is to use the proposed thyristor-based pulse generator to implement a compact, adjustable and robust fault control design capable of detecting discrepancies between the input command and response signals. Thanks to the flexible THDE, the fault recognition system is prepared to distinguish between temporary and actual errors.

1.6 General Organization of the Thesis

The thesis is organized as follows: A comprehensive literature review is presented in CHAPTER 2. It discusses existing works on the characterization of readout interfaces and their constituent building blocks, while focusing on their main challenges and limitations. Three chapters of this hybrid thesis are based on three publications to achieve the research objectives

stated in CHAPTER 1. There is also a complementary chapter containing the unpublished material.

CHAPTER 3 presents the first publication, which is a journal paper published in IEEE ACCESS. It describes a VCO design showing reduced phase noise and improved linearity to overcome the challenges and obtain the first objective. This chapter outlines the proposed topology and provides the analytical models and measurement results. Also, the effectiveness of the proposed VCO characteristics is validated through a Matlab/Simulink model of a closed-loop PLL-based sensor interface.

The second publication presented in CHAPTER 4 is a journal paper published in TCAS-I seeking to achieve the second and third objectives by proposing a high-performance VCO-based TD-comparator. This chapter mainly explores a low-power low-noise glitch-free PFD architecture with minimal DZ, BZ to ameliorate the offset, resolution, and speed of the proposed TD-comparator without the need for any calibration scheme. In this design, the proposed VCO in CHAPTER 3 has been adapted to perform V2F conversion and to enhance the TD-comparator's noise performance.

In CHAPTER 5, the third publication, which is a journal paper published in TCAS-II, is presented. This chapter describes a novel CMOS thyristor-based delay element to achieve the fourth objective. This design employs two current sources, a digitally controlled (DC) and a voltage controlled (VC), to demonstrate the design choice trade-offs while providing a wide range of delay amounts, a reduced temperature and process sensitivities.

In CHAPTER 6, the steps towards meeting the general and the fifth objectives of this research are explained. This chapter provides further information to verify the functionality of the proposed innovative circuit designs, discussed in previous chapters, in an electronic readout interface. The proposed subsystems, namely the time-based monitoring stage and the internal control stage, are described in this chapter, which has also been published in two peer-reviewed conference papers (the fourth and fifth publications listed in Section 1.5). In addition, complementary circuit designs required to meet the specifications of the proposed interface are presented, and their functionality and operation are demonstrated through post-layout simulation and measurement results.

A general discussion of the thesis' objectives and accomplishments is provided in CHAPTER 7. Finally, CHAPTER 8 presents the concluding remarks, main contributions of this research, and future research scopes.

CHAPTER 2 LITERATURE REVIEW

2.1 Load Switch Interface

In this section, a literature review of load switch systems is presented. Furthermore, conventional discrete approaches are studied, as well as fundamental tradeoffs associated with integrated solutions.

In recent years, power management circuits have been widely used to drive circuits in applications ranging from automotive to communications and industrial technologies. Load switches are power supply channel components that perform the function of supplying and coupling power to a load or a device, such as a digital logic circuit or a memory cell, and cutting off power supply to the unused loads. A basic load switch includes four connections: input voltage, output voltage, enable port, and ground. As explained in section 1.2.3, to improve the working reliability of a traditional load switch, designers have attempted to integrate functions for load switches.

Having said that, a controllable electrical load switch combining a power system and a control device to connect a source voltage to a load has been developed in [30], for lighting system applications. In order to minimize the average magnitude of the current when the switching device is in the off-state, the power system includes a switching regulator for extracting energy directly from the input voltage. In order to provide on-state power control, an inductive transformer is connected in series with the switching device. However in this discrete structure, the power inputs are connected to a pre-existing wall switch and do not utilize an on-chip pass transistor switch. Also, its power system produces a low power output (around +5V) referenced to circuit ground, which restricts its application to low voltage switch applications. Further, these devices have been too large to fit replacement switch requirements.

The other method for performing a load switch is presented in [31], in which a charge pump is used to drive a gate of the load switch. It is necessary to control the charge pump frequency based on the required states of the load switch for an appropriate output to be coupled to the load switch. However, this design is limited to applications in which the power source must be multiplied over a period of time such as in portable computers. In this case, MOSFET power transistors are used to switch peripheral devices like disk drives and displays, and the system configuration serves as the "high side" driver. Therefore, charge pump circuits are used to drive MOSFET transistor gates beyond the voltage levels on the supply rails in order

to fully activate the switch and enhance its performance. This technique also suffers from high power losses in the charge pump oscillator and high voltage ripple due to the switching of the main phase-leg switches in high current applications. Therefore, the configuration of this load switch limits it to the low current applications, and it cannot be used for low-side switches.

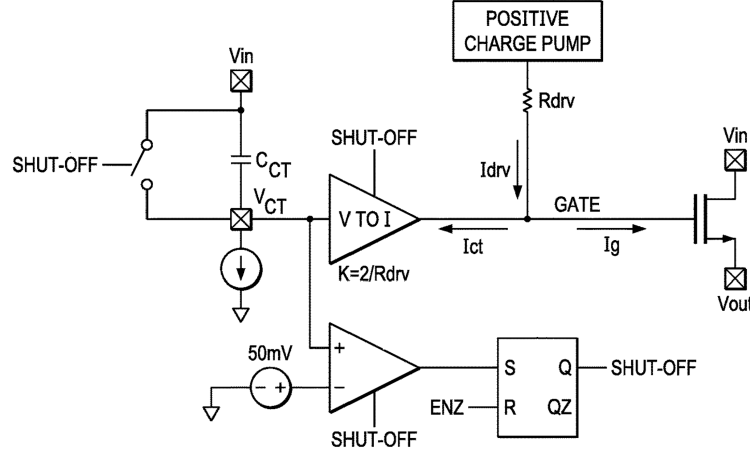


Figure 2.1 A low quiescent current NMOS load switch with shut-off circuitry [32]

In [32], a low quiescent current load switch is disclosed with a transconductor that converts voltage to current for insertion into a pass transistor's gate. This current-controlled gate then delivers power from the power supply to a load. As illustrates in Fig. 2.1, an additional resistive driver circuit is also used to provide power to the gate from a charge pump. A constant gate slope control is used for the NMOS load switch to oversee the variation rate of the gate voltage over time and disable the driver when the gate is activated. To further improve the circuit design and reduce unwanted quiescent current, a shut-off circuit and a comparator are included to disable gate slope control when not required.

An integrated load switch circuit that attempts to overcome the problem of slew rate in the driving phase is presented in [33]. Figure 2.2 shows this stand-alone load switch IC that contains driver and slew-rate control circuits. In contrast with most commercial load switches using NMOS for the pass element, this circuit utilizes a P-type power MOSFET (M_{P1}) to improve performance in a radiation environment. This IC contains five nodes that are connected to the input voltage, external load, ground, and a soft-start capacitor C_{ss} that is used to store energy and control the pass transistor's slew rate. Since the driver and slew-rate control circuit are derived from the same power rail as the MOSFET switch and load, the design may be suitable for some industrial applications where the low power consumption is not often the decisive factor. In addition, leakage current and quiescent

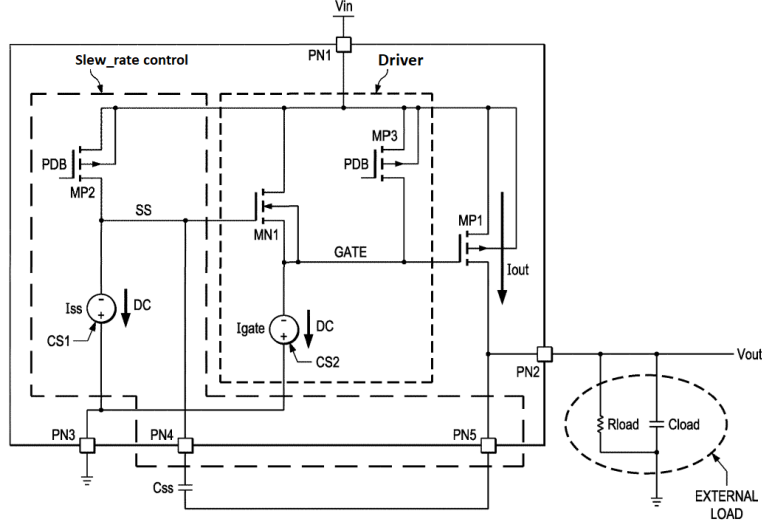


Figure 2.2 A load switch circuit having a controlled slew-rate [33]

current are unavoidable in this structure due to the use of only two PMOS transistors as switches to drive the gate of the power MOSFET and enable the load switch. The leakage results in a longer time for pulling down the load switch's gate node, which limits the speed of the architecture.

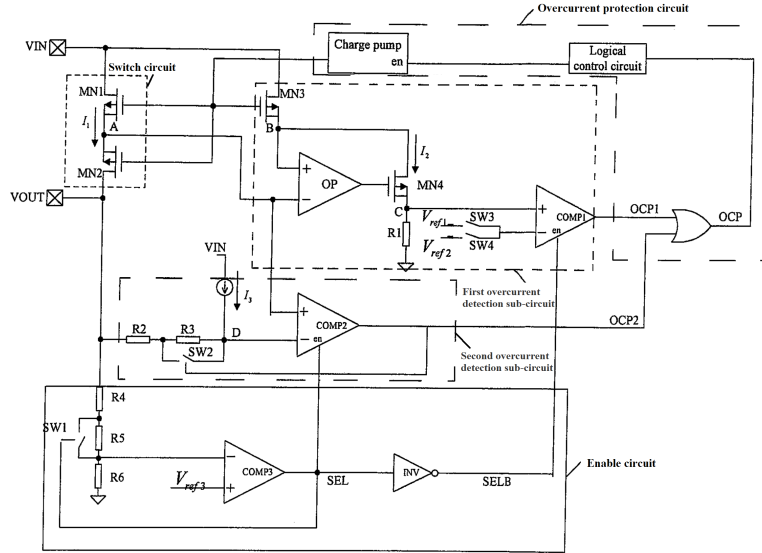


Figure 2.3 A load switch circuit having an overcurrent protection circuitry [34]

Overcurrent protection is another important consideration in load switch systems. In [34], a load switch design that incorporates an overcurrent detection method and a portable device is described. This architecture consists of a switch circuit, two overcurrent detection sub-circuits, an enable circuit, and an overcurrent protection circuit as shown in Fig. 2.3.

As shown in Fig. 2.3, this architecture consists of two overcurrent detection sub-circuits, which detect overcurrent when the output voltage of the switch circuit exceeds or falls below a preset threshold. In practical applications, the first and second overcurrent detection sub-circuits must be configured with a suitable voltage threshold. By defining a too small threshold, the current mirror may not be accurate, which will result in a breakdown of the switch circuit. On the other hand, if a threshold is set too high, erroneous activation of the overcurrent protection may occur, causing the second comparator (COMP₂) to mistakenly activate the overcurrent protection. This disables the switch circuit, preventing the chips from functioning properly. Therefore, the design and implementation of the system require careful consideration, which adds to the complexity of the system.

To sum, all of the structures outlined above are confined primarily to the pass transistor and driver circuitry, as well as some single protection circuits. However, the designers did not take into consideration one of the most important requirements of the load switch structure, which is the monitoring and fault control circuits. In order to monitor and sense the state of the switch, send feedback to the controller (FPGA or MCU), and provide input for fault detection, a readout interface is required. In parallel, the growing demand for compact and high-performance designs is leading to the emergence of SoC-based topology, particularly in industrial atmosphere [35]. Therefore, a load switch interface IC, which provides a smaller footprint than a discrete component-based load switch system, is a promising alternative.

2.2 Electronic Interfacing Technique

A sensor interface IC connects directly to a sensor element and provides the necessary signal conditioning to produce an accurate signal for monitoring and control systems. Due to the diversity of sensor types and operating environments, a variety of methods are available to characterize the interface manner. In this section, we review the literature on the main types of interfacing circuits and select the most robust solutions with the greatest degree of integration.

2.2.1 Analog Amplitude-based Interface

Over the years, analog interface circuits (including analog blocks, e.g., built-in ADCs) have evolved for many types of sensors [5]. These interface circuits consisted of an analog processing chain and discrete components for processing the output signals from an off-chip sensor [4]. Also, due to the development of integrated chip design, these types of techniques were increasingly used in mixed-signal ICs (Application-Specific Integrated Circuit (ASIC)

and SoC) that deal with analog signals [36]. Many low-power applications, including ubiquitous sensor networks, require analog interfaces with various flexible characteristics, such as high-resolution, high-speed, and low-power operation. Towards this end, sensor interfaces, especially wireless sensor nodes, should provide very low power dissipation while maintaining the performance requirements for data conversion units. Therefore, the ASIC or SoC interface must be flexible enough to be able to conform to a variety of requirements and conditions.

In order to address this challenge, modulation/demodulation techniques have been employed in interface circuits. The first automatic readout circuit based on a bridge is described in [37] for differential capacitive sensors that convert capacitive variations into DC voltage. This method can also be applied to inductive sensors, including AC-excited bridges. It transmits amplitude-modulated signals that need to be demodulated and digitized before they can be read by a digital system [38]. The above works, however, have two major drawbacks: a nonlinear input-output relationship and a limited dynamic output range, which means that the interface output reached saturation before full sensor variation was achieved. To cope with these limitations, a redesigned bridge-balancing strategy has been proposed in [39]. By using an improved Voltage Controlled Resistor (VCR), linearization of the I/O relationship as well as full range detection capability were achieved. However, the main drawbacks of this design are its dynamic response and a relatively long feedback settling time.

In resistive sensor applications, the resistive parameter is assessed by applying a voltage across the sensor while reading the current, or vice versa. The voltage or current must then be converted into the digital domain in order to be compatible with a computer, controller, or microprocessor. When resistance variations are small, voltage dividers and Wheatstone bridges are used followed by precision differential or instrumentation amplifiers to reduce the offset voltage. This results in large and complex configurations, requiring linearization techniques due to the inherent dynamic range limitations [40]. Alternatively, quasi-digital converters, i.e., resistance-to-frequency [41], -period [42] or -duty cycle [43] converters, are preferred if the resistance variations are extremely large. This converter provides not only a wider dynamic range but also simplifies the interface to digital systems as no ADC is required. Through the use of a simple digital counter, the resistance is indirectly measured. Most of the quasi-digital converters proposed in the literature focus on achieving a wide dynamic range, however other issues such as robustness and simplicity have not been fully addressed, which is essential for low-cost, low-power readout circuits for practical implementation [44]. To tackle these problems, a ratiometric approach is proposed to ensure robustness to component and power supply variations without increasing complexity [45]. This is a common

method for measuring analog signals from sensors and converting them to a digital signal compatible with a processor [46]. A ratiometric approach has the advantage of not requiring internal regulators, thereby reducing energy consumption and costs. However, the dynamic range of the output is dependent upon the supply voltage, and this would present a major problem in cases where the supply voltage continuously decreases, e.g., in autonomous portable equipment.

2.2.2 Time-based Interface

In recent years, with the demand for low power, low-cost, and small area designs, more innovative integrated on-chip techniques and topologies have emerged to interface the analog physical and digital cyber worlds. Furthermore, the evolution of advanced scaled down semiconductor technologies has largely benefited digital architectures as the reduction in parasitic capacitance greatly improves both power and speed performance, enabling substantial area reductions. Analog circuits, on the other hand, are less scalable and suffer more when applied to nm CMOS technologies. Apart from matching and noise issues, the threshold voltage (V_{th}) is reduced less significantly than the power supply. Thus, analog signals in the voltage domain exhibit a reduced signal swing range [47].

In these circumstances, an appealing approach to obtain low-cost mixed-signal ICs with high timing resolution, high speed and low power is time-domain processing using digital circuitries. Indeed, in a much broader sense, digital circuits, which deal with only two voltage levels (i.e., supply voltage and ground level), can be used not only for “digital signal processing” but also for “time-domain processing” so as to replace conventional analog interface methods like voltage-domain ADC, Operational Transconductance Amplifier (OTA), mixers, etc. A digitally oriented time-based mechanism offers high frequency capabilities, small chip areas, high energy efficiency, scalability to smaller technologies, robustness to process variations, and ultra-low voltage capabilities [48]. As a result, time-based Sensor-to-Digital Converters (SDC) have gained significant popularity in recent years [4, 6, 18].

To realize the described vision, a PLL-based frequency-to-digital conversion mechanism has been proposed [49, 50]. As shown in Fig. 2.4(a), a VCO is used in the PLL-based interface to transform sensor information into frequency information by creating a Pulse-Width Modulation (PWM) signal or clock signal. A digitally steered oscillator provides the reference, so an external reference is not required. This architecture had a similar behavior as traditional Delta-Sigma ($\Delta\Sigma$) ADCs without the need for large analog loop filters. One of its primary advantages is the possibility of replacing a voltage-domain quantizer with a time-domain quantizer that can provide a higher level of timing resolution. Moreover, when the two oscil-

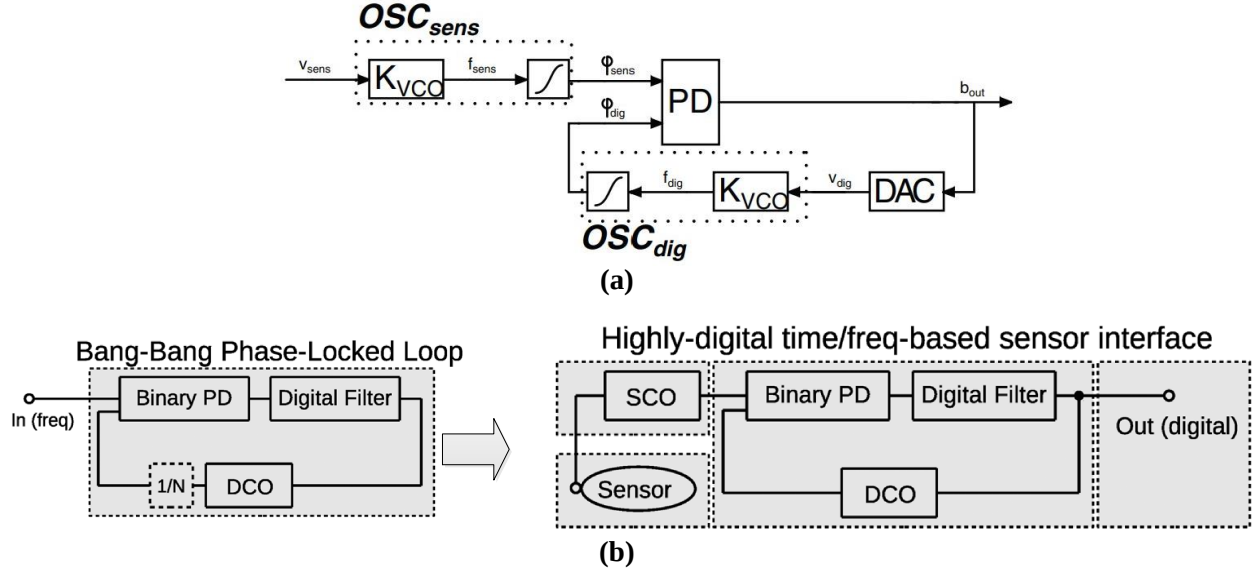


Figure 2.4 Block diagram overview of (a) PLL-based interface architecture [49], and (b) highly digital BBPLL-based sensor interface [50]

lators are well matched, the impact of temperature drift, voltage dependency, etc., is reduced since it results in a common-mode drift of the output frequency of both the sensor-steered and the digitally steered oscillators.

Fig. 2.4(b) illustrates a highly digital interface that is supported by the Bang-Bang Phase-Locked Loop (BBPLL) structure [50]. To employ the BBPLL in a SDC, the sensor signal has been modulated into the frequency domain using a Sensor-Controlled Oscillator (SCO). Depending on the type of sensor (e.g., capacitive), this block may be implemented easily using a capacitance-controlled oscillator. The BBPLL has been used to demodulate the sensor signal to the digital domain, resulting in a highly-digital SDC. As both architectures shown in Fig. 2.4 do not require external reference signals (time or voltage), they are very appealing to fully integrated systems.

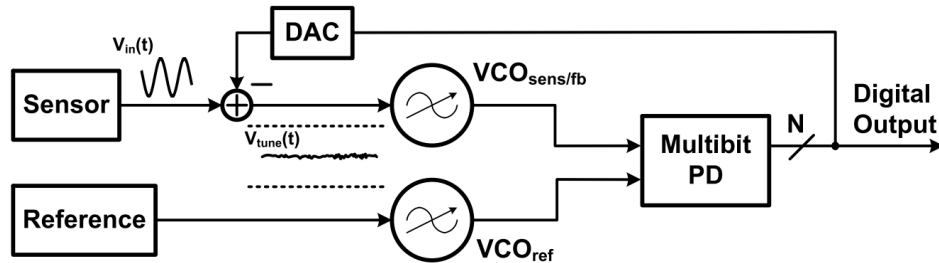


Figure 2.5 Block diagram of the closed loop PLL-based sensor interface architecture [23]

A closed-loop PLL-based sensor interface architectures presented in [23], which its building blocks is shown in Fig. 2.5. The architecture consists of two matched VCOs and a multibit phase detector. The conversion principle is based on the locking of the two identical VCOs: one controlled by a reference voltage and one by a voltage determined by both the sensor and the feedback signal. By operating the system in this manner, the second oscillator period only varies within a narrow range around the first oscillator reference period. In comparison to previous methods, this operating principle provides better linearity and a fixed sampling rate for the system. However, the main limiting factor is still the VCO phase noise, while the speed is strongly dependent on the performance of the PD.

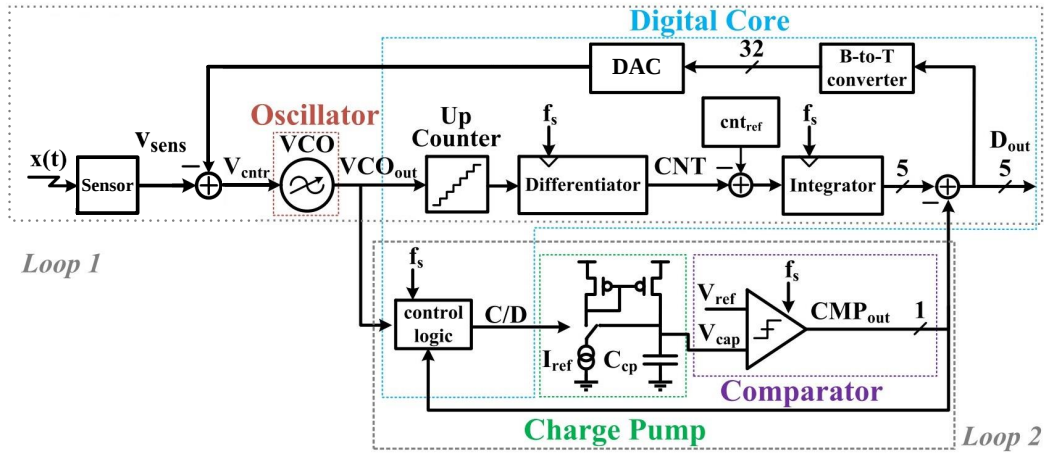


Figure 2.6 Block diagram of the closed loop count-based sensor interface [17]

Recently, a high-resolution sensor-to-digital count-based readout interface is proposed in [17]. As shown in Fig. 2.6, this highly digital time-based architecture includes a VCO, counter, and digital feedback loop for the readout process. In addition to the inherent first-order noise shaping provided by the VCO, the second loop is considered to provide a SMASH configuration and realize second-order noise shaping. The second loop consists of a control logic, a charge pump, and a comparator. The comparator is implemented using a dynamic latch-based comparator and serves as a 1-bit quantizer. The final digital output in SMASH configuration is obtained by subtracting the 1-bit digital output of Loop 2 from the 5-bit digital output of Loop 1. In this architecture, the VCO design demonstrates high linearity and acceptable phase noise performance at the expense of a larger area due to employing a large degeneration resistance. Also, the transient noise in the comparator can jeopardize the integration signal V_{cap} . Therefore, a low noise TD-comparator might relax the noise requirements.

2.3 Time-Mode Electronic Interface Sub-circuits

2.3.1 Voltage-Controlled Oscillator (VCO)

Generally, the main configurations of VCOs are ring type, LC resonant, and relaxation circuit. The high Q resonator of the LC-VCO results in better phase noise performance. There is, however, a limitation to the tuning range of these structures, as well as an inefficiency of complexity, area, and cost due to including the high-performance bulky passive devices [51]. Instead, ring VCOs are more appealing in scaled CMOS applications because of their wide tuning range, smaller silicon area, multiphase output capability, and lower power consumption [52]. However, the main concern with ring VCOs is their nonlinear $f - V$ characteristics and poor phase noise behavior.

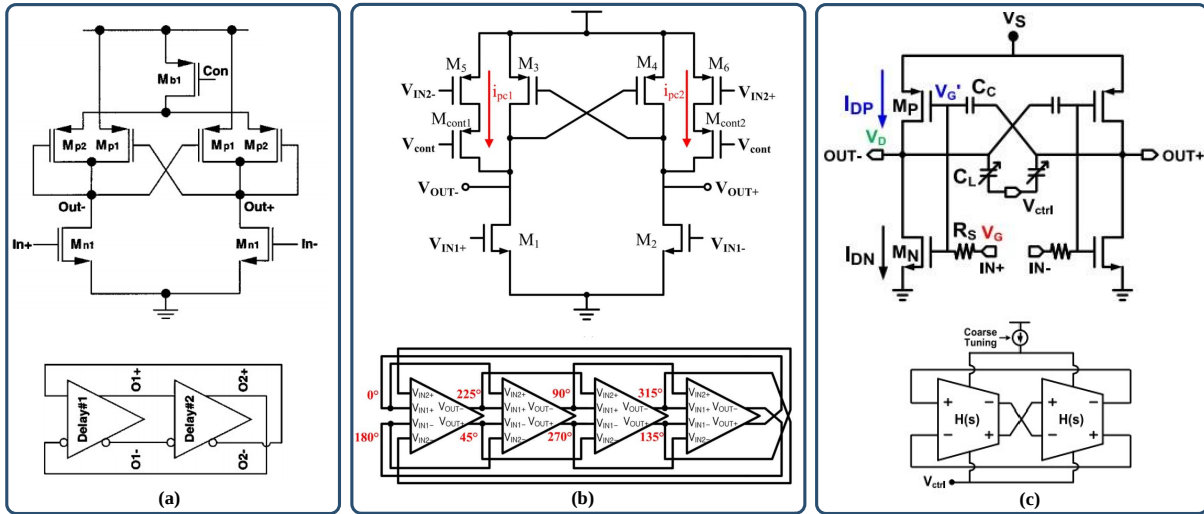


Figure 2.7 Overview over the implemented differential ring VCOs in (a) [53], (b) [51], and (c) [54]

Ring VCOs are commonly divided into two types: single-ended and differential. Fig. 2.7 depicts the schematic of several differential VCOs presented in [51, 53, 54]. To reduce phase noise, authors in [53] propose a 2-stage differential VCO with rail-to-rail voltage swings. However, the delay cells used in their design limit their noise performance by injecting a substantial amount of noise during the transition periods of the VCO. A second study presented in [51] examined the reduction of channel thermal noise at the output node of the VCO during the transition period of the output voltage swing. This VCO performance is restricted as a result of low tuning range and high power consumption. An ultra-low power differential ring VCO was described in [54]. This VCO architecture reduces power consumption through the elimination of the cross coupling latch of the conventional ring VCO. As can be seen

in Fig. 2.7(c), instead of using a latch, the inverters in the delay cell are connected to an additional RC network to produce negative conductance. This delay cell design, however, shows inadequate phase noise performance, a limited tuning range, and a large surface area due to the passive components used. When compared to single-ended VCOs, differential ring VCOs may exhibit greater phase noise at the same power, operating frequency, and delay stage number, and their phase noise performance may even be worse without tail current noise minimization [55]. In contrast, differential ring VCOs provide better common-mode noise rejection while being less sensitive to substrate and supply noises.

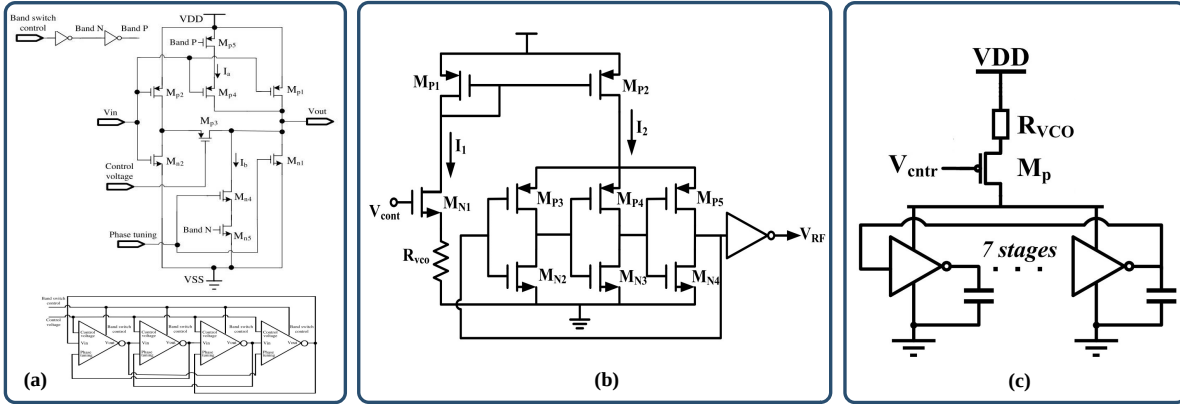


Figure 2.8 Overview over the implemented single-ended ring VCOs in (a) [56], (b) [57], and (c) [17]

Single-ended VCOs have become increasingly popular due to their advantageous characteristics such as simple structure, small area, low temperature coefficient, and wide tuning range. Several single-ended VCO designs have been presented in the literature, most of which are based on simple inverters, current-starved inverters, etc. Schematic diagram of some recent examples of these architectures are shown in Fig. 2.8. In an attempt to improve the performance of the conventional design, a band switch function is employed in [56] in order to suppress control line noise and compensate tuning range. In spite of this, the additional mechanism for controlling the band switch adds to the overall phase noise and incurs power overhead. To enhanced linearity, a the 3-stage ring VCO was presented in [57], where a source degeneration resistor R_{vco} is added to linearize the current through controlling transistor. Despite using a large resistor value that reduces the VCO gain, marginal linearity was achieved in this architecture. Also, there is a poor performance in terms of phase noise. A recent study suggested a simple structure for the VCO based on an inverter chain [17]. As shown in Fig. 2.8(c), to reduce flicker noise, a PMOS tail transistor is selected to convert the control voltage into a current that drives a seven-stage VCO. Also, the R_{VCO} degenerates the PMOS transistor, improves linearity and reduces the $1/f$ corner frequency at the cost

of some gain loss. Although this structure achieved good phase noise performance, it suffers from a large silicon area.

Even though single-ended ring VCOs exhibit good phase noise performance, their sensitivity to substrate and supply noises must be reduced through proper physical layout considerations. Moreover, the rejection of common-mode noise is another important aspect of VCO design. This feature might be suppressed in applications that have two identical oscillators placed closely together. The reason for this is that, when two oscillators are operated in the same physical environment, the related noise appears as a common mode perturbation on their oscillation frequencies [58]. Consequently, these factors should be considered when selecting the proper ring VCO design for a specific application.

2.3.2 Phase-Frequency Detector (PFD)

PFDs play an essential role in many critical applications as they detect both frequency and phase simultaneously, unlike phase detectors which only detect phase transition errors [59, 60]. Therefore, the quality of this design has a significant impact on the overall performance of its applications.

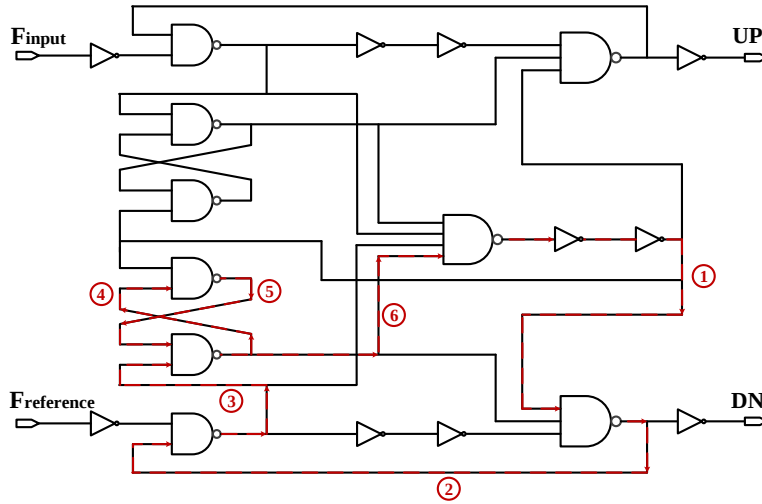


Figure 2.9 The conventional PFD architecture

Fig. 2.9 shows the logic diagram of a conventional PFD. This device suffers from high power consumption, huge silicon area, as well as a non-zero DZ and BZ in phase characteristics, which results in jitters and a restriction on the maximum operation frequency and speed [61]. It is due to the fact that a traditional PFD is an asynchronous state machine, with six reset paths that must be traversed in order to reset the circuit, causing each reset path to slow

down the overall design speed [62]. Therefore, various architectures have been proposed and implemented in literature to overcome these shortcomings.

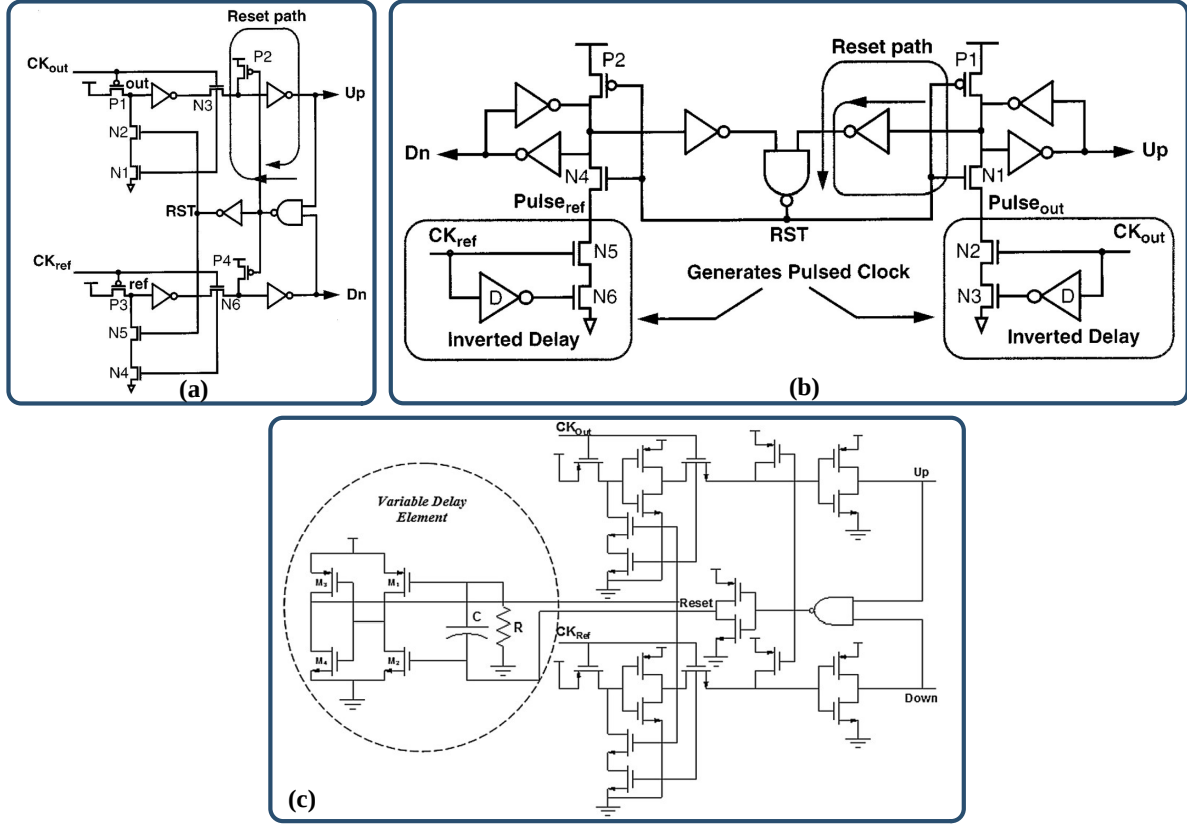


Figure 2.10 The schematic diagram of (a) pass-transistor DFF PFD [25], (b) latch-based PFD architecture [25], and (c) a pre-charged PFD using variable delay element in reset path [60]

In some prior-art PFD designs, in order to overcome the effects of the DZ, some delay was added to the reset path to generate short pulses, as illustrated in Fig. 2.10 [25,60]. The delay of the reset path, however, contributes to the BZ and further restricts the effective range of phase comparison. In addition, a large delay in the reset path will increase phase noise due to the inherently noisy current sources that will be activated for a longer period of time. The latch-based PFD shown in Fig. 2.10(b) achieved a fast frequency acquisition, however it dissipated more power due to short circuit current flows during the reset of the master latch and also failed to operate at high frequencies. The pre-charged PFD design shown in Fig. 2.10(c) improved the DZ and BZ by adjusting the reset delay. However, when there is a significant difference in frequency between the inputs, the latter failed to detect the pulses of the reference signal.

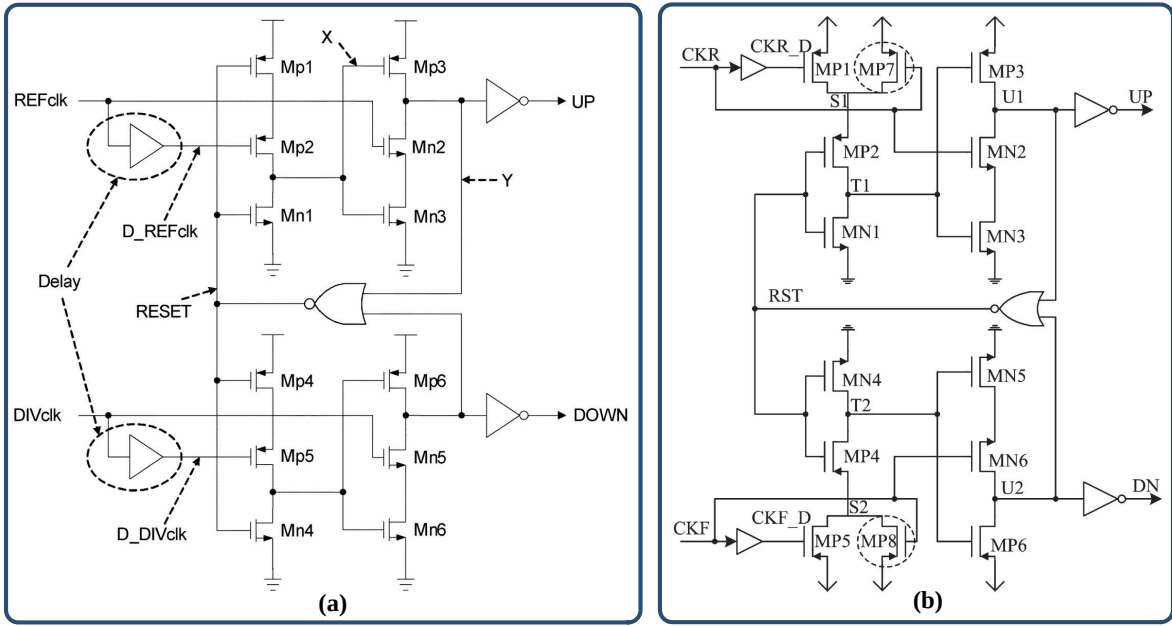


Figure 2.11 Prior-art PFD architectures with delay cells incorporated into the input lines, presented in (a) [24] and (b) [27]

Two PFDs with improved BZ is shown in Fig. 2.11, in which a delay cell is inserted into the input signals path. Using this approach, the PFD responds to incoming edges by shifting the leading pulse up to the end of the reset process. It is necessary, however, that the added delay does not exceed the reset time in order to ensure correct operation. Otherwise, the input pulse that triggers the reset would activate the output after the reset ends, resulting in a failed PFD. Furthermore, the BZ is the difference between the reset time and the additional delay time, which tends to zero if the two times are close together. Nevertheless, the BZ is divided into two main courses, namely the reset time as well as the input node pre-charge time [27]. Pre-charge time takes a considerable amount of BZ if the reset time is greatly shortened. It is also possible that the delayed signal following a reset may not provide sufficient time for charging the internal nodes, resulting in an unwanted state shift at the output.

Another problem with conventional PFDs was that unwanted glitches appeared at the output of the PFDs, resulting in static power dissipation, phase offset, and dynamic jitter [63]. Also, an undesired one-shot pulse might occurs at the beginning of the output signals when inputs rise simultaneously. According to Fig. 2.12, several prior-art designs that have been introduced to overcome glitch and phase mismatch in a PFD by eliminating the reset delay and considering the contrary effect of the second input as well as the first input during the detection of the first output status (UP) [28, 64, 65].

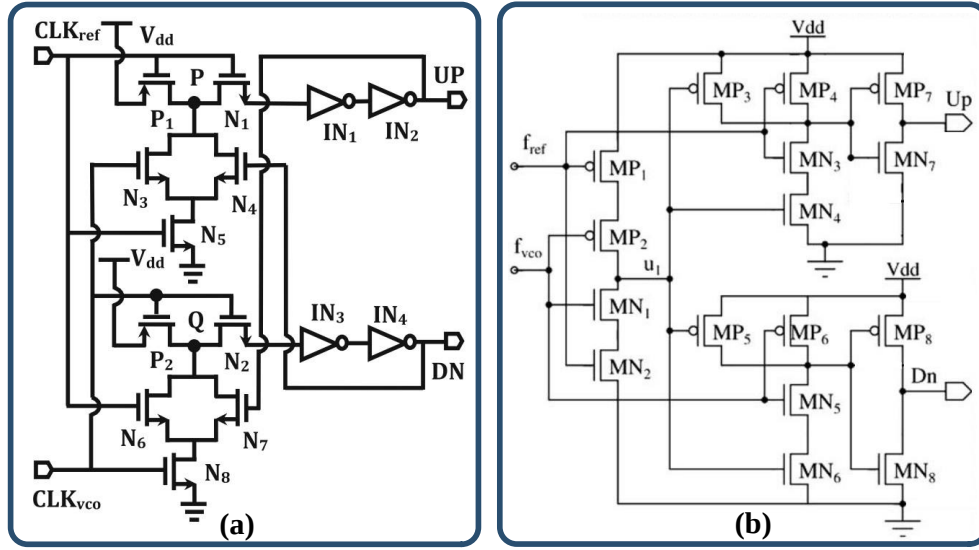


Figure 2.12 Prior-art suggested PFD designs to reduce glitch and undesired pulse presented in (a) [28] and (b) [64]

However, these designs cannot meet the ideal state of PFD because when the second input is high potential and the first input switches to high, the state of the UP output does not change, which idiomatically means the system is blind to the variation in input. In addition, these configurations result in erroneous behavior when the phase difference between the inputs is $|\Delta\phi| \geq \pi$. When π degree phase difference exists, zero signal is produced in the outputs, limiting the phase operation range to $[-\pi, \pi]$. The second issue is that, when $|\Delta\phi| > \pi$, the circuit will not reset and inaccurate signals will be generated at the output, which means the structure is impractical when there is more than π change in the phase.

2.3.3 Time-Domain Comparator

As explained in Section 1.3, TD-comparators have gained considerable attention recently due to their low voltage operation capability, a high time-domain resolution, noise adaptive characteristics, and digital behavior. By using these advanced comparators, the input and reference input voltages are digitized and converted into pulses with frequency-domain information and then compared based on their time/frequency durations. In general, the V2T conversions are performed by Voltage-Controlled Delay Line (VCDL) [66, 67], VCO, etc [19, 20, 68, 69]. Additionally, a phase detector (PD) is required to detect phase transition error, while it can be enhanced by employing a PFD. Due to the use of low-efficiency

building blocks (mainly V2T converter and phase detection units), most prior-art time-based comparators have been limited by their low speed, large offset, and poor jitter performance. They might also suffer from a non-integrable large silicon area because of comprising bulky components (such as capacitors) in order to attain high speed performances [70].

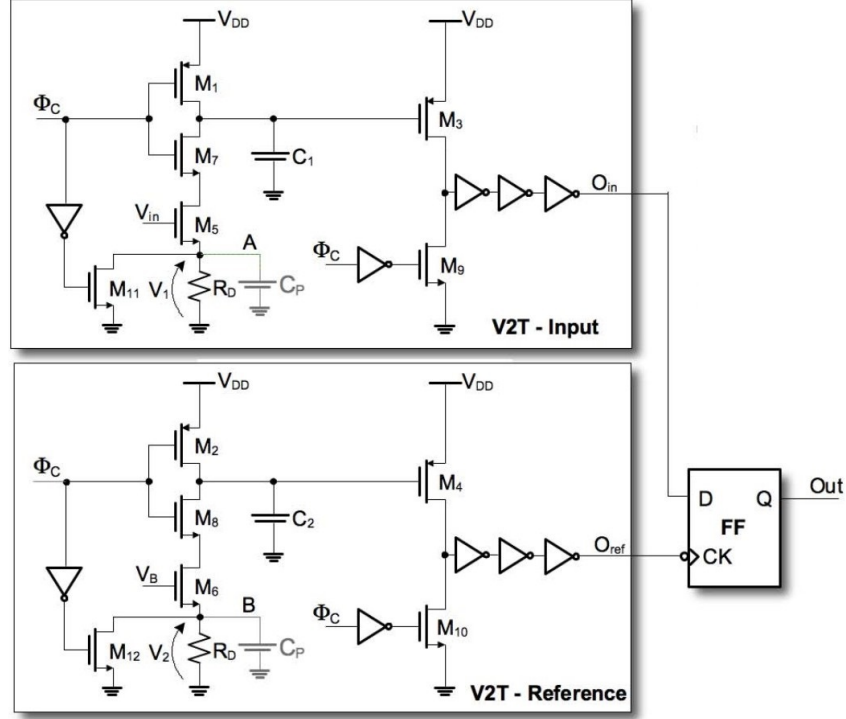


Figure 2.13 Schematic of the TD-comparator based on V2T conversion [71] (©[2008])

Andrea Agnes et al. proposed a TD-comparator based on V2T conversion as shown in Fig. 2.13 [71]. While this design achieved a lower energy consumption compared to traditional comparators, it has several shortcomings. This design utilized V2T units to convert the static state containing a large resistance, while the phase difference is detected by a flip-flop that has an inevitable non-zero setup time and DZ. Furthermore, the comparison procedure can waste a large amount of energy. This occurs because after the comparator has made a comparative result, the V2T conversion circuits continue their operation to be discharged. Therefore, this design exhibited limited speed, power consumption efficiency and precision, and large area.

According to the Section 2.3.2, the DZ and BZ of the PFD block are the primary concerns that have a direct impact on the comparator resolution, speed, noise, and spurious tones. Therefore, several designs attempt to overcome this problem. Fig. 2.14 shows a VCDL-based TD-comparator presented in [66]. The number of delay stages in VCDLs and the value of the load capacitance are increased in this design to boost voltage-to-time sensitivity. A small

input voltage, however, may result in an insufficient time difference between pulses at the output of VCDLs, which falls within the DZ of the employed binary PD. Thus, the VCDL must oscillate until the phase difference reaches a level greater than the DZ. Due to the fact that the number of oscillations and comparison time depend on the level of input voltage, large amounts of power must be consumed.

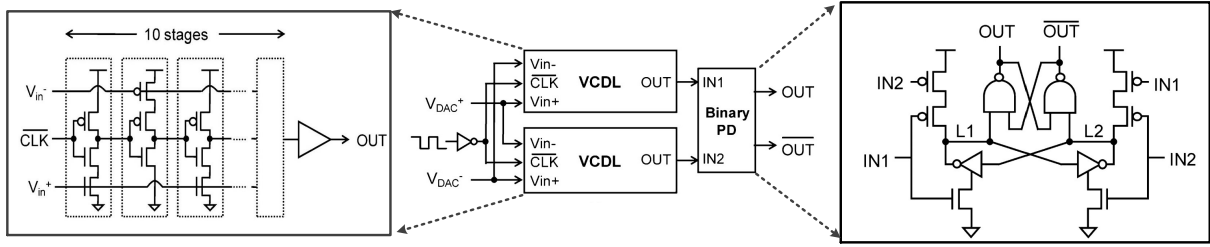


Figure 2.14 A VCDL-based TD-comparator [66] (©[2011])

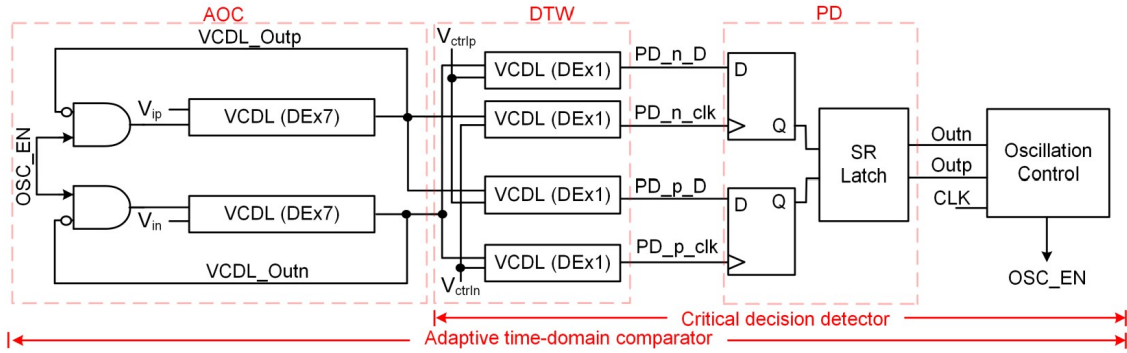


Figure 2.15 An adaptive VCDL-based TD-comparator with differential threshold window (DTW) [67] (©[2018])

Fig. 2.15 illustrates an adaptive TD-comparator design with an adjustable oscillation circuit [67]. A differential threshold window (DTW) technique is used to set the time-domain threshold of the comparator for noise-and-power tradeoff optimization. By using the VCDL with positive feedback, closed loop operation, and a conventional non-minimal DZ PD, the output jitter caused by PD's DZ may be added to the random IRO of the comparator. Therefore, its performance is limited in terms of offset, speed, as well as normalized energy per comparison due to additional circuitries. Furthermore, since flip-flops use different paths for clock and data, the systematic mismatch results in an additional offset delay that can significantly alter by supply voltage lowering.

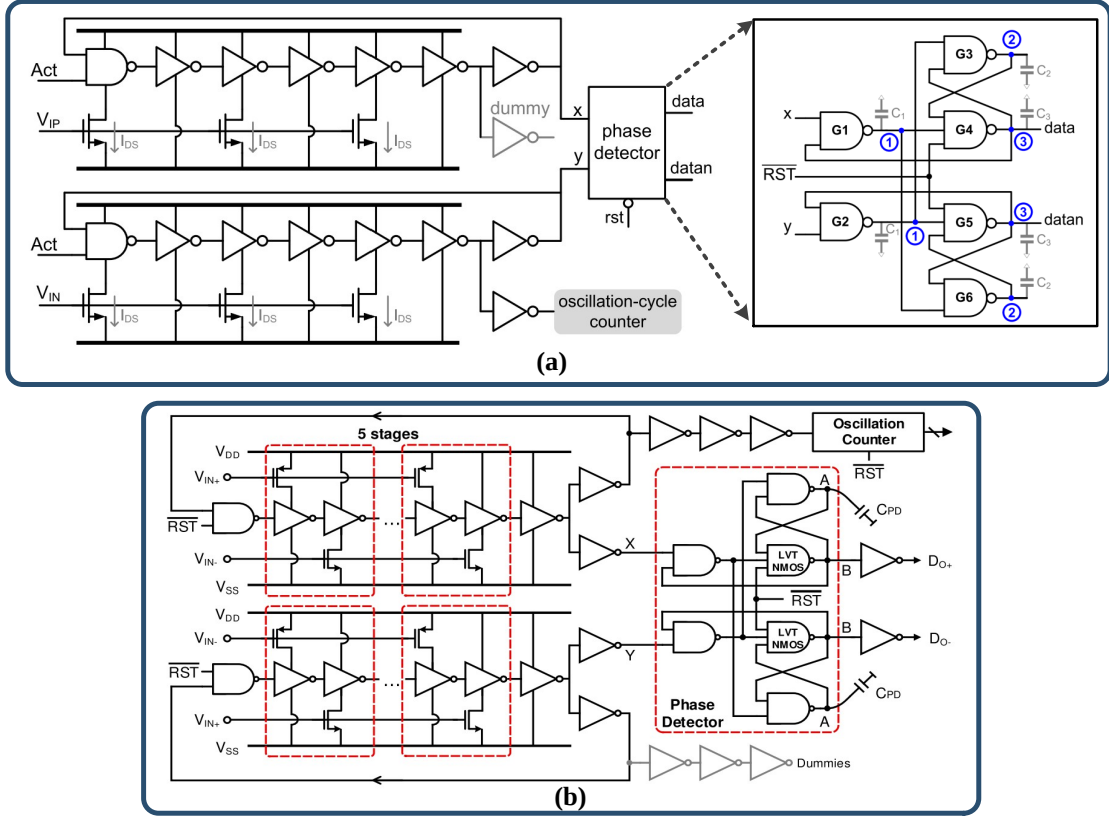


Figure 2.16 Prior-art VCO-based TD-comparators using (a) a bypass window technique [19] (©[2019]), and (b) a oscillation cycle counter [72] (©[2020])

Another type of TD-comparator is based on VCOs, which have the benefit of inherent parallel coarse quantization without requiring any additional cost. Fig. 2.16 shows the schematic diagram of two almost similar closed-loop VCO-based comparator architectures presented in [19, 72]. In [19], a bypassing function has been utilised to overcome the metastability problem caused by non-zero DZ PD. To determine the size of a bypass window, this design requires an oscillation cycle counter and a window-size detection scheme. As the DZ time can be affected by PVT variations, the size of bypass windows may change during operation, negatively impacting the functionality of the system. Similarly, the probability of encountering metastability in the design of [72] is evaluated by observing the Number of Oscillation Cycle (NOC) through a counter. In this architecture, VCO's delay cells with only a PMOS or NMOS input were employed, providing fast resetting paths. However, since transient noise induces early stops, the noise distribution is highly dependent on the DZ of the PD. Thus, higher accuracy may be achieved in both of these structures at a lower speed (higher NOC) and greater silicon area.

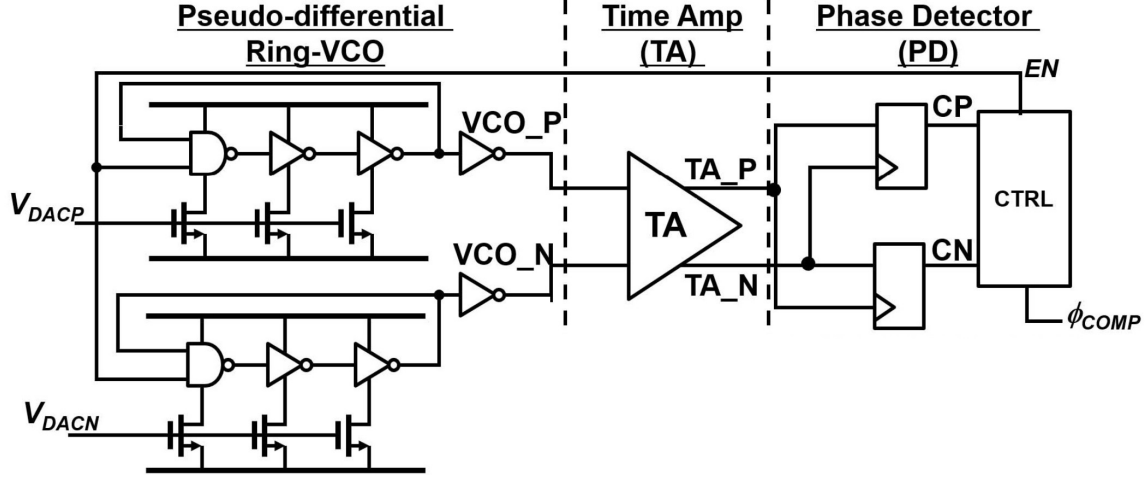


Figure 2.17 A VCO-based TD-comparator employing a time amplifier [68] (©[2021])

Another VCO-based TD-comparator recently proposed in [68]. As can be seen in Fig. 2.17, a time amplifier is employed at the end of the differential VCO to amplify the time difference between the VCO outputs and cancel out the impact of PD's DZ. However, this consideration leads to inefficient energy performance. It is due to the fact that the power-hungry Op-Amp dissipates 16% of the total power consumed by the comparator. Even though the speed of the comparator was improved by the used topology, the additional circuit implementation resulted in a larger area, more noise sources and increased power consumption.

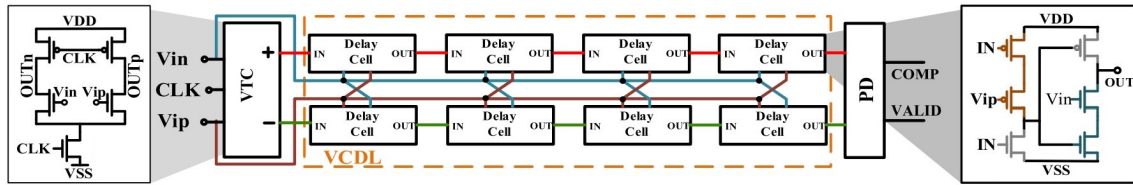


Figure 2.18 A VCDL-based open-loop TD-comparator [73] (©[2022])

A recent work has proposed an open-loop TD-comparator based on VCDL [73], as shown in Fig. 2.18. By using an open loop approach, this implementation realizes a very compact design and eliminates the need for extra counters or bypass window logic to suppress the DZ for higher linearity. However, noise and power efficiency are strongly affected by PVT variations for open loop time-domain comparators. Therefore, closed-loop comparators based on VCOs are usually preferred, since the delay difference in each cycle can be accumulated during oscillation, allowing better noise performance, robustness, and higher SNR to be achieved in the application system.

2.3.4 Pulse Generator and CMOS Thyristor-Based Delay Element

Many applications require pulse generators that generate digital pulse trains or patterns with a constant output pulse width, such as instrumentation systems, audio synthesizers, cryptography bit-extraction, etc. Likewise, a practical pulse generator is also needed for the fault detection control scheme employed in the target load switch interface in order to produce a pulse with a stable and tunable width. There have been several reported methods for implementing pulse generators that include the use of a delay element (DE), an OTA, or a current conveyor-based transconductance in addition to some passive components [74–78]. However, these configurations are characterized by high power consumption, input-dependent performance, limited operation range, and a large occupied area. While DE-based pulse generators are capable of generating monostable pulses, their primary disadvantage is that their DE designs are of low performance.

The main reason for these limitations is that prior-art pulse generator structures typically use inverter chain, RC delay, or differential delay cells. Although non-complex RC delay and inverter chain structures are relatively simple to design, they are highly susceptible to environmental conditions such as temperature variations and power supply noise. Additionally, they are not suitable for delivering a large delay content due to the need to increase the number of inverter stages or add more passive components, both of which result in area and power inefficiencies. A differential delay circuit also consumes significant static power due to the constant conduction of the building transistors. It is therefore necessary to eliminate short circuit currents in order to dissipate less power.

An appropriate alternative to the conventional delay cell is the CMOS thyristor-based delay element (THDE). Using this structure, a pulse generator can be developed that avoids short circuit currents and produces pulse patterns with a wide frequency range. Due to the fact that the current controls the delay rather than the voltage in this architecture, the power supply rejection ratio and temperature sensitivity can be enhanced. Furthermore, power dissipation, including static power, is reduced since the transistors operate in switching mode.

The first THDE concept was introduced in 1996 [79]. As shown in Fig. 2.19(b), this method incorporates a positive feedback mechanism to provide successive operation by settling the output of the delay circuit, making it ready to accept the next input immediately. Also, the biasing technique and the feedback mechanism enhance the sensitivity of the power line. There is, however, a charge sharing problem with this circuit. In addition, any mismatch between the two current sources in this circuit will result in a change in the pulse width of the clock. The THDE architecture presented in [80] rectified these issue by the shown topology in Fig. 2.19(c). Afterwards, the THDE design in [81], improved the delay circuit

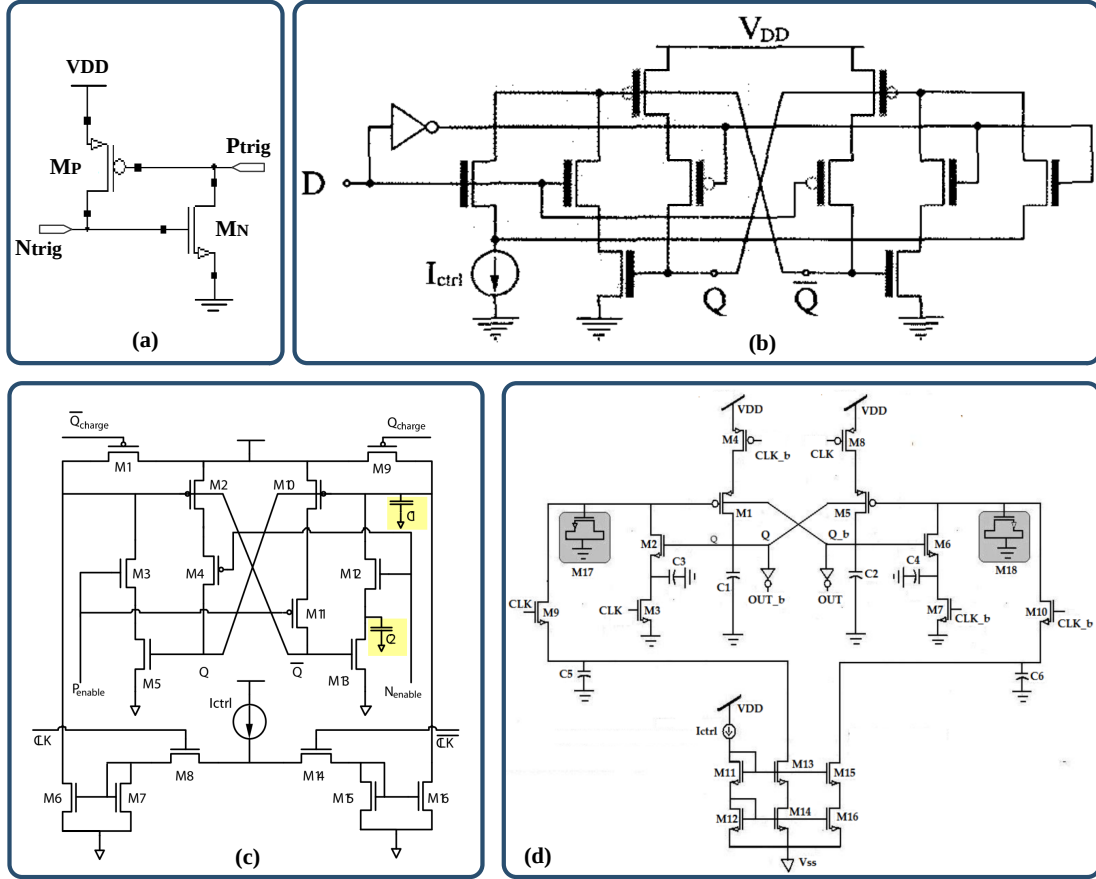


Figure 2.19 Circuit diagram of (a) a CMOS Thyristor, (b) the first THDE [79], (c) a THDE with a charge sharing cancellation technique [80], and (d) a THDE with a improved charge sharing and extended delay range [81]

by modifying the circuit and adding two transistors that act as capacitors as depicted in Fig. 2.19(d). As a result of these additional integrated capacitors, the charge sharing effect is further reduced, since the gate capacitance of the main nodes is increased. Also, it extended the achievable delay range and reduced the circuit sensitivity to power supply noise and temperature variations.

An asynchronous delay cell was proposed in [82] by using thyristor-like circuits. As can be seen in Fig. 2.20, in order to delay timing information asynchronously, a flip-flop, SR latch, and transmission gate were utilized, along with an analog tuning control voltage for setting the delay time. This architecture realized a small-area low-energy DE with no static power dissipation. However, the range of delay is limited.

Fig. 2.21(a) illustrates a voltage-controlled THDE with variable loading capacitors. Input

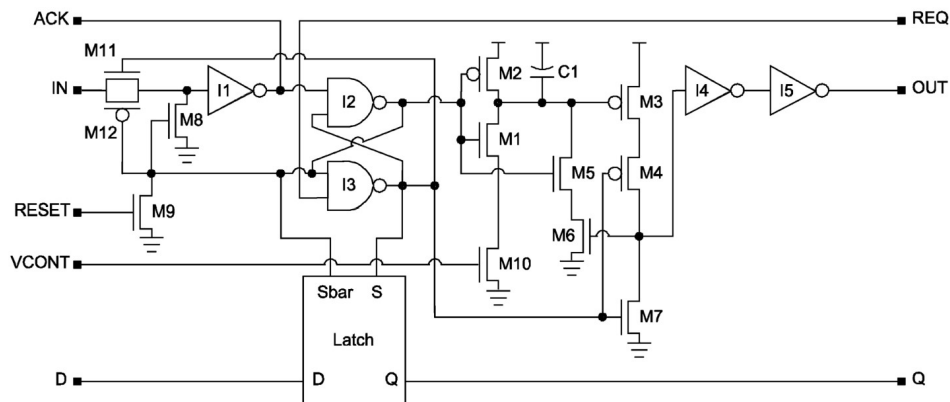


Figure 2.20 Schematic diagram of an asynchronous THDE [82]

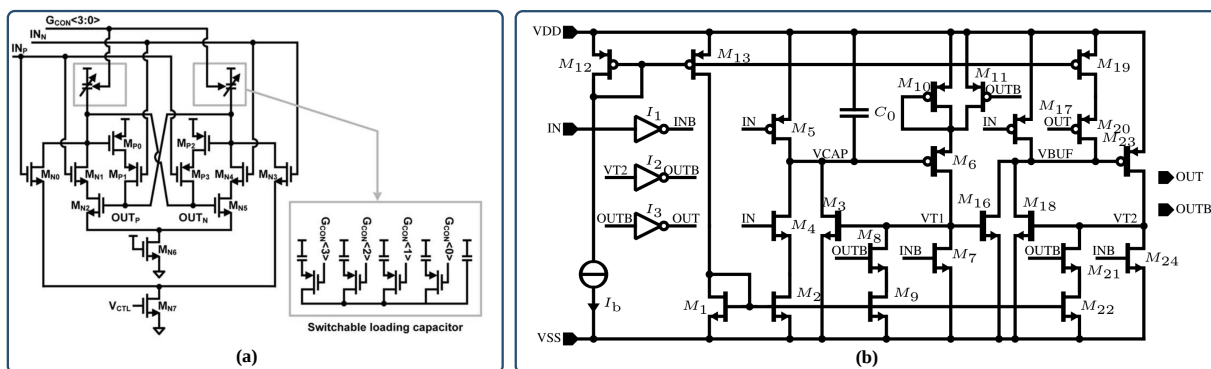


Figure 2.21 Schematic circuit of (a) a voltage-controlled THDE with a switchable loading capacitor array [83], and (b) a THDE with the micro- to millisecond delay range [84]

signal strength is determined by the current flowing through the biasing transistor, which is controlled by an analog control voltage. Through the digitally control of the capacitance of the switchable loading capacitor array, the strength of the positive feedback can be adjusted, thereby changing the delay amounts. This architecture is characterized by a restricted range of delays, high temperature sensitivity, and low accuracy. A low-power THDE with delay durations in the micro- to millisecond range was proposed in [84]. Fig. 2.21(b) shows the schematic diagram of this topology, which employs two CMOS thyristor stages. In the first stage, a diode-connected transistor has been connected in series with the PMOS transistor of the thyristor core to multiply its threshold voltage and achieve a longer delay. However, this improvement is only applicable to a single edge DE, and it cannot be applied to both rising and falling edge delays. Because it leads to a voltage drop at the nodes of the thyristor, which results in a voltage level below the threshold of the output inverters. Therefore, the

output pulses may exhibit a different rise and fall delay and differ in width compared to the input periode. In the second stage, the transition slopes are steepened, which reduces the shunt currents in the following blocks during the switching process. It is noteworthy that this system utilized an ideal current source in order to provide a low current control and minimize power consumption. However, this is not compatible with the requirements of fully integrated, SoC-based designs.

2.4 Summary

In this chapter, a review of state-of-the-art works on various topics related to this thesis has been presented. The load switch circuits have been explored and reviewed as a particular application of this thesis. Then, the prior-art electronic interfacing techniques have been reviewed with an emphasis on time-based interfaces. Considering the potential impacts of sub-block imperfections on the overall readout interface behavior, we have reviewed the most recent circuit implementations of the fundamental components that are involved. The main trade-offs in the design of time-domain circuits are discussed with respect to time-based interfaces requirements. An overview of the different types of VCOs and PFDs is provided that will help the designer in selecting the appropriate type for a given application. We review the majority of available novel and recently developed TD-comparator architectures in the literature, while describing the two prominent types, namely, VCO-based and VCDL-based. An overview of the previous designs approach is provided, as well as their disadvantages and routing causes. Aside from that, another circuit requirements of the aim application is discussed, which are the square-wave generator and the delay element. According to the application specifications, we have found that the thyristor-based design offer the most effective solution. Therefore, a comprehensive background on THDE structures is provided in order to identify the shortcomings of previous approaches. Consequently, several proposed time-domain circuit architectures are discussed in the following chapters to mitigate the mentioned limitations, along with theoretical analysis and analytical equations, simulation and measurement results to evaluate the performance of the proposed designs.

CHAPTER 3 ARTICLE 1 : A LOW-PHASE-NOISE CMOS RING VOLTAGE-CONTROLLED OSCILLATOR INTENDED FOR TIME-BASED SENSOR INTERFACES

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3.1 Abstract

We describe in this paper an improved ring voltage-controlled oscillator (VCO) showing a reduced phase noise while allowing an extended frequency tuning range. The phase noise improvement is obtained through the minimized contribution of tuning line noise while maintaining a rail-to-rail swing. The proposed VCO features a linear tuning characteristic yielding a constant gain over a wide range of operating frequencies. An analytical model is extracted resulting in closed-form expressions for the VCO phase noise. Employing the analytical expressions, the contributed noise and phase noise limitations are fully addressed, and all the effective factors are investigated. The VCO prototype was fabricated in a 0.35 μm CMOS process. It consumes 0.903 mW from a 3.3 V supply when running at its maximum oscillation frequency of 9.37 MHz. The measured VCO phase noise is -147.57 dBc/Hz at 1 MHz offset from the 9.37 MHz oscillation frequency, and the circuit occupies a silicon area of 0.005 mm². A state-variable MATLAB[®] model of a time-based sensor interface has been developed including the impact of phase noise nonideality. The system-level simulations demonstrate that the PLL-based sensor interface exploiting the proposed VCO characteristics can achieve a 88.43 dB signal-to-noise ratio over a 1-kHz bandwidth.

3.2 Introduction

The voltage-controlled oscillator (VCO) is a critical circuit in modern analog and mixed-signal integrated system designs such as phase-locked loops (PLLs), clock/data recovery, frequency modulation/demodulation, on-chip clock distribution, and synchronizing circuits [56, 57, 85, 86]. Over the past decades, the semiconductor industry has been directed towards smaller technologies that are especially effective for digital circuits while raising some difficulties in

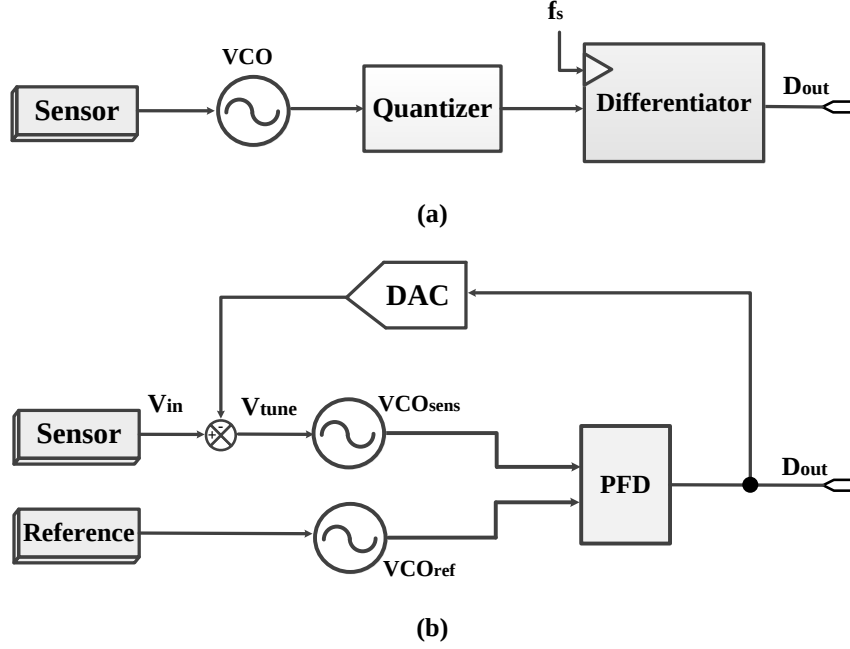


Figure 3.1 Block diagram of two types of VCO-based sensor interfaces: (a) the count-based open-loop [21], and (b) the PLL-based closed-loop sensor interface [23]

designing analog systems [2,3]. Supply voltage reduction, weak intrinsic transistor properties (e.g., lower gain and devices' mismatch), large power and chip area result in poor portability of purely analog solutions to other technology nodes [4]. Therefore, time-based and digitally-oriented structures became increasingly popular among electronic research trends.

Moreover, VCO-based architectures are of great interest in time-based integrated circuits (ICs) such as time-domain comparators, analog-to-digital converters (ADCs), time to digital converters, time-based sensor interfaces, etc. This stems from the fact that VCOs offer highly digital, energy-efficient, and scalable solutions [19]. Also, they realize relatively simple configurations of multi-bit noise shaping in A/D conversion or quantizer in delta-sigma modulator [87,88]. Fig. 3.1 conceptually illustrates the VCO's function in two important types of time-based sensor interfaces or sensor to digital converters. The inherent first-order noise-shaping property of the VCO makes it an essential circuit in these interfaces. The highly digital scalable implementation of these interfaces has gained much attention due to their potential for compactness, portability, and power efficiency [6, 18, 50, 89].

The most common techniques to implement VCOs are ring structures, LC resonant configuration, or relaxation circuits [51, 90, 91]. LC-VCOs exhibit better phase noise performance owing to the high Q resonator. However, besides the limited tuning range of these structures, adding high-performance bulky passive devices (such as inductors) to a CMOS process leads

to chip complexity, and area and cost inefficiency [51]. On the contrary, ring VCOs are a popular alternatives in scaled CMOS technologies since they offer a wide tuning range, less die area, straightforward integrated design, multi-phase output capability, and good power performance [52]. Consequently, a ring-type VCO is a promising approach for voltage-to-time conversion, frequency translation, and generating required periodic signals for timing in digital circuits that are widely used in industrial platforms.

However, nonlinear performance and poor phase noise are the key issues in ring VCOs. For instance, the nonlinear nature of voltage-to-time conversion provokes a linearity issue in a time-domain comparator, and the VCO phase noise has a great impact on its resolution [19, 20]. Besides, the performance of VCO-based ADCs is severely distortion limited by VCO gain variation (tuning nonlinearity) that causes an inter-stage gain error [92]. Moreover, in an open-loop VCO-based sensor interface shown in Fig. 3.1(a), the VCO's nonlinearity leads to the appearance of harmonic spurs in the output spectrum and limits the overall system signal-to-noise ratio (SNR) [21, 22]. To tackle this issue, the closed-loop interface architecture depicted in Fig. 3.1(b) is usually employed [23]. Although the VCO in a loop ensures higher linearity, the operating frequency range is narrowed, and the additional feedback network results in a low conversion speed, a larger area, and an increased power budget [58]. The limiting factor in these close-loop time-based interfaces is the VCO phase noise [23]. As a result, an on-chip VCO design with improved linearity correction, less gain variations, low phase noise, and full-swing is significantly required in any analog/digital applications.

Generally, there are two types of ring VCOs: single-ended and differential. Single-ended VCOs are widely used in digital nature applications due to their low complexity, smaller area, lower temperature coefficient, and wider tuning range. Also, a differential ring VCO may show larger phase noise compared to a single-ended VCO at the same power, operation frequency, and the number of delay stages. While, its phase noise performance could even be worse without tail current noise minimization technique [55]. In contrast, differential ring VCOs offer better common-mode noise rejection with a lower sensitivity to substrate and supply noises. In a single-ended ring VCO, these sensitivities can be reduced to some extent through proper layout design consideration. In addition, in the closed-loop time-based sensor interface shown in Fig. 3.1(b), the common-mode sensitivity of the single-ended VCO can be suppressed by having two identical oscillators laid out close together. It is due to the fact that when two oscillators operate in the same physical environment, the related noise appears as a common mode perturbation on their oscillation frequencies [58]. Therefore, the above factors should be considered when selecting the appropriate design of ring VCO for a particular application.

In an attempt to obtain a VCO with low phase noise, authors in [53] promote rail-to-rail voltage swings. However, their employed delay cells limit the noise performance by injecting a substantial noise during the VCO's transition periods. Another study presented in [51] focused on reducing injected channel thermal noise in transistors during VCO's output transitions. Nevertheless, the VCO performance remains limited due to the low-frequency tuning range and the large power consumption. A band switch function is employed in [56] to suppress the control line noise and compensate for tuning range. However, the additional mechanism for band switch control increases the overall phase noise while suffering from power overhead. An ultra-low-power ring VCO was reported in [54]. It uses a differential delay cell to generate negative conductance without requiring the cross-coupled latch. This design suffers from an unattractive phase noise performance, a low frequency tuning range, and a large occupied area due to the passive components used in the delay cell implementation.

This work presents a compact, wide-swing, enhanced phase-noise, and low-power CMOS ring VCO. The delay elements used in the proposed VCO show a full-swing output, a linearized characteristic, and a steady gain. A theoretical analysis considering the impact of intrinsic and extrinsic sources of noise has been developed to study the VCO phase noise. Also, the effectiveness of this architecture is validated through a MATLAB/SIMULINK model of a closed-loop PLL-based sensor interface. The rest of the paper is organized as follows: Section II describes the general phase noise definitions for ring-type VCOs. The design and the theoretical analysis of the proposed VCO architecture are revealed in Section III. Section IV presents the measurement results of the fabricated VCO, while Section V discusses the proposed VCO's performance compared to the prior art and examines its potential in a time-based sensor interface by employing a state-variable MATLAB[®] model. The conclusion is drawn in Section VI.

3.3 Phase Noise In The Ring Oscillator Design

There is an inherent trade-off between ring oscillators' diverse properties, including phase noise, tuning range, linearity, gain, voltage swing, power dissipation, and supply voltage. In a practical VCO, noise sources add uncertainty to zero crossing times and create a variable interval between transitions known as jitter. As a result of the time-domain deviation from perfect periodicity, oscillation frequency varies from the ideal constant, causing a nonuniform output phase. In the frequency domain, this short-term instability or random fluctuations in the phase of an output signal is defined as phase noise [93]. Phase noise induces various interferences and errors in integrated circuits' functionality, so it is a leading concern in a VCO circuit design.

Several models have been developed to quantify these fluctuations, analyze the phase noise of the oscillator, and characterized it in terms of the normalized single side-band (SSB) noise spectral density [55, 93–95]. According to the type of devices used to implement the VCO, the contributing noise sources can be thermal noise of parasitic resistance, thermal noise of transistors' channels, and transistors' flicker noise ($1/f$ noise) which is responsible for the phase noise at low frequency. Since the band of interest for most applications is usually dominated by white noise and flicker noise, the VCO phase noise power spectral density (PSD) can be represented as a simplified model of [89, 96]

$$\mathcal{L}\{\Delta f\} = \frac{b_{-2}}{\Delta f^2} + \frac{b_{-3}}{\Delta f^3}, \quad (3.1)$$

where b_{-2} and b_{-3} are the noise levels for the white and the flicker noise dominated regions, respectively.

As noted earlier, phase noise and jitter are different ways of quantifying the same phenomenon. Several attempts have been made to link these two parameters, resulting in a direct relationship that holds for white noise sources. Therefore, to analyze the effect of white noise on the phase noise of a VCO, the time-domain jitter calculation method is often used [95, 97]. In the presence of $1/f$ noise, however, the assumption of uncorrelated sources of jitter between successive oscillator periods is no longer valid [55]. So, it is difficult to determine the correlation between the jitter of transitions, induced by low-frequency noise sources, over multiple cycles. Therefore, to account for flicker noise, a straightforward circuit analysis on random VCO modulation is preferred [95].

The output oscillation frequency of a VCO is determined by its control voltage through the VCO gain (or sensitivity), K_{VCO} . Suppose an injected voltage noise at the tuning node of the oscillator. For a given noise amplitude, the noise in the output frequency is amplified by K_{VCO} . Clearly, it will affect the noise spectral density and thereby the phase noise behavioral model. Accordingly, the flicker noise impact on phase noise can be determined by considering the direct modulation of oscillation frequency caused by the circuit transfer function. As any noise generated in the control scheme can provoke additional phase noise, it is necessary to examine the disturbance of the output phase and frequency arising from the circuit's integrated noise and the extrinsic noise accompanied by the control voltage. We leverage these principles to find the phase noise expression for the proposed VCO, which is described in detail in section 3.4.3.

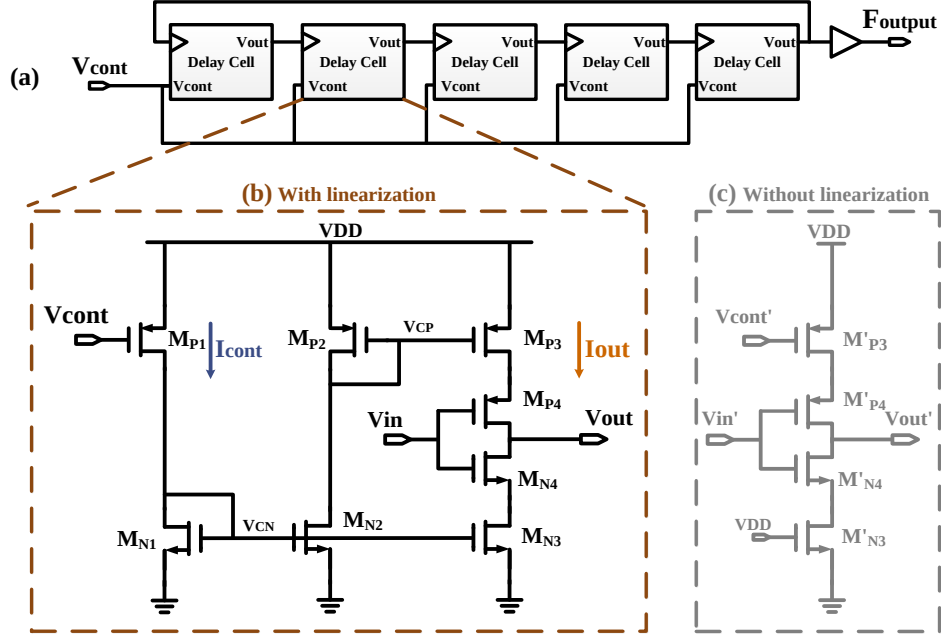


Figure 3.2 (a) Block diagram of the proposed ring VCO, (b) schematic of the proposed delay cell with linearization, and (c) delay cell without linearization

Table 3.1 Aspect ratio of the used transistors

Transistor	W/L (μm)	Transistor	W/L (μm)
M_{P1}	4/7	M_{N1}	5/0.5
M_{P2}	8/4	M_{N2}	5/0.5
M_{P3}	5/4	M_{N3}	3/0.5
M_{P4}	5/5	M_{N4}	2/5

3.4 Proposed VCO Architecture

Fig. 3.2(a) presents the architecture of the proposed VCO. It consists of five delay cell stages in addition to a buffer at the output of the VCO to sharpen the generated signal and drive the VCO load. The implementation of the proposed linearized delay cell is illustrated in Fig. 3.2(b). In each current-starved delay cell, the control voltage (V_{cont}) is applied to the voltage-controlled current source M_{P1} and the resulting current, I_{cont} , is mirrored to the inverter (constructed from M_{P4} and M_{N4}) through the current mirror M_{N1} , M_{N2} , and M_{P2} . The replica current source M_{P1} in each stage dynamically biases the current-starved inverter and avoids current variation at I_{cont} which may lead to some linearity error. Also, the replicated current mirror is chosen to transfer the current and clamp the voltage of nodes with high parasitic capacitance and assure that currents in each stage are equivalent and a full swing can be attained at the output of the delay cell.

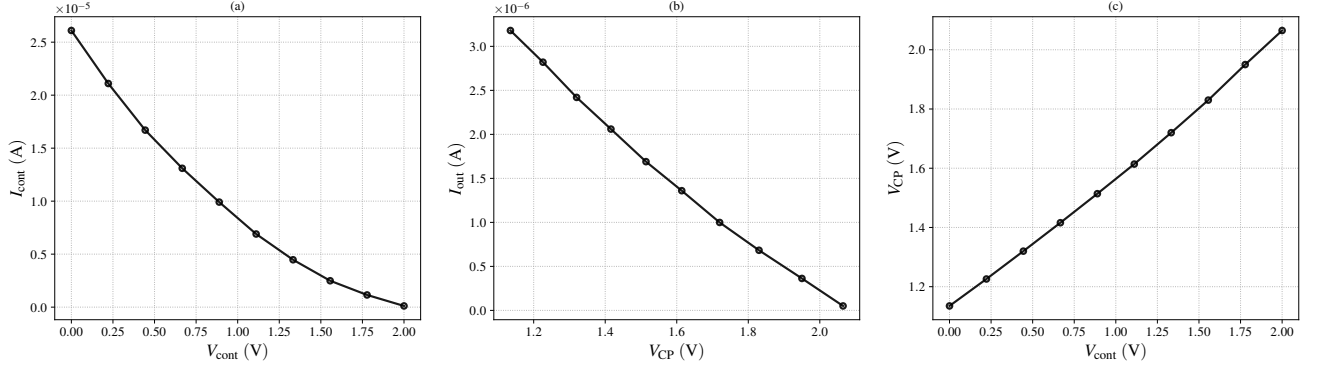


Figure 3.3 (a) Controlling current versus tuning voltage, (b) average output current versus the biasing voltage V_{CP} , and (c) the biasing voltage versus voltage control

The target point of this VCO design is to generate pulse signals up to 10 MHz; thus, five delay cells ($N = 5$) are found to be sufficient to cover this range of frequency. Also, fewer number of delay cells mitigates phase errors that might be added due to the mismatch of delay cells [22]. Transistors' aspect ratios shown in Table 3.1 are considered for the constituent transistors of the VCO delay cells.

3.4.1 Linearization

For a single-ended VCO, the oscillation frequency is primarily realized by the number of stages (N) and the average propagation delay (t_p) of delay cells, as

$$f_{\text{osc}} = \frac{1}{\tau} \simeq \frac{1}{2N \cdot t_p}. \quad (3.2)$$

The propagation delay is measured when the output signal crosses the toggle point, which is assumed to be in the middle of transition at $V_{\text{DD}}/2$. According to the proposed design, the j^{th} delay cell can be viewed as the operation of an inverter with a pull-up and pull-down current supplies, I_{P_j} and I_{N_j} respectively. So, the oscillation frequency in the j^{th} delay cell of an N -stage ring VCO can be calculated as [95]

$$f_{\text{osc}} = \frac{2}{V_{\text{DD}} \cdot C_{\text{tot}}} \left(\sum_{j=1}^N \frac{1}{I_{N_j}} + \frac{1}{I_{P_j}} \right)^{-1}, \quad (3.3)$$

where C_{tot} is the total parasitic capacitance seen at the output of each delay element [97].

Supposing $I_{N_j} \simeq I_{P_j} \simeq I_{\text{out}}$, the nominal frequency of oscillation is given by

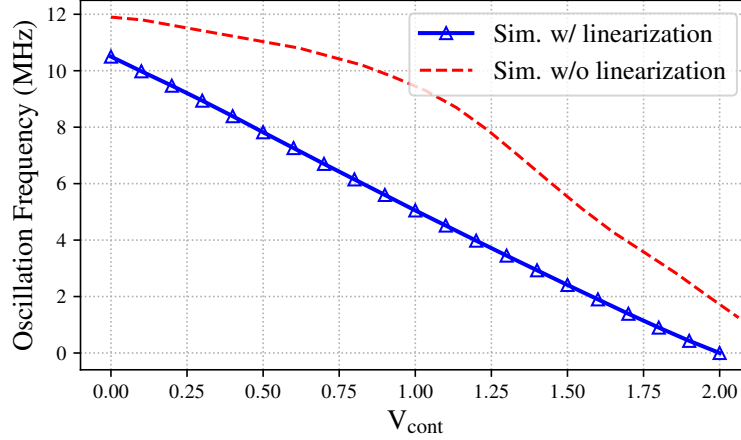


Figure 3.4 Simulated VCO output frequency versus its control voltage with and without the linearization method

$$f_{\text{osc}} = \frac{I_{\text{out}}}{N \cdot V_{\text{DD}} \cdot C_{\text{tot}}}. \quad (3.4)$$

Therefore, the output frequency of a ring VCO is directly related to the current supplied to the inverter branches. Fig. 3.2(c) shows the conventional current-starved delay stage without linearization, where the control voltage applied to the pull-up PMOS (M_{P3}), and M_{N3} remains always on. In this design the gate-source voltage of M_{P3} , $V_{\text{GS}_{P3}}$, determines the VCO control voltage and the current flowing through it is related to $V_{\text{GS}_{P3}}^2$. This results in a nonlinear output current with respect to V_{cont} , and hence a nonlinear output frequency. Thus, to enhance the linearity of the $f_{\text{osc}} - V_{\text{cont}}$ characteristic in a VCO, a linear current (with V_{cont} variation) should be supplied to the inverter stacks of the delay cells.

In the proposed delay cell implementation, shown in Fig. 3.2(b), this nonlinearized circuitry is rectified by means of entering V_{cont} to a voltage-controlled current source, M_{P1} , and using a current mirror biased in strong inversion. As depicted in Fig. 3.3(a), owing to the saturation-operating of M_{P1} , the resulting control current, I_{cont} , shows a nonlinear behaviour with V_{cont} . To compensate for this nonlinearity, the current mirror transistors are designed to transfer a linear biasing voltage (V_{CP} or V_{CN}) as functions of V_{cont} to the load transistors M_{P3} or M_{N3} in the pull-up or pull-down operation, respectively.

Considering the pull-up network activation moment, the load transistor M_{P3} is biased in the triode region, and its drain-source current equals I_{out} . So, the output current of the proposed VCO is linearly related to its $V_{\text{GS}_{P3}}$ and, hence, to its bias voltage V_{CP} (see Fig. 3.3(b)). This feature, along with the linear behavior of V_{CP} versus the controlling voltage V_{cont} (see

Fig. 3.3(c)) ensures that the proposed VCO maintains a linear relationship between I_{out} and V_{cont} and controls the frequency response nonlinearity. Fig. 3.4 shows the operation frequency of the proposed VCO with and without the linearization versus its control voltage. As can be seen, a good enhancement in the VCO linearity compared to the design without the proposed linearization is obtained.

3.4.2 VCO Gain

The VCO's gain is defined as

$$K_{\text{VCO}} = 2\pi \frac{\partial f_{\text{osc}}}{\partial V_{\text{cont}}} . \quad (3.5)$$

Since the propagation delay time is estimated by the average output tail current going through the output capacitance, the gain can be expressed as

$$K_{\text{VCO}} = 2\pi \frac{\partial I_{\text{out}}}{2 \cdot N \cdot V_{\text{sw}} \cdot C_{\text{tot}} \cdot \partial V_{\text{cont}}} . \quad (3.6)$$

where V_{sw} is the voltage swing of V_{out} . It is noteworthy that V_{sw} may be reduced at a quite small I_{out} due to slowed swing and increased voltage headroom of MOS transistors. Since the minimum operation mode in the proposed VCO is around 100 kHz, V_{sw} can be assumed to be independent of the bias current and V_{cont} at such range. On the other hand, in contrast to some conventional ring VCOs which are tuned by supply voltage variation, the proposed delay cell boosts the output swing by coupling the control signal to the gate of the current source transistor, M_{P1} . This bias-controlled voltage/current configuration is optimized in such a manner that the current mirror transistors remain in the saturation region for the entire control voltage range and the load transistors in the inverter tail make a narrow voltage headroom. Hence, a maximized voltage swing and a wide tuning range are obtained.

Therefore, the current-source biasing leads to a high steepness in transition slope, faster transition, output swing augmentation, and tuning range improvement. These features in addition to the optimized MOS sizing diminish the VCO gain. As explained in section II, reducing the gain can decrease the phase fluctuation due to low-frequency noise in components and the control terminal. However, to achieve a reasonably wide tuning range, a large K_{VCO} is required [56]. Thus, for applications that require low phase noise and a wide tuning range, manufacturers typically design oscillators with a moderate gain and a large input voltage range to satisfy these conflicting requirements at the cost of power consumption. Lowering the K_{VCO} has a minimal impact on the functionality of the proposed VCO since the required frequency tuning range is only from 0.01 MHz to 10 MHz over a 2 V input range.

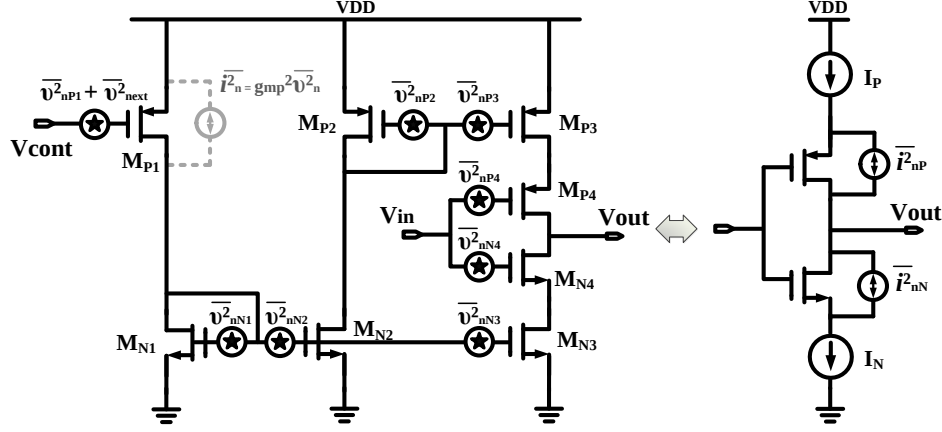


Figure 3.5 Equivalent noise circuit of the proposed delay cell

3.4.3 Noise Analysis

To derive the proposed VCO's noise contribution, the generated noise by means of each delay stage has to be first calculated. Likewise, the extrinsic noise at the control line should be included in the total noise associated with the circuit. The noise in the MOSFETs can be referred to the gate as a series noise voltage source with a PSD of $\overline{v_n^2}$ (or equivalently noise current source $\overline{i_n^2}$ across the drain) [94]. By considering the M_{P1} reflected current to the current-starved inverter stacks, the equivalent noise transfer model of the proposed delay cell can be illustrated as shown in Fig. 3.5. It is worth mentioning that pull-up and pull-down currents incorporate the uncorrelated noise effect of M_{P1} and the current mirror transistors.

Phase Noise Due to White Noise

The uncertainty in propagation delay of the proposed VCO can be modeled in the output current I_{out} across the C_{tot} . This current is accompanied by a noise current source with a white noise spectral density of $\mathcal{S}_{i_n}^w = \langle \overline{i_n^2} \rangle = 4k_B T \gamma g_m$, where coefficient γ is typically equal to 2/3 for long-channel transistors. $\overline{i_n^2}$ would result in a Gaussian distribution of the propagation delay (t_p), which can be referred to as timing jitter. The total variance of the period jitter in view of the uncertainty in rising edge ($t_{p_{rise}}$) and falling edge propagation delay ($t_{p_{fall}}$) can be calculated as

$$\sigma_\tau^2 = N \cdot \left[\sigma_{t_{p_{rise}}}^2 + \sigma_{t_{p_{fall}}}^2 \right], \quad (3.7)$$

where the variance of the jitter due to the uncorrelated white noise is $\sigma_{t_p}^2 = \frac{\overline{i_n^2}}{2I_{out}^2} \cdot t_p$ [97].

Using equations (3.7) and (3.2), the total period jitter approximated as

$$\sigma_\tau^2 = \frac{2 \cdot k_B \cdot T}{I_{\text{out}} \cdot f_{\text{osc}}} \left[\frac{\gamma_n}{(V_{\text{DD}} - V_{\text{th}_n})} + \frac{\gamma_p}{(V_{\text{DD}} - V_{\text{th}_p})} \right]. \quad (3.8)$$

The general relationship between phase noise and jitter, where the phase noise is dominated by white noise, is [23, 50, 95]

$$\sigma_c^2 = \mathcal{L}\{\Delta f\} \cdot \frac{\Delta f^2}{f_{\text{osc}}^3}. \quad (3.9)$$

Therefore, the SSB phase noise of VCO due to white noise can be estimated as

$$\mathcal{L}\{\Delta f\} = \frac{2k_B T}{I_{\text{out}}} \cdot \frac{f_{\text{osc}}^2}{(\Delta f)^2} \left[\frac{\gamma_n}{(V_{\text{DD}} - V_{\text{th}_n})} + \frac{\gamma_p}{(V_{\text{DD}} - V_{\text{th}_p})} \right]. \quad (3.10)$$

Phase Noise Due to flicker Noise

Flicker noise should be interpreted differently than white noise since its fluctuation rate is much lower than the oscillation frequency, and it relies on distinct mechanisms of phase noise and jitter [95]. From the principal analysis, explained in section II, input noises can be multiplied with the modulation sensitivity, yielding the frequency deviation that can be translated to an equivalent RMS phase deviation. Therefore, the SSB spectral density caused by a given noise in the VCO can be written as [95]

$$\mathcal{L}\{\Delta f, K_{\text{VCO}}\} = \mathcal{S}_{v_n}(\Delta f) \cdot \frac{K_{\text{VCO}}^2}{4 \cdot \Delta f^2} = \frac{\langle v_{n_T}^2 \rangle \cdot K_{\text{VCO}}^2}{4 \cdot \Delta f^2}, \quad (3.11)$$

where v_{n_T} represents voltage noise sources in series with circuit branches. It composes the channel integrated noise as well as the external noise at the VCO tuning node, which modulate the carrier frequency.

The delay is directly modulated by the flicker noise associated with pullup and pulldown current supplies. Therefore, according to (3.3) and (3.11), the equivalent SSB phase noise due to flicker noise contribution can be written as [95]

$$\mathcal{L}\{\Delta f, K_{\text{VCO}}\} = \mathcal{S}_{i_n}^{1/f}(\Delta f) \cdot \frac{K_{\mathcal{I}}^2}{4\Delta f^2} = \langle i_{n_T}^2 \rangle \cdot \frac{(\partial f_{\text{osc}} / \partial I_{N_k})^2}{4\Delta f^2} = \frac{1}{4\Delta f^2} \left(\frac{f_{\text{osc}}}{2 \cdot N \cdot I_{\text{out}}} \right)^2 \cdot \overline{i_{n_T}^2}, \quad (3.12)$$

where $\mathcal{S}_{i_n}^{1/f}(\Delta f)$ is spectral density of flicker noise in the inverter line current and $K_{\mathcal{I}}$ is the sensitivity of f_{osc} to the pull-up (or pull-down) current.

Concerning the control-line noise contribution in the phase noise of the VCO, an extrinsic noise coming from other components or circuitry with a PSD of $\overline{v_{n_{\text{ext}}}^2}$ has been assumed at the tuning gate of M_{P1} . This noise will be added to M_{P1} voltage noise ($v_{n_{P1}}$) and mirrored to the inverter line current noise with the mirroring factor of the κ_m . As a result, the total input noise current density is arisen from the current fluctuations of inverter tail transistors, controlling PMOS, and the extrinsic noise injected into the tuning node. Therefore, the SSB phase noise of N stage VCO can be calculated as

$$\mathcal{L}\{\Delta f, K_{\text{VCO}}\} = \frac{1}{4\Delta f^2} \left(\frac{f_{\text{osc}}}{2 \cdot N \cdot I_{\text{out}}} \right)^2 \cdot N \left[\left(\overline{i_{n_{N_k}}^2} + \overline{i_{n_{P_k}}^2} \right) + \overline{i_{n_{P1}}^2} + \overline{i_{n_{\text{ext}}}^2} \right] \quad (3.13)$$

The MOSFET flicker noise PSD in the active region is $\overline{v_n^2} = \frac{K_f}{WLC_{ox}\Delta f}$, where $K_f \approx 10^{-25}(\text{V}^2\text{F})$ is a process dependent constant and K_{fP} is usually lower than K_{fN} . By substituting the equivalent current noise $\overline{i_n^2} = g_m^2 \overline{v_n^2}$ in equation (3.13), the SSB phase noise caused by flicker noise can be described as

$$\mathcal{L}\{\Delta f, K_{\text{VCO}}\} = \frac{1}{16 \cdot N \cdot I_{\text{out}}^2} \cdot \frac{f_{\text{osc}}^2}{(\Delta f)^2} \cdot \left[\frac{2I_{\text{out}}}{\Delta f} \cdot \left(\frac{\mu_n K_{fN}}{L_{N4}^2} + \frac{\mu_p K_{fP}}{L_{P4}^2} + \frac{\mu_p K_{fP}}{L_{P1}^2} \right) + \kappa_m \cdot g_{m_{P1}}^2 \overline{v_{n_{\text{ext}}}^2} \right]. \quad (3.14)$$

Consequently, equation (3.14) combined with (3.10) approximate the total phase noise characteristics of the proposed VCO. Usually phase noise is expressed in decibels (dB) as $10 \cdot \log(\mathcal{L}\{\Delta f\})$, and its units are dB below the carrier in a 1 Hz bandwidth, generally abbreviated as dBc/Hz [96].

As specified in the analytical model equations (3.10) and (3.14), the white and flicker phase noise are inversely proportional to the drain current of MOSFETs in the inverter stack. This is because the delay is directly affected by the noise associated with the transistors connected to the output nodes [51]. Therefore, as the current noise associated with the current mirror transistors is reflected to the inverter with a κ_m of less than one, the noise originating from those MOSs is not included in the model to simplify the analysis. At the low offset frequency, the flicker noise of transistors used to implement the delay element is the dominant close-in phase noise source. Generally, transistors operating in a periodically stable region have more contribution to the circuit phase noise than transistors functioning in a switching mode. Thus, transistors composing the current source (M_{P1}), and inverter (M_{P4} - M_{N4}) which run in a period stable state, generate more $1/f$ noise. This impact was reduced by adopting PMOS transistors for input controlling source since holes are less likely to be trapped and leads to inherent lower flicker noise than NMOS transistors. Also, the transistors' sizes are

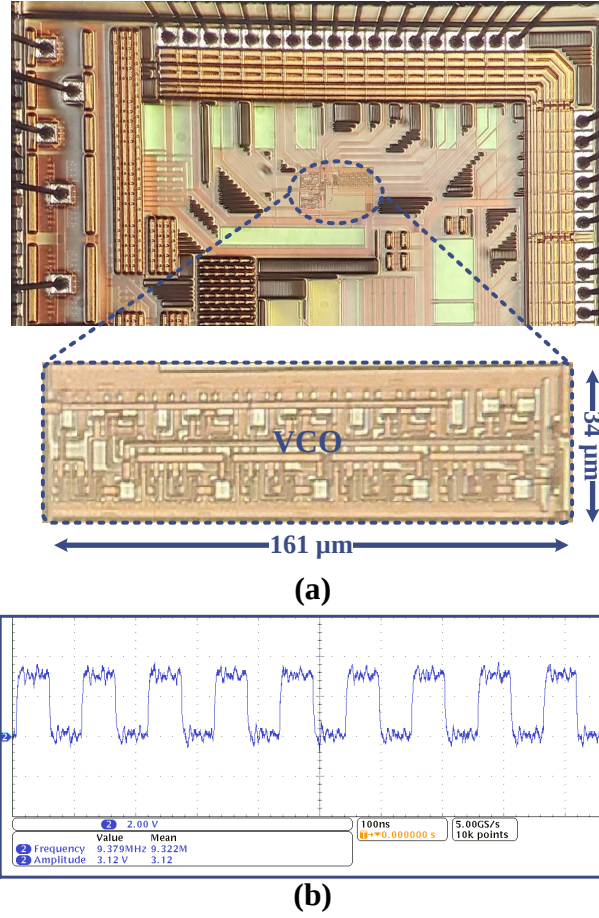


Figure 3.6 (a) Chip micrograph of the proposed VCO. (b) Measured output waveform of the VCO for a control voltage of 0 V and the maximum operation frequency

selected large enough with respect to the I_{out} and f_{osc} to alleviate this noise. On the other hand, as the output voltage swing is maximized in the proposed VCO, transistors connected to the output node (M_{P4} - M_{N4}) are periodically turned off. So, less thermal noise is injected into the channels of the inverter transistors during output transitions. Consequently, the noise power is decreased compared to the carrier power, resulting in improved phase noise performance [53]. Furthermore, by incorporating the replicating current mirror into each cell, the long metal lines, in physical implementation, that act as antennas for the transient noise of the oscillator can be avoided. In addition, the mismatch between delay cells was reduced by allowing a proper physical layout design and adopting layout matching techniques. This further improves the jitter and phase noise performance of the implemented VCO. Meanwhile, by forming a guard ring layer around the VCO design, the output signals have been protected from coupling to the underlying substrate noises. The power supply noise is also reduced due to the use of on-chip linear bypass capacitors within the free chip area.

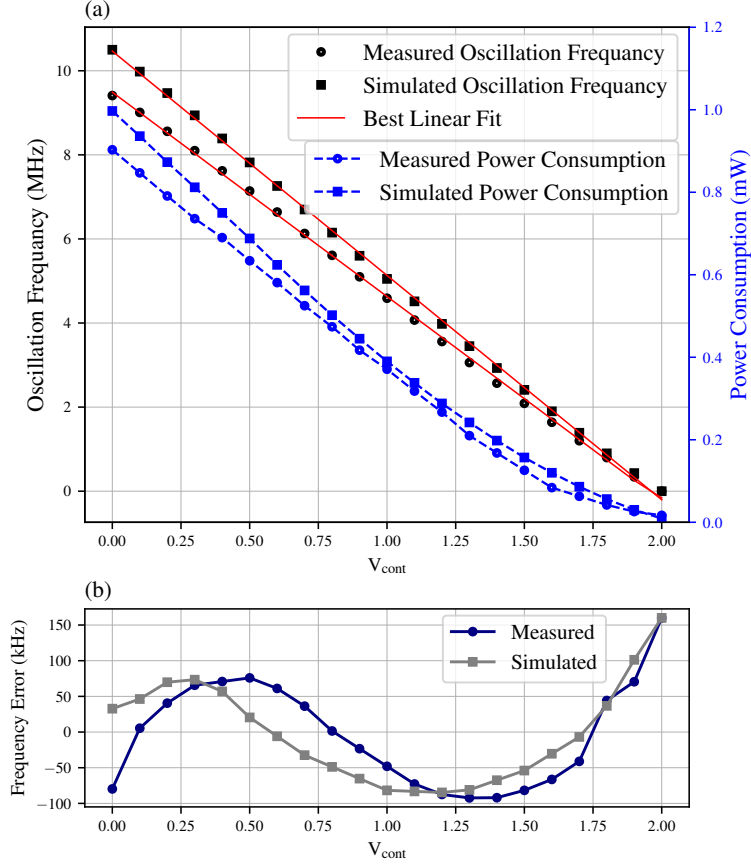


Figure 3.7 (a) Simulated and measured oscillation frequency and power consumption of the proposed VCO versus its control voltage, and (b) The nonlinearity error of the VCO frequency

3.5 Measurement Results

The proposed ring-VCO is designed and fabricated using a $0.35\ \mu\text{m}$ standard CMOS technology with a supply voltage of 3.3 V. The chip micrograph of the proposed linear ring VCO prototype, which is a part of a monitoring and readout circuit in a projected industrial sensor interface, is shown in Fig. 3.6(a). The VCO occupies an area of $0.005\ \text{mm}^2$ with a form factor of $34\ \mu\text{m} \times 161\ \mu\text{m}$. The chip is wire-bonded inside a pin grid array (PGA) package for measurements. The package is soldered to a custom printed-circuit board (PCB) for the test. Decoupling capacitors with values of $0.1\ \mu\text{F}$ and $10\ \mu\text{F}$ are utilized to filter the power lines. Fig. 3.6(b) illustrates the oscilloscope transient waveform of the proposed VCO's output signal at a control voltage of 0 V and the maximum oscillation frequency.

The simulated and measured oscillation frequency and its corresponding core power consumption of the integrated VCO as a function of its tuning voltage are depicted in Fig. 3.7(a). The

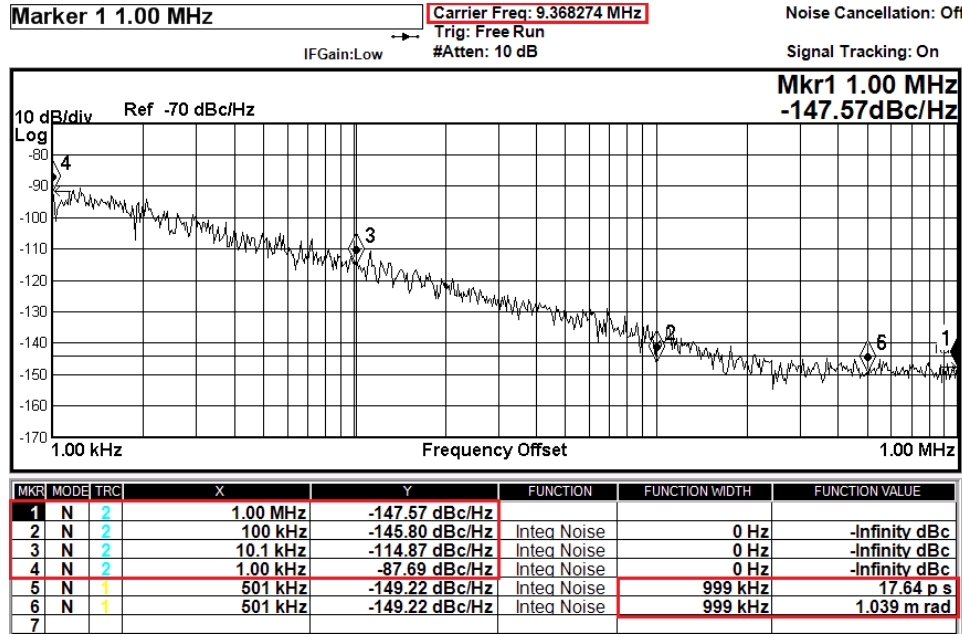


Figure 3.8 Measured phase noise performance of the VCO

proposed VCO visually exhibits improved linear performance. The simulated and measured nonlinearity error over the tuning range is presented in Fig. 3.7(b), yielding a maximum error of 0.8% and 0.9%, respectively. As can be seen in the figure, nonlinearity might be increased for $V_{\text{cont}} \geq 2$ V.

The VCO was designed to generate an output frequency between 0.01 MHz and 10 MHz for a control voltage varying from 0 to 2 V. However, the measured output is from 0.01 up to 9.37 MHz resulting in a tuning range, TR_f , of 199.5%. This slight reduction in the maximum measured frequency is due to process variations and the parasitic capacitances from PCB traces and the coaxial cable in the signal path.

Fig. 3.8 shows the measured VCO phase noise behavior, where it exhibits -87.69, -114.87, -145.80, and -147.57 dBc/Hz at 1 kHz, 10 kHz, 100 kHz, and 1 MHz offset from 9.37 MHz carrier, respectively. Furthermore, it shows the measured RMS jitter at 1 MHz bandwidth of integration equal to 17.64 ps (or 1.039 mrad). Since SSB phase noise follows a slope of -30 dB/dec up to 100 kHz offset frequency, we can conclude that flicker noise is the main contributor to the proposed VCO's phase noise, as was expected based on its operating frequency range. In addition, the measured spectrum of the presented VCO circuit, when tuned to generate a maximum frequency of 9.37 MHz (with $V_{\text{cont}} = 0$ V), is shown in Fig. 3.9(a). Fig. 3.9(b) illustrates the output signal power of the proposed VCO corresponding to the operating frequencies over a control voltage varying from 0 to 2 V. The results include the loss associated with the cable and interfaces.

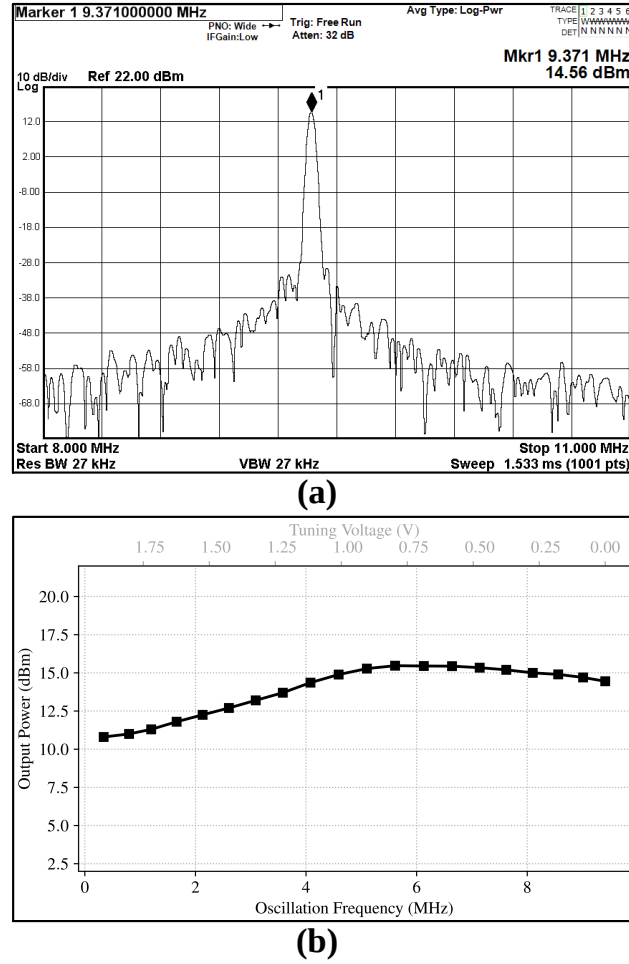


Figure 3.9 (a) Measured spectrum of the VCO at a control voltage of 0 V. (b) Measured output signal power versus oscillation frequency

Fig. 3.10 shows the measured phase noise of the proposed VCO versus frequency offset for different oscillation frequencies. Also, the phase noise result at maximum f_{osc} obtained by the developed analytical model of (3.10) and (3.14), is plotted in Fig. 3.10 as dashed line with corresponding measured phase noise color. The used circuit parameters are shown in the inset. The carrier frequency in the analytical equations is optimized with respect to the measured value of the maximum oscillation frequency of 9.37 MHz. Since the control voltage is provided from a DC generator during measurement, the measured PSD of $v_{n_{ext}} = 5 \text{ nV}/\sqrt{\text{Hz}}$ is used for the extrinsic noise accompanying the bias voltage. As the tuning voltage increases, the output current and the oscillation frequency decrease. As shown in analytical equations (3.10) and (3.14), oscillation frequency and output current have opposing effects on the phase noise. Thus, control voltage increments have only resulted in a few dB improvements.

Comparison of the analytical model prediction with the measured phase noise shows that

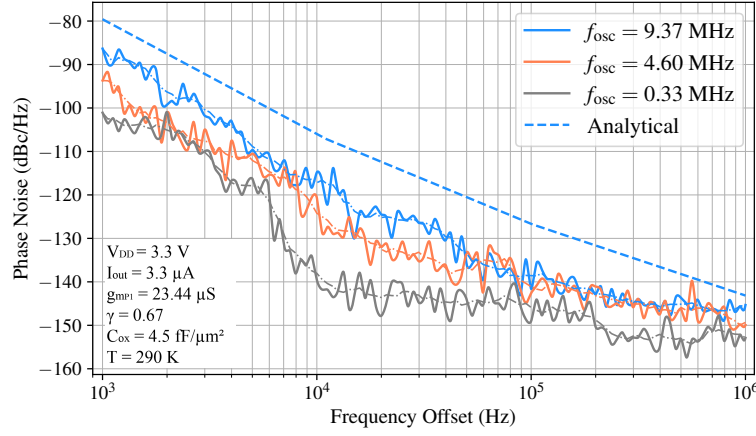


Figure 3.10 Measured phase noise of the proposed VCO at different oscillation frequencies compared to the noise analytical model @ $f_{\text{osc}} = 9.37$ MHz

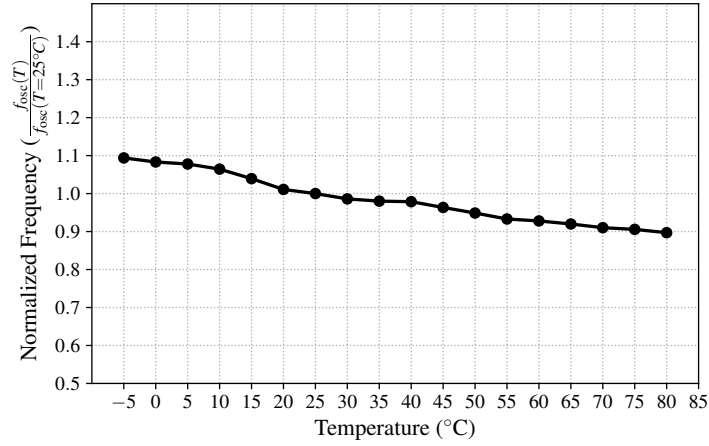


Figure 3.11 Measured temperature sensitivity at maximum oscillation frequency (frequency is normalized to $f_{\text{osc}} = 9.37$ MHz at room temperature)

the average phase noise difference is less than 8% as the frequency offset changes from 1 kHz to 1 MHz. This slight difference stems from some correlated noise sources on different nodes of the oscillator. For instance, substrate and supply noise arising from current switching in other parts of the chip are considered negligible in the analytical model. Also, the induced phase noise of the output buffer, which is not considered in the analytical model, influences the total phase noise result. Because of this, the measured phase noise for the offset of more than 10 kHz does not follow the same slope as the estimated phase noise from the analytical equations. A temperature evaluation is performed in the temperature range of -5 °C to 80 °C. Fig. 3.11 illustrates the measured drift in the normalized frequency at the nominal value of 9.37 MHz (measured at room temperature) due to temperature variation. It shows that the average temperature sensitivity is less than $\pm 10\%$.

Table 3.2 Performance summary and comparison of the proposed VCO with prior-art publication

Reference	Tech. (nm)	Supply (V)	Oscillation Freq. (MHz)	Pdis (mW)		Phase Noise (dBc/Hz)		Frequency TR _f (%)	Area (mm ²)	FoM ₁ (dBc/Hz)		FoM ₂ ^a (dBc/Hz)
				Avg.	Max.	$\Delta f=10\text{kHz}$	$\Delta f=1\text{MHz}$			$\Delta f=10\text{kHz}$	$\Delta f=1\text{MHz}$	
This Work	350	3.3	0.01-9.37	0.32 ^b	0.903 ^b	-114.87	-147.57	199.5	0.005	-174.75	-167.5	-193.45
TVLSI'15 [56]	180	1.2	12.6-48	1.2	1.8	-50 ^d	-109.38	116.83	0.0216	-121.05	-140.41	-161.77
JSSC'06 [86]	250	2.4	7	N.A	1.5	N.A	N.A	N.A	0.12 ^c	N.A	N.A	N.A
TCASI'18 [57]	130	1.2	2-20	0.227	N.A	-51 ^d	-88.59	163.6	0.01 ^c	-120.2	-117.74	-142
JSSC'13 [2]	130	1	5.822-8	N.A	0.031	-72.46	-112.46	27.33	0.025 ^c	-142.8	-142.84	-151.58
ISSCC'16 [90]	180	1.4	10.5	N.A	0.22	-94.3	-135.07	N.A	0.025	-161.3	-162.07	N.A
JSSC'17 [21]	40	0.8	1.05	0.017	N.A	-84 ^d	N.A	N.A	0.003 ^c	-142.1	N.A	N.A
JSSC'20 [17]	180	1.8	0.7-9.5	N.A	0.01	-87	-127	172.54	0.0237	-156	-154	-178.7
TVLSI'19 [98]	180	1.2	13.4	N.A	0.158	-68.69	-124.07	N.A	0.117	-139.24	-154.6	N.A

^a At 1 MHz offset frequency, ^b Considering the output buffer consumption, ^c Estimated from die micrograph, ^dEstimated from measured phase noise plot, ^eAt 0.6 MHz offset frequency

3.6 Discussion

3.6.1 Comparison to the State of the Art

Table 3.2 summarizes the measured performance of the proposed ring-VCO compared with prior VCO designs implemented in various CMOS processes, from 40- to 250-nm technologies, while operating at a low-frequency similar to the one of the proposed VCO. Using almost the same carrier frequency, the proposed design shows a better phase noise performance, an extended frequency range, and a smaller silicon area. The energy-efficient designs given in [2], [21] and [17] suffer from poor phase noise, even though they operate at low frequencies of 5.822 MHz, 1.05 MHz and 2.24 MHz, respectively.

In favor of a fair comparison with other relevant works at different oscillation frequencies and power dissipation, the following well-known Figure-of-Merit (FoM) is utilized [51]:

$$\text{FoM}_1 = \mathcal{L}\{\Delta f\} - 20 \log \left(\frac{f_{\text{osc}}}{\Delta f} \right) + 10 \cdot \log \left(\frac{P_{\text{dis}}}{1 \text{ mW}} \right) \quad (3.15)$$

where $\mathcal{L}\{\Delta f\}$ is the phase noise at the offset frequency of Δf , f_{osc} is the oscillation frequency and P_{dis} is the VCO's consumed power. In addition, another FoM (FoM₂) with respect to the total frequency tuning range (TR_f) is defined as [91]:

$$\text{FoM}_2 = \mathcal{L}\{\Delta f\} - 20 \log \left(\frac{f_{\text{osc}} \cdot TR_f}{10 \cdot \Delta f} \right) + 10 \cdot \log \left(\frac{P_{\text{dis}}}{1 \text{ mW}} \right) \quad (3.16)$$

with

$$TR_f = \frac{f_{\text{max}} - f_{\text{min}}}{f_{\text{central}}} (\%). \quad (3.17)$$

From the FoM_1 perspective, the performance of all VCOs in terms of power consumption and phase noise with respect to two different carrier frequencies are examined. The FoM_1 of the proposed VCO is -174.75 and -167.5 dBc/Hz at 10 kHz and 1 MHz frequency offset, respectively. As shown in Table 3.2, the presented work shows a better FoM_1 amidst the designs with roughly the same operating frequency. Structures reported in [90], [17] and [98] have good FoM_1 or FoM_2 , but exhibit high phase noise, large area, and limited tuning frequency range.

The proposed VCO achieves low power and a small integration area compared with similar designs listed in Table 3.2. The average power consumption is 0.32 mW, and the power dissipation at a maximum oscillation frequency of 9.37 MHz is 0.903 mW including the power of the output buffer. Despite the high supply voltage and the long-channel technology whose power consumption is inferior, the proposed VCO shows a wide frequency range with a tuning voltage up to 2 V and a FoM_2 of -193.45 dBc/Hz. In addition, it shows a linear voltage tuning range over 60% of VDD while significantly outperforming conventional techniques in terms of phase noise property.

Additionally, the VCO contributed noise can be characterized by the input-referred phase noise spectrum as a function of the offset frequency. Phase noise can be accurately represented as input-referred noise by applying the inverse of the system transfer function [50, 89]. Since phase is the integral of the frequency, the VCO acts as an ideal integrator for the control voltage when the output variable is a phase. So, its transfer function can be simply expressed as $H_{\text{VCO}}(s) = \frac{K_{\text{VCO}}}{s}$. The one-sided PSD of input-referred phase noise as a function of the certain Δf , can be defined as [89, 96]

$$S_{\text{IRPN}}(\Delta f) = S_{\phi}(\Delta f) \cdot \frac{\Delta f^2}{K_{\text{VCO}}^2} = \mathcal{L}(\Delta f) \cdot \frac{2\Delta f^2}{K_{\text{VCO}}^2}, \quad (3.18)$$

where $S_{\phi}(\Delta f)$ is the one-sided PSD of phase noise. So, the input-referred noise of the proposed VCO with a phase noise of -147.57 dBc/Hz at 1 MHz offset and a gain of 4.7 MHz/V is calculated to be 12.58 nV/ $\sqrt{\text{Hz}}$. As explained, the proposed VCO is designed for a sensor interface application where a low-frequency range was adopted. However, by adjusting tran-

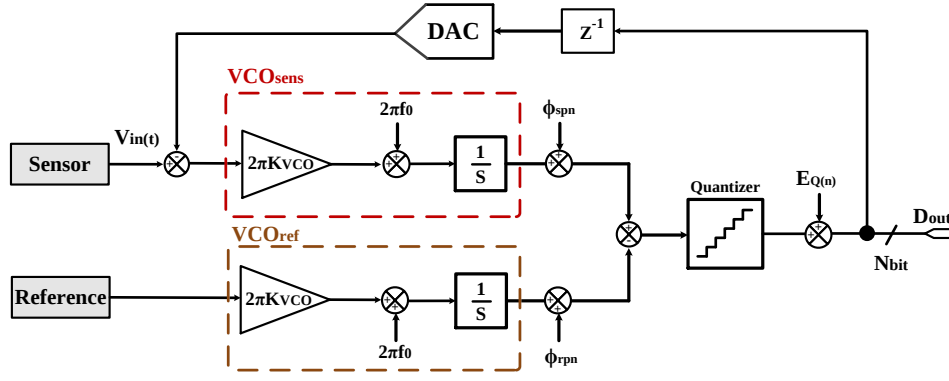


Figure 3.12 Simulation model of a PLL-based sensor interface incorporating the VCO's phase noise effect

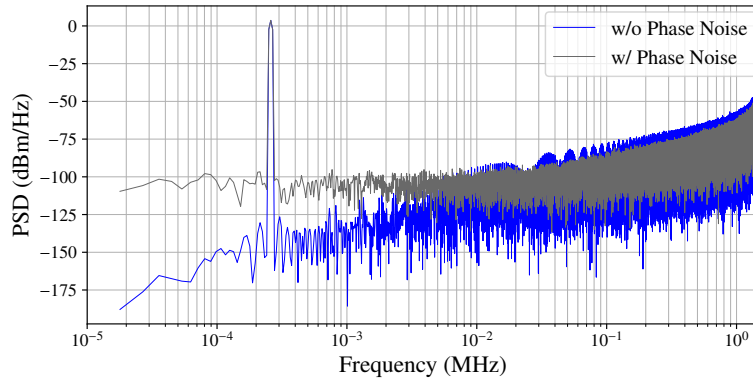


Figure 3.13 Simulated output spectrum with and without VCO phase noise (-147.57 dBc/Hz @1 MHz offset equivalent to 17 ps jitter, $K_{VCO} = 4.7$ MHz/V, $f_s = 9.37$ MHz (free-running frequency), $N_{bit} = 4$)

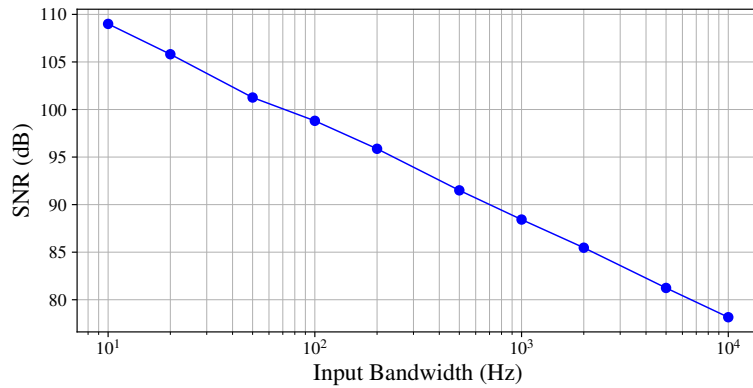


Figure 3.14 SNR versus input bandwidth for a measured VCO phase noise of -147.57 dBc/Hz @ 1MHz offset, gain $K_{VCO} = 4.7$ MHz/V, and quantization bit $N_{bit} = 4$

sistors' feature size in the proposed design, a higher oscillation frequency could be achieved. Generally, the maximum oscillator frequency as a function of the CMOS technology development has an ascending behavior while the phase noise performance is descending. Therefore, the proposed design at higher frequencies and scaled technology nodes may experience some degradation in its phase noise performance.

3.6.2 System-level Sensor Interface Architecture

To evaluate the efficiency of the proposed VCO as an embedded sub-block, a system-level time-based sensor interface is performed with MATLAB/SIMULINK. The measured VCO circuit parameters are adopted in this implementation and the overall performance is examined. Fig. 3.12 shows the corresponding simulation model of the closed-loop PLL-based sensor interface presented in Fig. 3.1(b) [23,50]. The conversion is based on the locking of two identical VCOs (VCOsens and VCOref). To model a practical VCO, its frequency is represented with a polynomial based on (3.5). The multi-bit PFD (phase frequency detector), which can be modeled as a time-domain quantizer, generates an N-bit code (Dout), which is the digitization of the sensor input signal ($V_{in}(t)$). The system's sampling rate is determined by the reference frequency. In the locking condition, the frequency of VCOsens is on average equal to the frequency of VCOref (or sampling frequency f_s).

Simulations are performed with the consideration of the oscillator phase noise at the output of the VCO (ϕ_{spn} and ϕ_{rpn}). The phase noise can be expressed in the time domain as a cycle-to-cycle jitter, σ_c^2 [95]. The jitter contributions can be transferred by $\sigma_c \cdot randn()$, where $randn()$ is a MATLAB[®] function used to generate normally distributed random numbers [50]. The measured jitter result of the proposed VCO (17 ps) is employed in simulation to provide a reasonable evaluation. The input signal with frequency of $f_{in} = 260$ Hz and peak-to-peak amplitude of 0.5 Vpp is applied. Fig. 3.13 shows the simulated power spectrum with and without the impact of phase noise for the PLL-based sensor interface. Fig. 3.14 illustrates the SNR of the interface circuit as a function of the input bandwidth (BW) while considering the proposed VCO measured characteristics. As can be seen, the SNR of 88.43 dB is achieved with low phase noise VCO at 1 kHz input bandwidth, $f_{osc} = 9.37$ MHz, and quantizer number of bits ($N_{bit} = 4$).

The impact of VCO's phase noise is usually applied to the system-level model by the matter of jitter. Since the analytical link between flicker-induced phase noise and jitter needs a complicated approximation, most of the prior arts consider only the white noise ($1/f^2$) in phase noise to jitter conversion [95]. Thus, the phase noise nonideality is estimated from the $1/f^2$ phase noise using (3.9) [23, 50]. Although the result of this approximation is not

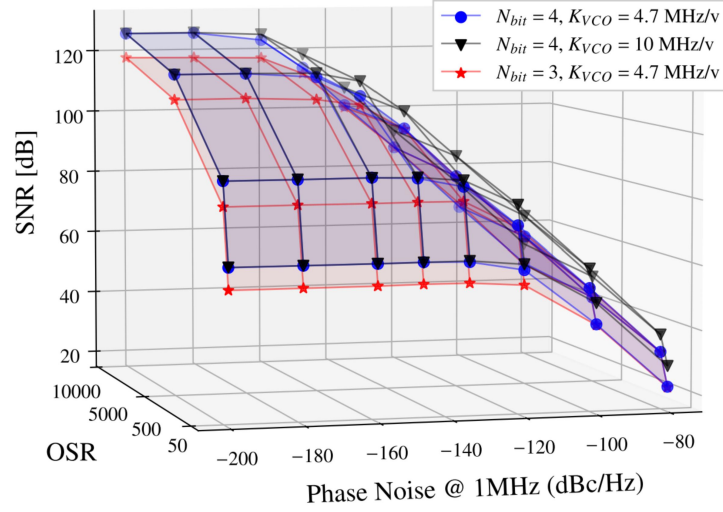


Figure 3.15 SNR as a function of VCO phase noise and OSR concerning different VCO gains and quantization bits

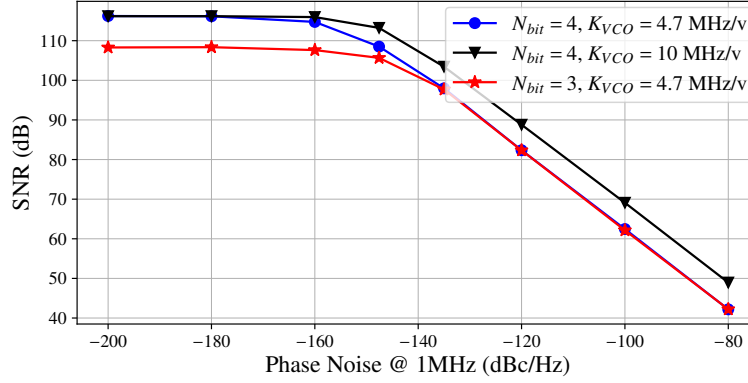


Figure 3.16 SNR as a function of VCO phase noise at OSR=5000

quite realistic, it is a tolerable approach to evaluate the influence of the VCO phase noise on the system's SNR. Fig. 3.15 shows the SNR as a function of the VCO phase noise and oversampling ratio ($OSR = f_s / 2BW$). It is visible that decreasing the VCO phase noise and increasing the OSR leads to SNR and hence resolution increment. However, OSR boosting is a more energy-efficient strategy at the cost of input bandwidth [50]. Fig. 3.16 shows the cross-section view of Fig. 3.15 at OSR=5000. It can be seen when the phase noise is insignificant (for the phase noise less than -160 dBc/Hz), the gain has no effect on the SNR performance while the SNR increases by 6.02 dB for each quantizer bit as expected from the ideal definition. On the contrary, in the phase noise dominant region (right-side), doubling the VCO gain improves SNR by around 4 to 8 dB depending on the phase noise value.

We can conclude that in a VCO-based sensor interface, the oscillator phase noise performance has a major impact on the overall system SNR. According to Fig. 3.14, the system can achieve over 14 effective number of bits (ENOB) of resolution for the practical VCO phase noise value of -147.57 dBc/Hz at a 1-MHz offset frequency (or 17.64 ps jitter), 4.7 MHz/V gain, 1 kHz bandwidth and an OSR of 4685. This substantiates the capability of the proposed VCO in the realization of a high-resolution sensor interface.

3.7 Conclusion

We presented in this paper the design and analysis of a linear, low-noise, and wide-tuning range ring VCO operating as part of a constituent block of an integrated readout sensor interface. The prototype was implemented in the AMS 0.35 μm CMOS technology under a 3.3 V supply. The measured oscillation frequency range extends from 0.01 to 9.37 MHz which represents a 199.5% frequency tuning range over a 2 V control voltage. At maximum frequency, the measured phase noise is -147.57 dBc/Hz at 1 MHz offset frequency, while the FoM of the proposed VCO is -167.5 dBc/Hz. The average power consumption is 0.32 mW while taking a silicon area of 34 μm $\times$ 161 μm . Also, we have discussed the performance analysis of a PLL-based sensor interface via a MATLAB/SIMULINK model and showed the impact of the VCO phase noise on the SNR performance of the targeted application. Simulated results indicate that a SNR of 88.43 dB can be obtained in a time-based readout interface utilizing the proposed VCO measured characteristics. Therefore, the proposed configuration allows realizing a compatible VCO structure for a wide range of analog/digital circuits requiring VCO, such as time to digital converters and sensor interfaces for numerous applications.

3.8 Acknowledgment

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CHAPTER 4 ARTICLE 2 : A LOW-OFFSET VCO-BASED TIME-DOMAIN COMPARATOR USING A PHASE FREQUENCY DETECTOR WITH REDUCED DEAD AND BLIND ZONES

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4.1 Abstract

We present in this paper a high-precision voltage-controlled oscillators (VCO)-based time-domain (TD) comparator. It involves two identical and linear VCOs to convert the input voltage difference of the comparator into the time/frequency difference. Also, it includes a novel low-power phase frequency detector (PFD) to compare the output frequencies of the VCOs. The proposed PFD technique reduces the problematic effects of missing edges and phase ambiguity in conventional circuits by minimizing dead-zone (DZ)/blind-zone (BZ) and suppressing unwanted output glitches. The TD-comparator prototype is fabricated in a 350-nm CMOS process having an active area of 0.01 mm². The comparator consumes 93.65 μ W power from a 3.3-V supply and provides a conversion rate of 2.7 MHz with 148 μ V_{rms} input-referred noise. Measurement results of 5 fabricated chips show an input-referred offset standard deviation of 81.14 μ V. Stand-alone characteristics measurements of the proposed PFD show a minimized DZ and BZ of less than 12 and 22.7 ps, respectively. With an almost $\pm 2\pi$ input phase range, the maximum operating frequency of the PFD is 1.32 GHz.

4.2 Introduction

Comparators are critical components in a wide variety of applications, such as voltage regulation, data conversion, and environmental and manufacturing process monitoring. As CMOS technology scaled down, lower voltage headroom, weaker intrinsic transistor properties, and inferior matching between transistors reduce the efficiency and portability of analog circuit designs [99]. Therefore, conventional dynamic voltage-based comparators show poor perfor-

mance in advanced technologies while they suffer from significant power consumption, large area, high offset, and noise [73].

On the other hand, finer power reduction, area scaling, and stability of time-based circuit techniques with highly digital implementation make them viable solutions that exploit the benefits of scaled CMOS processes [6, 17]. Thus, energy-limited designs like sensor networks or analog-to-digital converters (ADCs), which are integral parts of data acquisition systems, biomedical and internet of things (IoT) applications, are directed to the time-domain (TD) comparators to fulfill their desired specifications [19, 72]. These advanced comparators represent and process signals in time (or frequency) instead of the voltage domain.

In a time-based comparator, both input and reference voltages are converted to frequency signals (square waves) and compared with their duration. Most reported TD-comparators provide relative efficiency and operate at low supply voltages or within the sub-threshold region [97]. Employing low-performance circuits for voltage-to-time (V2T) conversion and diversion detection blocks result in low speed and poor jitter behavior in prior works [71]. The V2T conversions are generally implemented by voltage-controlled delay lines (VCDLs) [66, 67], voltage-controlled oscillators (VCOs), etc [19, 20, 68, 69]. Also, the comparator requires at least a phase detector (PD) to detect the phase transition error, while it can be improved by using a phase-frequency detector (PFD).

A PFD is a circuit that compares two input digital signals, particularly pulse signals with an associated oscillation frequency, to determine which one has a zero-crossing earlier or more often. A conventional PFD is an asynchronous design with six reset mechanisms adopted to reinitialize the circuit, each of which reduces the operating speed [62]. Therefore, several techniques have been implemented to improve phase/frequency detection performance [27, 28, 64]. However, the presence of a dead-zone (DZ) and a blind-zone (BZ), which are a time slot of missed phase error detection close to 0° , and 360° respectively, is another predominant demerit of prior-art PFDs [24–26].

Most employed PFDs in the TD-comparators are based on latches, flip-flops, or counters that suffer from inevitable non-zero setup time and DZ [71, 100]. Due to closed loop operation, the output jitter caused by PFD's DZ may be added to random input-referred offset (IRO) of the comparator [29]. Likewise, using counters to compare the frequency information of the input signals results in a quite long comparison time (in the range of milliseconds). So, to increase the comparison accuracy, an increment in the number of counter bits is required. Therefore, the traditional phase/frequency comparison approach is inadequate for high-speed applications. Furthermore, conventional PFDs often produce glitches or undesired one-shot pulses at their output. This may cause a short circuit between the supply and ground, that

results in considerable static power consumption, dynamic jitter, phase offset, and wrong comparator output.

In an attempt to mitigate the DZ effect in the TD-comparator, the authors in [66] increased the number of delay stages in VCDLs or load capacitance to multiply the voltage-to-time sensitivity. However, if the input voltage is too small, the time difference of pulses at the output of VCDLs is inadequate and within the DZ. So, the VCDL has to oscillate until the phase difference reaches a level that exceeds the DZ. It means considerable power has to be consumed since the number of oscillations and decision time depend on the input voltage level. A bypassing function has been adapted in [19] to overcome the metastability problem induced by non-zero DZ PD. This scheme needs an oscillation cycle counter to find the number of oscillation cycles (NOCs) and a window-size detection scheme to indicate the size of a bypass window. Therefore, better accuracy may be obtained at a lower speed and larger silicon area. In [68], a time amplifier is utilized at the end of the differential VCO to amplify the time difference among the VCO outputs and overcome the employed PFD DZ. However, this results in additional circuit implementation, area, noise sources and power consumption.

In this work, we present a fully integrated low offset, low noise, high resolution, high speed, and small area VCO-based TD-comparator. The proposed design aims to overcome the prior art's limitations by providing an improved low-noise PFD, with minimized DZ or BZ, free of glitches and undesired one-shot pulses. The presented TD-comparator employs a low phase noise ring VCO. This latter features a linear tuning characteristic yielding a constant gain over a wide range of operating frequencies. Due to this gain stability, the proposed VCO-based comparator can operate over a wide range of input common-mode voltages. Advantageously, a feedback control block interpolates a controlling signal to VCOs and enables or disables the operation of voltage-to-time conversion. This controlling unit prevents further power dissipation when the comparison ends. The low-power proposed PFD can also be considered as a stand-alone design compatible with all technically possible electronic circuit combinations. This paper is organized as follows: Section 4.3 describes the architecture and operation principle of the proposed TD-comparator, where the circuit configurations of the VCO and the PFD as a design sub-blocks are also studied. The detailed analysis and simulation results of the proposed comparator are provided in Section 4.4. Section 4.5 presents the experiential validation of the chip prototype, and Section 4.6 concludes the paper.

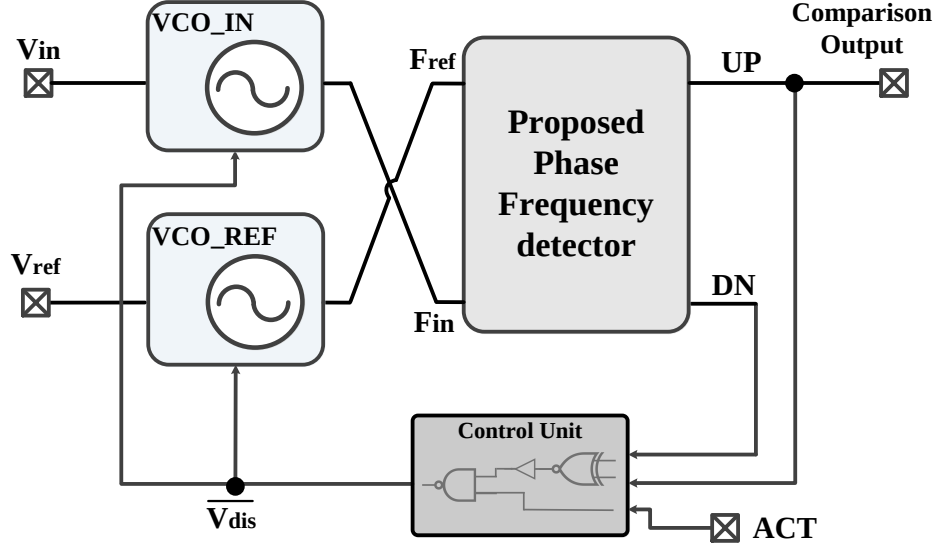


Figure 4.1 Block diagram of the proposed VCO-based TD-comparator

4.3 Circuit Description

4.3.1 Architecture of the Proposed TD-comparator

Fig. 4.1 illustrates the configuration of the proposed TD-comparator consisting of two symmetric VCOs receiving the input and reference voltage signals, a PFD, and a control unit. When the active signal, **ACT**, is low, VCOs' outputs are reset to logic '0'. Once **ACT** is triggered to high, the circuit is configured to start the operation. **VCO_IN** and **VCO_REF** convert voltage signals of V_{in} and V_{ref} to the corresponding digital output with particular frequency information F_{in} and F_{ref} , respectively. Each time-domain pulse signal is characterized by a phase and an oscillation frequency depending on the value of the VCOs inputs voltage. Further, the PFD derives the output of VCOs and generates two outputs which are usually designated as "up" (**UP**) and "down" (**DN**) signals representative of the frequency and phase comparison. To clarify, in an ideal PFD, if the phase or the frequency of F_{ref} is leading (i.e., ahead of) F_{in} , the PFD will produce a pulse signal proportional to the inputs' phase difference on the first **UP** output terminal, and perform a zero signal at the **DN** output. Conversely, if the F_{ref} is lagging the F_{in} , the error pulse is produced on the **DN** terminal, and a zero output is formed on the **UP** terminal. A feedback control scheme, including logic circuits, is employed to generate a control signal $\overline{V_{dis}}$ to enable or disable the circuit operation. This prevents further oscillation of VCOs and power dissipation when one of the **UP** or **DN** transitions to high and terminates the comparison procedure.

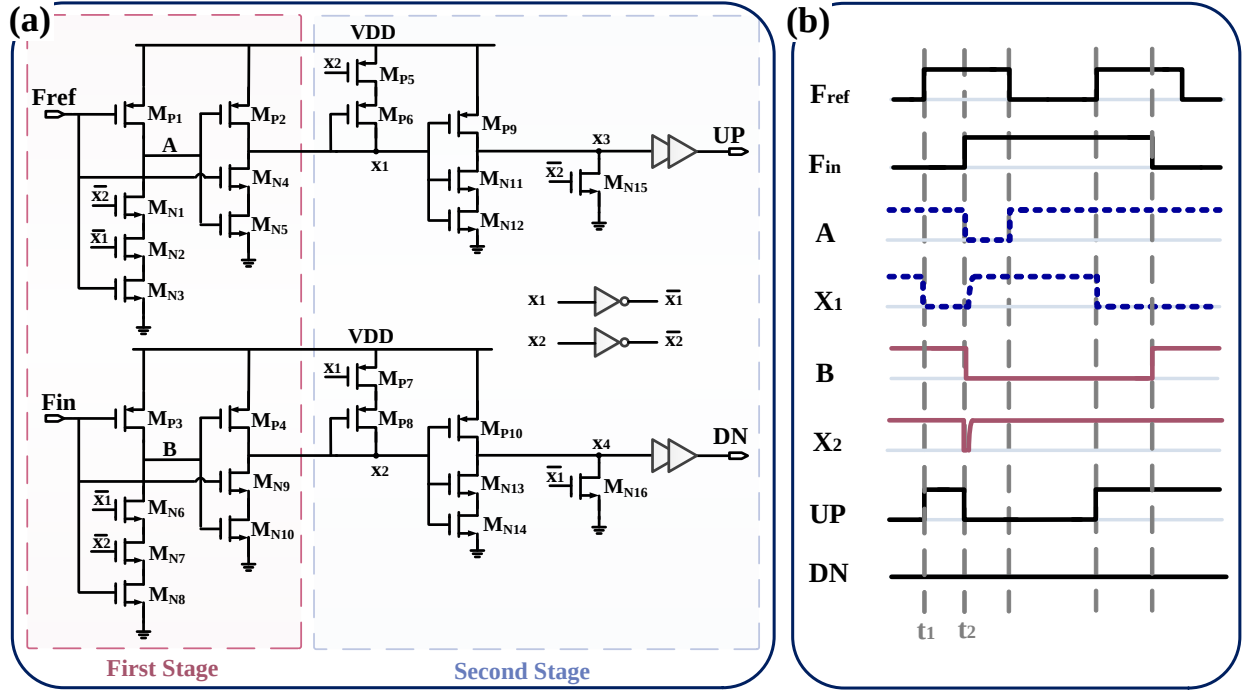


Figure 4.2 The proposed PFD: (a) Circuit diagram, and (b) timing diagram

4.3.2 Phase Frequency Detector

1) Background

PFDs have been widely used in many critical applications beside of TD-comparator circuits such as clock data recovery (CDR), phase-locked loops (PLLs), and delay-locked loops (DLLs) [24–26, 64]. Incorporating DZ and BZ in phase and frequency detection directly impacts the overall operation of any related application. DZ implies that the PFD finds out zero phase error between the two inputs when an infinitesimal phase difference ($\Delta\phi$) is present. In case where $\Delta\phi$ is nearly equal to 2π , the rising edge of the leading signal may coincide with the reset process, rendering it unrecognizable. So, in the reset region, the PFD perceives the subsequent lagged signal as the leading one, resulting in an incorrect output at the contrary terminal. The PFD is blind in that region and unable to respond properly to any transitions in input signals [27]. This reduces the range of phase characteristics of the PFD to $\pm 2\pi - \Delta_{BZ}$ (less than the ideal linear range of $\pm 2\pi$), where Δ_{BZ} is the width of the BZ region.

Consequently, these are the main factors affecting the PFD phase characteristics, as for example, DZ introduces phase noise into a PLL system, and BZ aggravates cycle slips, lengthens the frequency acquisition process and reduces the range of phase-locking [27]. In a TD-

comparator application, thermal and flicker noises can be presented as jitter at the VCO outputs and integrated over time. Because of these phase fluctuations, DZ in a PFD inhibits a fast decision. Consequently, the DZ is responsible for the noise and the comparator delay. BZ becomes more crucial for high-frequency operation, while both of which have a significant effect on resolution. Moreover, most PFD designs entail some unwanted small pulses at the outputs, such as glitches (at each state-switching time) and the one-shot pulse which occurs at start-up (when F_{in} and F_{ref} signals rise at the same phase). These intruding narrow pulses mean that the UP and DN signals are simultaneously at high potentials for a short interval, causing leakage currents and increasing reference spurs [28].

To overcome these limitations, several approaches were presented to suppress the DZ and BZ issues. Usually, some delay is added in the reset path to generate short pulses in order to minimize the impact of the PFDs' DZ [25,26]. However, the delay of the reset path contributes to the BZ and further reduces the effective phase comparison range [24,27]. Also, adding a large delay in the reset path increases the phase noise because of the inherently noisy current sources that are activated for a longer time. A PFD with improved BZ is presented in [24], where a delay cell is inserted into the input lines of the circuit. The additional delay shifts the leading pulse up to the end of the reset process, allowing the PFD to respond to the incoming edge. However, the added delay must be less than the reset time to guarantee the correct operation. Otherwise, the PFD cannot function properly since the output might be reactivated at the end of the reset. In this approach, the BZ becomes the difference of reset and additional delay time, which tended to zero if they were close. However, the BZ is composed of two main courses, the reset time and the input nodes pre-charge time [27]. If the reset time is greatly shortened, the required pre-charge time takes a considerable amount of the BZ. Besides, the delayed signal following a reset may not provide sufficient time for charging the internal nodes, resulting in an unwanted state shift at the output.

In the literature, several approaches have been presented to reduce or overcome glitches and phase mismatches in PFDs. For instance, removing the reset delay, including a nonlinearity function, or incorporating the opposing effect of the second input (F_{in}) besides F_{ref} in the UP output detection and vice versa [28,64]. These schemes, however, were not capable of following the ideal state of the PFD since if F_{in} is at high potential and the F_{ref} switches to logic '1', the UP state will remain unchanged. Moreover, most of these architectures are infeasible for $|\Delta\phi| > \pi$ and have complex and large area hardware. As a result, an effective PFD that suppresses the traditional drawbacks of this design is critical to developing electronic systems.

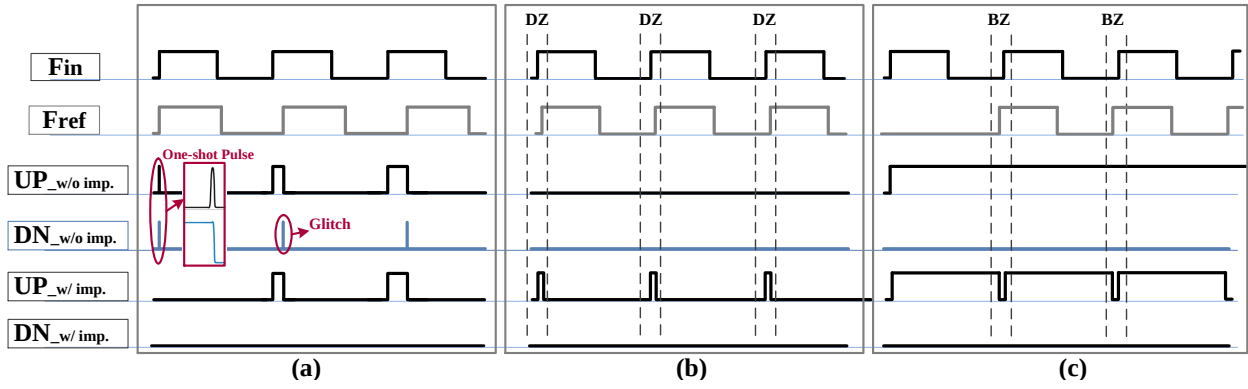


Figure 4.3 Transient response of the PFD with and without the proposed improvement in: (a) the glitch and one-shot pulse, (b) the DZ ($\Delta\phi \simeq 0$), and (c) the BZ ($\Delta\phi \simeq 2\pi$)

2) The proposed PFD

Fig. 4.2(a) shows the circuit diagram of the proposed PFD. It includes two processing stages where each comprises an upward and a downward circuit for receiving the frequency signals of F_{ref} , and F_{in} . The first stage is composed of two interconnected transistor branches from M_{P1} to M_{P4} , and M_{N1} to M_{N10} . This stage receives the digital inputs F_{ref} and F_{in} and produces the result signals x_1 and x_2 , which represent an intermediate state of the UP and DN signals, respectively. The operation of the first stage is reset through the transistors $M_{N1} - M_{N2}$ in the upward and $M_{N6} - M_{N7}$ in the downward circuit, once the two input frequency signals have a high potential and signals x_1 and x_2 are both at logic '0'. If $\overline{x_1}$ and $\overline{x_2}$ are '1' during the precharge of transistor M_{P1} (or M_{P3}), contention will take place because both PMOS and NMOSs will be ON. Therefore, an extra “foot” transistor M_{N3} (and M_{N8}) is added to the bottom of the reset stack to avoid contention and provide additional control on the reset. This footed gates scheme ensures that the reset signal should activate only when both inputs are at high potential.

The second stage of the proposed PFD is configured to detect and eliminate spurious pulses in the intermediate signals of x_1 and x_2 , in order to provide enhanced digital outputs at the main UP and DN terminals. The transistor branches $M_{P5} - M_{P6}$ and $M_{P7} - M_{P8}$ are used to reduce or prevent charge losses caused by leakage currents at nodes x_1 and x_2 , and keep them at high potential when both incoming inputs are logic '1'. The combination of transistors $M_{P9} - M_{N11} - M_{N12}$ and $M_{P10} - M_{N13} - M_{N14}$ provide improved inverters using a stacking technique, in which the width and height of the mentioned undesired pulses may be modulated at nodes x_3 and x_4 , respectively. According to the stacking principle, when more than one transistor is turned off in a stack of series-connected transistors, the subthreshold leakage current flow will be decreased. Therefore, employing two NMOS in the improved

inverter, in addition to one-shot pulse adjustment, reduce the leakage current and thereby the power dissipation of the circuit. Finally, the transistors M_{N15} and M_{N16} which are gate-controlled by the result signals $\bar{x}_1$ and $\bar{x}_2$, prevent glitches at PFD's outputs that occur at each switching state.

Fig. 4.2(b) shows the timing diagram of the proposed PFD. In this example, the reference signal F_{ref} has higher frequency and leads the input signal F_{in} . In the beginning, both outputs are at low potential, and node A and B are pre-charged to V_{DD} (logic '1'). At time t_1 , F_{ref} rises to logic '1' and turns transistors M_{N4} and M_{N5} on. So, x_1 falls to low potential and its corresponding output, UP, toggles to high. The state is held until the F_{in} signal rises to high at time t_2 . Thereupon, transistors M_{N9} and M_{N10} switch on, making result signal x_2 to fall to logic '0'. Since both result signals x_1 and x_2 are at low potential at the same time (means $\bar{x}_1$ and $\bar{x}_2$ to be at logic '1'), signals at nodes 'A' and 'B' will be reset to logic '0' through transistors $M_{N1} - M_{N2}$, and $M_{N6} - M_{N7}$, respectively. Further, transistors M_{P2} and M_{P4} will be activated, setting x_1 and x_2 to logic '1', which in turn drives the UP output to logic '0'. At the time t_2 , since $\bar{x}_2$ is at logic '1' for a small portion of time, a spike (glitch) might occur at node x_4 that could be propagated erroneously to the DN terminal. Together, the transistor M_{P10} and M_{N16} act as a voltage divider to reduce the amplitude of undesired pulse signal at node x_4 . Thereby, the tiny spikes will be suppressed by the following buffer. The aforementioned explanation is also applicable for the contrary instance when F_{ref} has a higher frequency or leading phase than F_{in} , and the detection result will appear at the DN output. Fig. 4.3(a) illustrates the transient behavior of the proposed PFD in relation to the unwanted spikes. The one-shot pulse at the start of the operation and glitches, that may occur in the response of a conventional PFD, are eliminated by the proposed configuration.

4.3.3 Dead-zone and Blind-zone

1) DZ and BZ in the proposed PFD

To shed light on the DZ and BZ mitigation in the proposed design, consider $F_{ref} > F_{in}$ and the upper branch circuit shown in Fig. 4.2(a). As shown in Fig. 4.3(b), in the case of a very slight Δf , there will be an extremely small phase difference between the two input signals of the PFD. Upon switching F_{ref} to logic '1' and node x_1 to logic '0', the UP output signal will rise to the high level only if $x_1 = '0'$ and $x_2 = '1'$ at the same time. Since the input F_{in} rises slightly after the rising edge of F_{ref} , x_2 will also become '0' shortly thereafter. Due to the short interval between falling time of x_1 and x_2 to logic '0', the UP node would not have sufficient time to be charged to logic high. Consequently, the upward circuit will fail to respond and detect the rising edge of its corresponding input, F_{ref} . Therefore, the presence or absence of

a DZ depends on the transition speed of the upward sub-circuit, and how quickly the output on terminal UP can switch to logic '1' when F_{ref} goes from low to high. The response speed of the upper sub-circuit is a function of the characteristics of the transistors M_{P1} , M_{N4} , and M_{N5} . By using the proper sizing and minimum length, the parasitic capacitance of these transistors can be reduced in order to increase the switching speed. Besides, employing a single PMOS M_{P9} , in the improved inverter, realises a fast rising edge at node x_3 and a rapid transition of the UP output to logic '1' to reduce or eliminate the DZ.

On the other hand, when operating at high frequencies (e.g., in the order of GHz), the $\Delta\phi$ between the input signals is insignificant, and the detection could be more difficult. Therefore, the proposed PFD is configured such that switching the output to logic '1' occurs faster than resetting the output to logic '0'. Thus, enough time interval will be provided for the circuit to detect and produce the narrow pulse response at the output. This functionality of the PFD can be obtained via the use of the inverted result signals $\bar{x}_1$ and $\bar{x}_2$, which are slightly delayed, to control the outputs falling on terminals UP and DN. In addition, the presence of two series NMOS in the improved inverter results in a slower falling edge delay compared to the rising edge delay at node x_3 (and x_4).

Likewise, when F_{in} is lagged to F_{ref} by a phase difference of nearly 2π , the upward circuit has a limited time to be reset and be ready for the next rising edge of F_{ref} (see Fig. 4.3(c)). Therefore, the BZ is correlated to the reset time and pre-charge time of internal circuit elements for dropping the UP output to the ground when F_{in} turns to logic '1'. Utilizing the transistor M_{N15} allows a quick state changing on UP to logic '0' to suppress the BZs. Furthermore, the foot transistor M_{N3} (and M_{N8}) in the reset stack help the BZ, because they minimize the reset time, especially when the phase difference is about 2π . Moreover, employing transistors M_{P5} in the up circuit and M_{P7} in the down one, which are gated through complementary intermediate results of x_2 and x_1 , substantially accelerates the reset process. As a result, the circuit is prepared to respond to the next rising state of the input, enabling the PFD to operate at high frequencies.

2) DZ and BZ in the TD-comparator

The operation principle of the proposed TD-comparator of Fig. 4.1, with and without employing a minimized-DZ PFD, is illustrated in the timing diagram shown in Fig. 4.4. LSB in this example represents the minimum detectable voltage difference or the comparator sensitivity. When $\overline{V_{\text{dis}}}$ is '0', the two ring-VCOs are enabled and begin oscillation. With the employed VCO configuration, when V_{in} is higher than V_{ref} , the frequency signal F_{in} is of a lower frequency than F_{ref} . If ΔV_{in} is large enough, e.g. more than 5 LSB, F_{ref} rises faster than

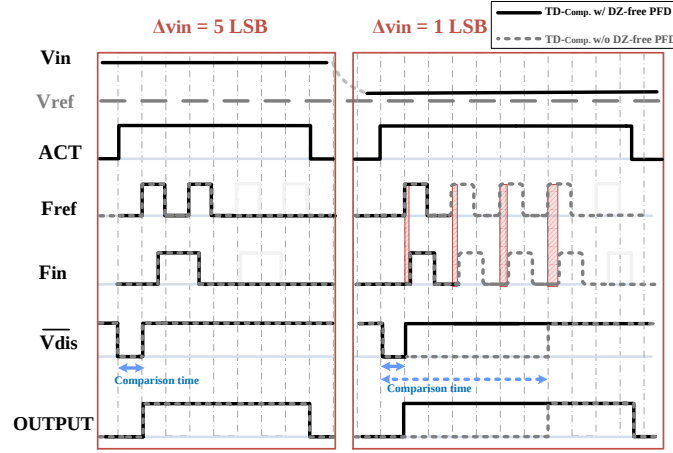


Figure 4.4 Operation of the proposed TD-comparator with and without DZ-free PFD when $\Delta V_{in} = 5$ and 1 LSB

F_{in} and the PFD yields the comparison results. Once the comparison output is acquired, $\overline{V_{dis}}$ converts to “disable” and prevents further oscillation of VCOs. When ΔV_{in} is too small (1 LSB or less), the VCOs’ output frequencies are very close and show a small time difference. In such conditions, the comparator with non-zero DZ PFD cannot make a correct decision since the slight period difference between signals is within the DZ. Therefore, VCOs remain activated and transmit pulses through the PFD until the difference in pulse times surpasses the DZ. As a result, the length of time for which the VCOs are enabled and the drawing power is significantly lower when the TD-comparator employs the proposed minimized-DZ PFD.

On the other hand, if ΔV_{in} is chosen so that the input signals of the PFD encounter a $\Delta\phi$ close to 2π , the BZ effect will be dominant. Alternatively, when applied to a high-frequency application, any ΔV_{in} may cause a phase shift of 2π due to the relatively short signal period. In these instances, the comparator may experience the condition mentioned above and need to expend additional time getting out of the BZ and responding to input signals. In a more severe case, the non-optimized BZ PFD may erroneously provide signal responses in the opposite output, and result in an incorrect comparator decision.

4.3.4 Voltage-controlled Oscillator

The circuit configuration of the proposed ring VCO is presented in Fig. 4.5. It is adapted for this comparator application from the delay cell architecture presented in [101]. It comprises from five delay stages with an output buffer for sharpening the produced waveform and driving the VCO load. In each current-starved delay cell, the control voltage (V_{cont}) is

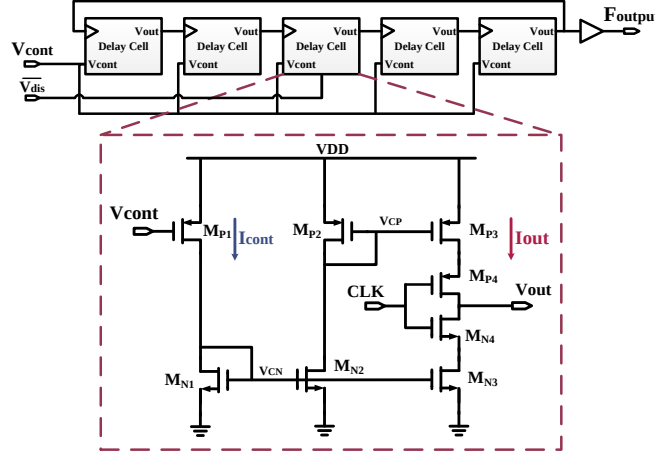


Figure 4.5 Circuit diagram of the proposed ring VCO

coupled to the gate of the voltage-controlled current source M_{P1} and the resulting current, I_{cont} , is mirrored to the inverter (composed of M_{P4} and M_{N4}) via the current mirror M_{N1} , M_{N2} , and M_{P2} . In the proposed VCO, the third delay cell has an additional input port connected to the node V_{CP} . This port receives the control signal $\overline{V_{dis}}$ to enable or disable the oscillation of the VCO as described in section II-A.

The controlling bias configuration is optimized so that the current source transistor, M_{P1} , and the current mirror transistors operate in the saturation region throughout the control voltage range and the load transistors in the inverter stage make a narrow voltage headroom. Thus, a maximized output amplitude and an opposite curvature of $f_{osc} - I_{cont}$ and $I_{cont} - V_{cont}$ characteristics will be achieved in order to rectify the nonlinear $f - V$ characteristic. By replicating the current source in each cell of the proposed VCO, the current-starved inverter can be biased dynamically, and linearity errors caused by fluctuations in I_{cont} can be reduced. Accordingly, the replica current mirror clamps the voltage at nodes with high parasitic capacitance and ensures that the currents in each stage are identical, resulting in a full output swing.

Improved linearity and constant gain of the VCO have a significant effect on the performance stability of the TD-comparator in terms of offset, noise, and energy per conversion. This is due to the fact that, in the case of employing a nonlinear VCO, the resulted Δf between the outputs of the VCOs in response to a fixed input voltage difference will change with common mode voltages (or V_{ref}) variations. Different Δf (or $\Delta\phi$) leads to different operating conditions for the following sub-blocks, resulting in an inconsistent outcome. Moreover, an inadequate $\Delta\phi$ may result in the non-functionality of the PFD, thereby limiting the input dynamic range of the comparator. Therefore, the linear VCO design results in a constant

conversion gain and allows the proposed VCO-based comparator to operate in a wide range of input common-mode voltages. It is worth mentioning that the VCO tuning nonlinearity also severely limits the performance of other time-domain applications, such as signal-to-noise and distortion ratio (SNDR) in VCO-based ADCs and PLL-based sensor interfaces [6, 17].

The large output voltage swing causes the switching mode transistors connected to the output node to turn on and off periodically. Thus, channels of the inverter transistors are subjected to less thermal noise during output transitions. In this way, the noise power is reduced as compared to the carrier power, leading to better phase noise performance [53]. The contribution of the control-line noise in the proposed VCO has been reduced through using a PMOS transistor for sourcing the input tuning current. As holes are less likely to be trapped, its flicker noise will be inherently lower than that of an NMOS transistor. Additionally, the VCO's white and flicker phase noises are inversely proportional to the drain current of transistors in the inverter line since they directly affect the delay of the VCO stages. Therefore, the noise associated with the controlling node transistor will be greatly reduced as it will be reflected in the output line current by a mirroring factor of less than one. Double guard rings of n+ and p+ connected to stable V_{DD} and GND rails are placed around each VCO delay cell to isolate the circuit from substrate noise. This consideration, along with an appropriate physical layout design, and applying layout matching techniques, allows further enhancement in jitter and phase noise performance.

4.4 Analysis and Simulations

4.4.1 Conversion Gain

The output frequency of a single-ended ring VCO is determined by the number of stages (N) and propagation delay (t_p) of delay cells. Based on the average current passing through the output capacitance, the propagation delay time at the toggle point ($V_{DD}/2$) can be estimated as

$$f_{\text{osc}} = \frac{1}{\tau} \simeq \frac{I_{\text{out}}}{N \cdot V_{DD} \cdot C_{\text{tot}}}, \quad (4.1)$$

where C_{tot} is the total parasitic capacitance seen at the output of each delay cell [97]. The proposed comparator receives a differential input (ΔV_{in}) through two identical VCOs. So, the differential frequency resulting from the inputs' difference can be written as [97]

$$F_{\text{osc_diff}} = F_{\text{ref}}\{\Delta V_{\text{in}}/2\} - F_{\text{in}}\{-\Delta V_{\text{in}}/2\} = \frac{(I_{\text{out}}\{\Delta V_{\text{in}}/2\} - I_{\text{out}}\{-\Delta V_{\text{in}}/2\})}{N \cdot V_{\text{DD}} \cdot C_{\text{tot}}} \quad (4.2)$$

According to Fig. 4.5, the generated current through the controlling PMOS (I_{cont}) is reflecting to I_{out} by a mirroring factor of κ_m . Owing to the saturation-operating of M_{P1} , the biasing current to the current-starved delay cells is given by

$$I_{\text{out}}\{V_{\text{in}}\} = \kappa_m \cdot I_{\text{cont}} = \kappa_m \cdot \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L}\right)_{\text{P1}} \underbrace{(V_{\text{DD}} - V_{\text{in}} - V_{\text{th}_p})}_{V_{\text{GS}_{\text{P1}}}}^2 \quad (4.3)$$

Having two VCOs with alike parameters and substituting equation (4.3) in (4.2) leads to

$$F_{\text{osc_diff}} \simeq \frac{-(\kappa_m \cdot \frac{1}{2} \mu_p C_{ox} (\frac{W}{L})_{\text{P1}}) \cdot (2(V_{\text{DD}} - V_{\text{th}_p}) \cdot \Delta V_{\text{in}})}{N \cdot V_{\text{DD}} \cdot C_{\text{tot}}} \quad (4.4)$$

Therefore, the total voltage-to-frequency (V2F) conversion gain can be expressed as:

$$\text{Gain}_{\text{VCO}} = \frac{F_{\text{osc_diff}}}{\Delta V_{\text{in}}} \simeq \frac{-\kappa_m \cdot \mu_p C_{ox} (\frac{W}{L})_{\text{P1}} \cdot (V_{\text{DD}} - V_{\text{th}_p})}{N \cdot V_{\text{DD}} \cdot C_{\text{tot}}} \quad (4.5)$$

Since the controlling voltage is inserted into a PMOS transistor in each delay stage, the conversion gain is negative.

4.4.2 Resolution

Resolution in a comparator usually defines the minimum voltage difference at the input that can be detected by the comparator. The time difference between the rising edge of the VCOs' output pulse signals in cycle i can be written as

$$t_{d_i} = \left(\frac{2i-1}{2}\right) \cdot \left|(\tau_{\text{ref}} - \tau_{\text{in}})\right|, \quad (4.6)$$

where τ_{in} and τ_{ref} are the oscillation period of VCO_IN and VCO_REF outputs, respectively. Due to restricting effect of the PFD's DZ time (t_{dz}), the comparator can only provide a

correct result when $t_{d_i} \geq t_{dz}$. Therefore, the required number of oscillation cycles to satisfy this condition is given by [97]

$$\text{NOC} = \left\lceil \frac{t_{dz}}{\tau_{\text{ref}} - \tau_{\text{in}}} + \frac{1}{2} \right\rceil + \frac{1}{2}, \quad (4.7)$$

which indicates that in the ideal case of $t_{dz} = 0$, only one cycle of oscillation is needed. According to Fig. 4.4, the comparator activation time equates the duration at which $\overline{V_{\text{dis}}}$ is at low potential. Since it obviously depends on the NOC and the output frequency of two VCOs, the comparison time of the comparator can be found as

$$t_{\text{comp}} = \left(\frac{2 \cdot \text{NOC} - 1}{2} \right) \min\{\tau_{\text{ref}}, \tau_{\text{in}}\} \quad (4.8)$$

Using equation (4.7) and supposing $V_{\text{in}} > V_{\text{ref}}$ which means $F_{\text{in}} < F_{\text{ref}}$ and $\tau_{\text{in}} > \tau_{\text{ref}}$, we have

$$t_{\text{comp}} = \left(\frac{2 \cdot \text{NOC} - 1}{2} \right) \cdot \tau_{\text{ref}} \quad (4.9)$$

and

$$t_{dz} = \left(t_{\text{comp}} - \frac{\tau_{\text{ref}}}{2} \right) \cdot \left(\frac{\tau_{\text{in}}}{\tau_{\text{ref}}} - 1 \right) \quad (4.10)$$

To find the minimum detectable voltage difference between the inputs (ΔV_{min}), we can retrieve equation (4.10) in response to $V_{\text{ref}} = V_{\text{in}} - \Delta V_{\text{min}}$

$$t_{dz} = \left(t_{\text{comp}} - \frac{\tau_{\text{ref}}}{2} \right) \cdot \left(\frac{F_{\text{ref}}\{V_{\text{in}} - \Delta V_{\text{min}}\}}{F_{\text{in}}\{V_{\text{in}}\}} - 1 \right) \quad (4.11)$$

According to equation (4.1) and the similar features of two VCOs, we can approximate

$$t_{dz} = \left(t_{\text{comp}} - \frac{\tau_{\text{ref}}}{2} \right) \cdot \left(\frac{I_{\text{out}}\{V_{\text{in}} - \Delta V_{\text{min}}\}}{I_{\text{out}}\{V_{\text{in}}\}} - 1 \right) \quad (4.12)$$

Using equation (4.3) and ignoring the high order terms of ΔV_{min} , we can find the following simplified equation of

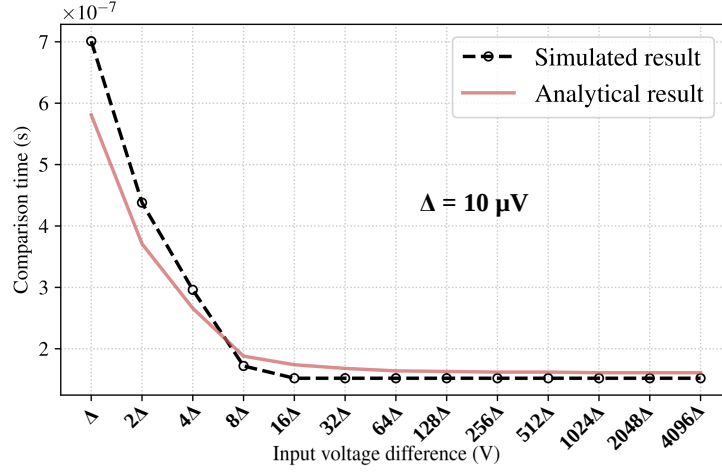


Figure 4.6 Comparison time (t_{comp}) versus differential input differences for $\Delta = 10 \mu\text{V}$

$$I_{\text{out}}\{V_{\text{ref}}\} = I_{\text{out}}\{V_{\text{in}} - \Delta V_{\text{min}}\} \simeq \alpha + \beta \cdot \Delta V_{\text{min}} \quad (4.13)$$

where α is $I_{\text{out}}\{V_{\text{in}}\}$ equal to (4.3) and β is a constant equal to

$$\beta = \kappa_m \cdot \mu_p C_{ox} \left(\frac{W}{L}\right)_{\text{P1}} (V_{\text{DD}} - V_{\text{in}} - V_{\text{th}_p}) \quad (4.14)$$

By substituting equations (4.3) and (4.13) in equation (4.12), we have

$$t_{\text{dz}} = (t_{\text{comp}} - \frac{\tau_{\text{ref}}}{2}) \cdot \left(\frac{\alpha + \beta \cdot \Delta V_{\text{min}}}{\alpha} - 1 \right) \quad (4.15)$$

Therefore, the comparison time and the resolution of the comparator can be approximated as

$$t_{\text{comp}} = \frac{\alpha \cdot t_{\text{dz}}}{\beta \cdot \Delta V_{\text{min}}} + \frac{\tau_{\text{ref}}}{2} \quad (4.16)$$

and

$$\Delta V_{\text{min}} = \frac{\alpha \cdot t_{\text{dz}}}{\beta \cdot (t_{\text{comp}} - \frac{\tau_{\text{ref}}}{2})} \quad (4.17)$$

As a result, the comparator resolution is directly influenced by the comparator resolving time and the DZ of PFD. Fig. 4.6 presents the comparison time of the proposed TD-comparator versus input voltage difference based on the analytical model (4.17) and simulated results. As shown, increment in the comparison duration time can enhance the resolution, owing to suppression of the available DZ at the cost of a longer activation time of the comparator (see Fig. 4.4). It is worth noting that the time taken by a comparator to resolve a small input difference is of critical importance, as it determines the clock frequency, sampling rate, and convergence speed in any data acquisition applications.

4.4.3 Input-Referred Offset (IRO)

The input-referred offset (IRO) of a comparator is an important performance metric for high-resolution applications. Mismatches between the symmetrical devices lead to an IRO voltage (V_{offset}) that can affect the charge/discharge characteristics and cause timing errors at the output delay stages chain. V_{offset} induced by the mismatch between VCOs at the input of the comparator multiplies with the V2F conversion gain, resulting in a frequency offset (f_{offset}) at the differential output of VCOs. Considering that the proposed VCO's conversion gain is negative, an additional V_{offset} reduces the accumulated time delay difference at the input ports of the PFD. According to (4.6), the time difference between the period of frequency signals at the input of the PFD must be greater than $2 \cdot t_{\text{dz}}$ to produce a toggle response at the comparator's output. Thus, the minimum distinguishable time difference by the PFD, which is equal to t_{dz} , can be translated into a specific amount of IRO. Consequently, in order to reduce offset voltage in the proposed TD-comparator, the mismatch between VCOs is minimized through the proper physical layout implementation and the performance of the proposed PFD is optimized to exhibit a minimal t_{dz} as explained in Section 4.3.3.

Offset voltage analysis is performed by inserting a slow ramp signal of ± 10 mV and $100 \mu\text{s}$ duration into V_{in} , while setting V_{ref} to a common mode voltage of 1.4 V. The input voltage difference at the crossing time of the comparator output is measured over 1000 iterations. The Monte Carlo simulation result incorporating process variation and mismatch is shown in Fig. 4.7. The mean value of the input-referred offset of the proposed design is $61.6 \mu\text{V}$ with a standard deviation of $28.9 \mu\text{V}$. Furthermore, corner simulations were performed at combinations of temperature variations from -40 to 85°C and supply voltage variations of 10% to demonstrate the robustness of the circuit offset with PVT variations. Fig. 4.8 shows the nominal and worse corner simulations which indicates less than 8% deviation in the worst-case scenario.

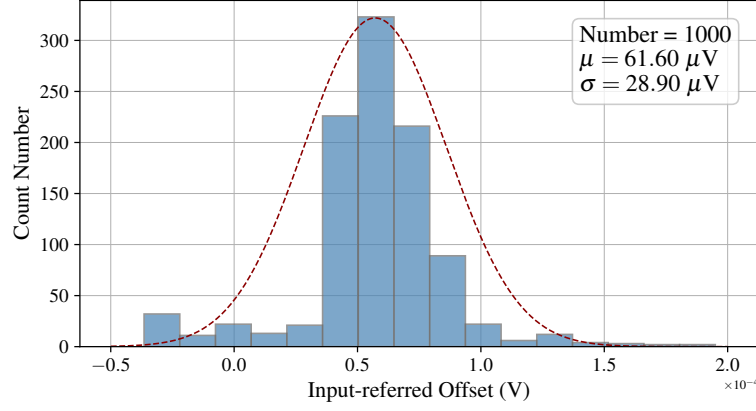


Figure 4.7 Monte-Carlo simulation results of IRO

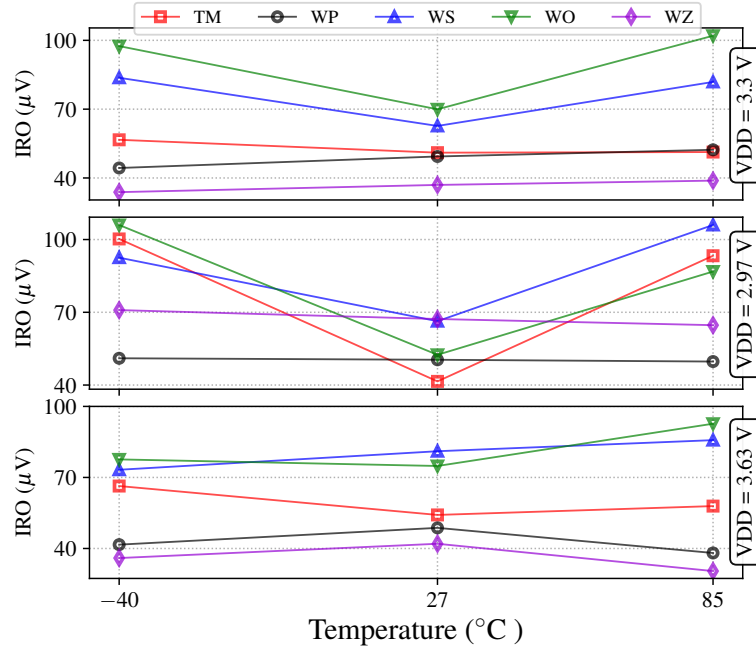


Figure 4.8 Simulated IRO characteristics throughout the PVT variations

4.4.4 Input-Referred Noise (IRN)

In a ring-VCO, the propagation delay of each cell, and hence the oscillation period, is jittered by noise during the pullup or pulldown process. This uncertainty in propagation delay at each delay cell can be modeled by a current noise spectral density of $\overline{i_n^2}$ along with the average current I_{out} across the total capacitance, C_{tot} . As the final output is a composite of the uncorrelated random noises from each delay cell, the standard deviation of the phase error due to the N stages must be taken into account. A straightforward analysis of [68, 102]

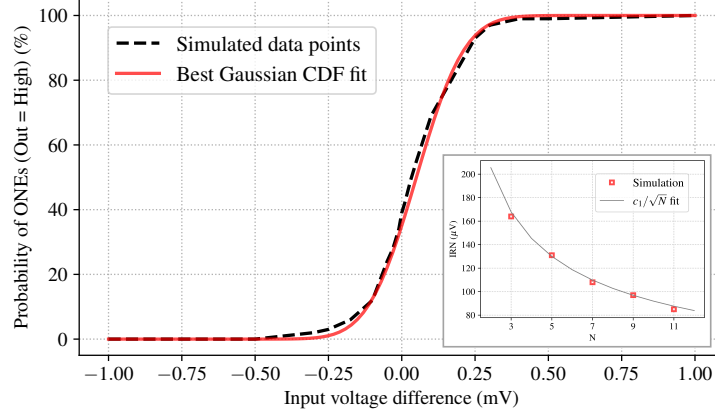


Figure 4.9 Simulated probability of output “high”, inferring IRN. Inset: IRN vs. number of delay stages

reveals that the total IRN of the VCO-based comparator is inversely proportional to $\sqrt{N}$. Therefore, the IRN of the comparator can be enhanced by designing a VCO with low phase noise (small jitter) or increasing the number of stages in the VCO.

Likewise, multistage VCO-based comparator improves IRN by integrating signals through oscillation cycles [19]. According to equation (4.5), increasing the N or adding an extra load capacitance at the output node of delay cells in addition to the parasitic capacitance, reduces the frequency difference between VCOs outputs. It means that the pulse difference of PFD’s input could be decreased and may be within the DZ region. Therefore, the number of oscillation cycles (NOCs) would be increased to get out of the DZ or overcome the available jitter. As a result, an increment in the oscillation cycle reduces the IRN. However, it enlarges the power consumption, area and phase errors resulting from the mismatch between delay stages. Finally, considering the time, area, power, eventual phase mismatch and targeted frequency (up to 10 MHz), five delay stages ($N = 5$) have been chosen in this work.

The SPECTRE transient noise simulation is utilized to determine the IRN of the comparator. With varying input differential voltages, the outputs of 500 comparisons are stored for each input voltage value. The probability of ONEs appearing on the output was subsequently counted. Assuming a Gaussian process for the noise, the effective IRN can be calculated by fitting the simulation results to the normal cumulative distribution function (CDF) [102]. Fig. 4.9 plots the outcomes of the transient noise analysis at a variety of input voltage differences. Curve fitting results in an IRN of $130 \mu\text{V}_{\text{rms}}$ for the proposed design. Also, the IRN of the proposed VCO-based TD-comparator versus the number of delay cells is shown in the inset of Fig. 4.9. As expected, the IRN voltage is attenuated by increasing the number of delay stages.

4.4.5 Energy Consumption per Comparison

Considering the required comparison time of the proposed TD-comparator, the average energy dissipation per comparison can be estimated as [97]

$$E_{\text{comp}} \propto (P_{\text{IN}} + P_{\text{REF}}) \cdot t_{\text{comp}} \quad (4.18)$$

where P_{IN} and P_{REF} are the power dissipation of VCO_IN and VCO_REF, respectively. Using equations (4.16) results in

$$E_{\text{comp}} \propto (P_{\text{IN}} + P_{\text{REF}}) \cdot \left(\frac{\alpha \cdot t_{\text{dz}}}{\beta \cdot \Delta V_{\text{in}}} + \frac{\tau_{\text{ref}}}{2} \right) \quad (4.19)$$

Consequently, the comparison energy relies on the supply voltage and the DZ of the PFD. In addition, it is inversely proportional to the voltage input difference. As expected, in the presence of non-negligible DZ and small input difference, the comparator has to dissipate more energy to make a decision.

4.5 Measurement Results

The proposed TD-comparator was fabricated in a 0.35 μm CMOS technology. The chip prototype is wire-bonded inside a 40 pins Dual in-line (DIP) ceramic package, and it is soldered onto a two-layer custom printed-circuit board (PCB) for measurements. Surface mount capacitors with values of 0.1 μF and 10 μF are used to decouple the power rails. The die photomicrograph is presented in Fig. 4.10. The VCO-based comparator's active area is 0.01 mm^2 while the VCO and the PFD occupy 36% and 21% of the total area, respectively. In order to support different modes of operation, some multiplexers have been incorporated into the chip prototype. In this manner, it is possible to select the input signals of the VCO and the PFD and evaluate their performance as a standalone circuit.

4.5.1 VCO

Fig. 4.11(a) illustrates the measured oscillation frequency of the VCO versus its tuning voltage. The proposed VCO visually exhibits an improved linear performance. The nonlinearity error over the 2 V controlling range is presented in Fig. 4.11(b), yielding a maximum error of 0.9%. The measured output frequency is 0.01 MHz to 9.37 MHz with a voltage control ranging from 0 to 2 V. This corresponds to a gain of 4.7 MHz/V and a frequency tuning

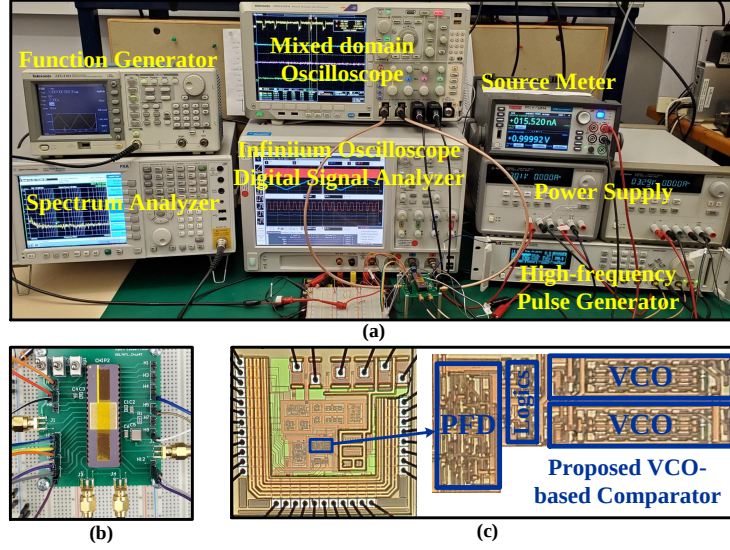


Figure 4.10 Experimental measurements: (a) Test bench setup, (b) prototype PCB of the design, and (c) die micrograph of the fabricated chip and the proposed VCO-based TD comparator

range ($TR_f = \frac{f_{\max} - f_{\min}}{f_{\text{central}}}(\%)$), of 199.5%. Fig. 4.12 depicts the measured spectrum and phase noise of the integrated VCO, where it exhibits -147.57 dBc/Hz at 1 MHz offset from a 9.37 MHz carrier. In low noise applications, a low phase noise VCO is crucial to maintaining signal quality and reducing interference and error rates. Since the phase noise will be input referred through the VCO sensitivity (gain), VCO designs with higher gain (with respect to the phase noise) can be used to improve the IRN performance of a TD-comparator at the expense of increased power dissipation and integration area.

4.5.2 PFD

Fig. 4.13 displays the operation waveforms of the proposed PFD at 500-MHz input frequencies when F_{ref} is leading F_{in} . In Fig. 4.13(a), the PFD outputs, UP and DN, are shown when the input phase difference is as small as 2.211° . While, Fig. 4.13(b) shows the PFD response for a phase difference close to 2π , 355.909° . As can be seen, the glitches and unnecessary one-shot pulses have been eliminated in the proposed design. Although the schematic simulation results demonstrate a DZ and BZ-free PFD, the noise contribution during experimental testing leads to a small amount of error. The measured DZ and BZ of the proposed PFD are found to be less than 12 and 22.7 ps, respectively. Fig. 4.14(a) presents the measured $\phi - V$ characteristics of the proposed PFD at 100 MHz, which represents the average output value relative to the input phase difference. The transfer characteristic reveals that the proposed PFD exhibits linear behavior over a wide operation range of $[-2\pi, 2\pi]$, with minimal DZ and BZ spots.

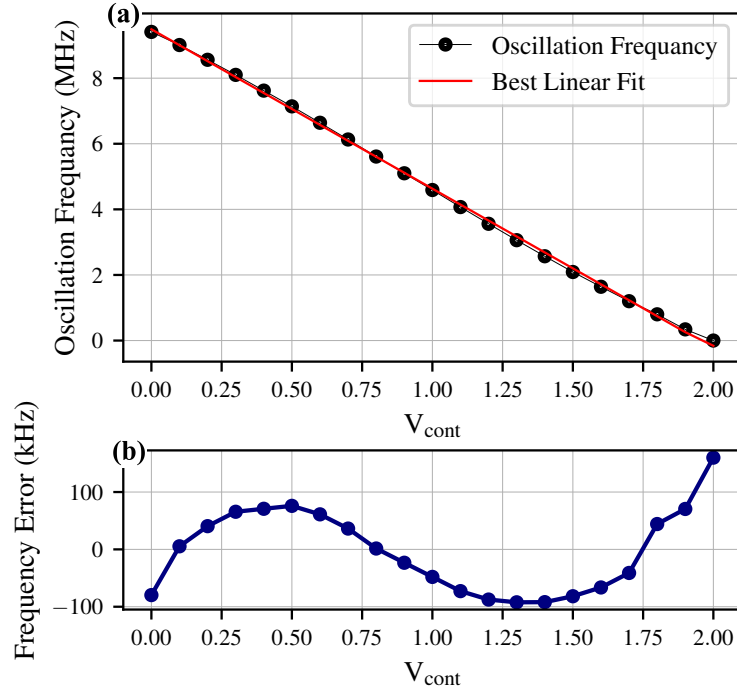


Figure 4.11 (a) Measured oscillation frequency of the proposed VCO versus the control voltage, and (b) the nonlinearity error of the VCO frequency

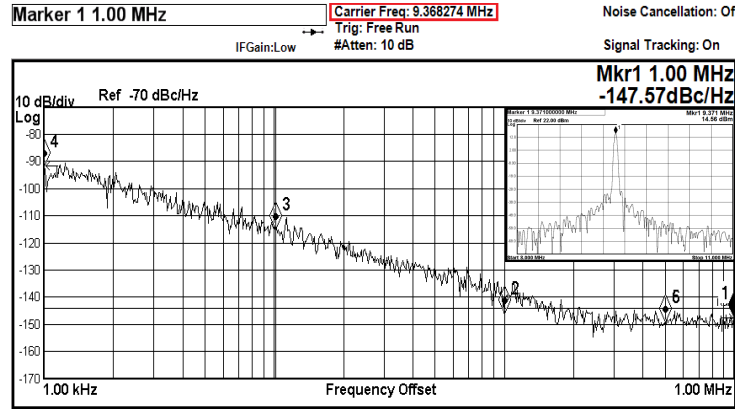


Figure 4.12 Measured spectrum and phase noise performance of the proposed VCO

The noise generated in the PFD device modulates the width and edge of the output UP and DN pulses, causing a random component in the following block and affecting the yield of the system. It would be most significant when the phase noise modulates the widths of the UP and DN signals differently [103]. Since the proposed PFD follows the ideal state diagram, UP and DN would not be simultaneously activated. Therefore, in the proposed design, the phase noise modulates only the UP or the DN pulse with respect to the frequency and phase

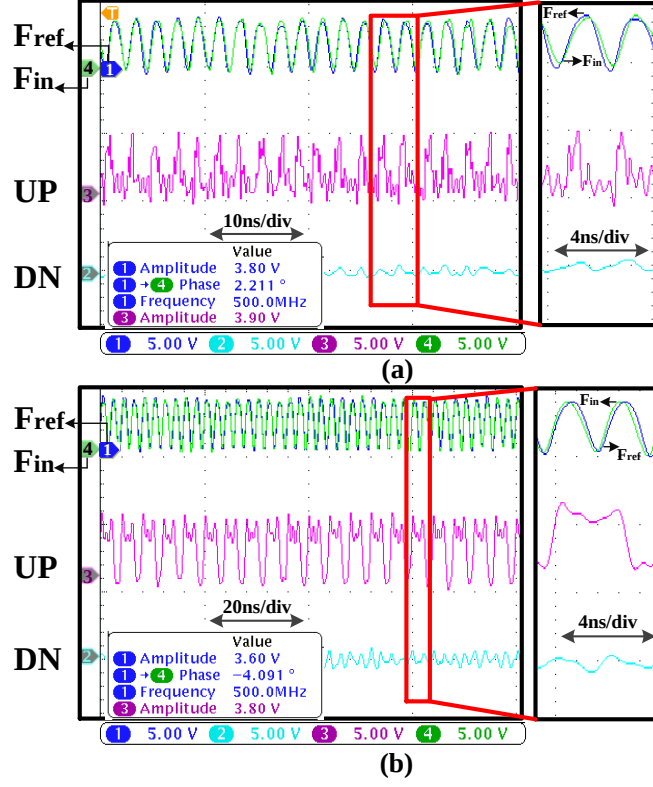


Figure 4.13 Oscilloscope waveforms of the proposed PFD; Measured UP and DN output signals (a) when $\Delta\phi$ is close to 0° , and (b) when $\Delta\phi$ is close to 360°

of the input signals. Fig. 4.14(b) illustrates the measured phase noise behavior of the PFD, where F_{in} and F_{ref} were set at 100 MHz and with 90° phase difference. Different noise sources can contribute to the PFD, such as DZ, finite reset time, and transistors. The phase noise of the proposed PFD is -136.71 dBc/Hz at 1 MHz offset. A performance summary of the proposed PFD is presented in Table 4.1. Compared to prior art PFD designs, the proposed design consumes less area and power, while offering advantageous DZ, BZ, and phase noise characteristics. The maximum operation frequency (f_{MAX}) is defined as the shortest period with correct UP and DN signals when input signals have the same frequency and 90° phase difference [28]. The post-layout simulated f_{MAX} for the proposed PFD is 1.32 GHz. The operating frequency is directly related to the speed of the transistors in response to the input signals; therefore, a scaled-down technology node with a lower minimum length will improve the f_{MAX} of the proposed design.

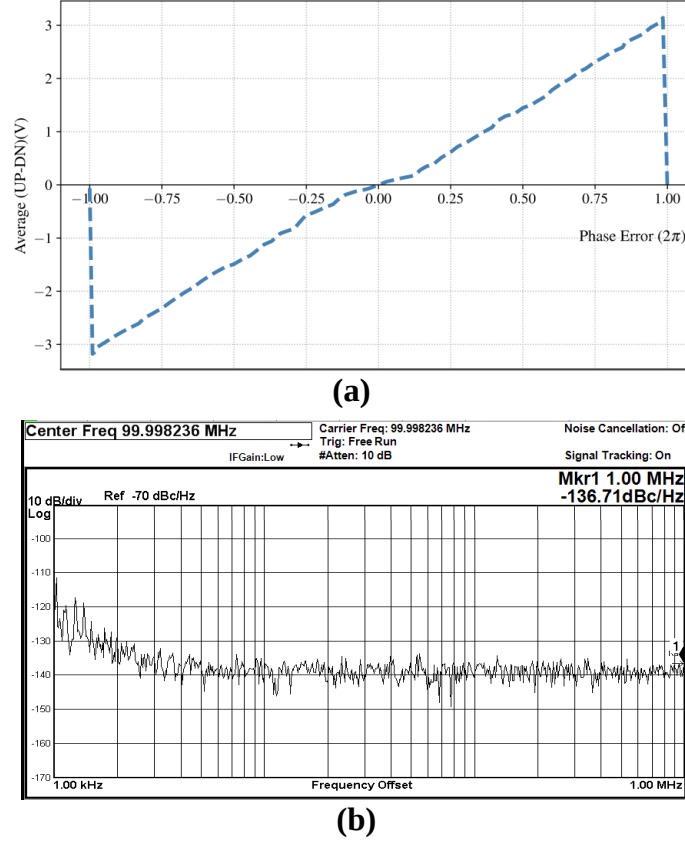


Figure 4.14 (a) Measured transfer characteristics ($\phi - V$), and (b) measured phase noise performance of the proposed PFD at 100 MHz

4.5.3 VCO-based TD-comparator

To characterize the offset of the comparator prototype, one of the comparator inputs is connected to a reference voltage. The other input is driven by a ramp signal which increases gradually over time from below the V_{ref} . Through an Infiniium digital signal analyzer, the output of the comparator is monitored in order to detect the input voltage difference when the output signal toggles (the trip point). The measurement is repeated 500 times, and the mean of these 500 points is interpreted as the offset [29]. The measurement instrument's offset and noise are obtained when the inputs of the analyzer are shorted and have been removed from all the following results. Fig. 4.15 illustrates the IRO histogram of the proposed VCO-based TD-comparator. The statistical information regarding the offset distributions of five comparators from five different chips indicates the minimum, maximum, and mean of $-74.2 \mu\text{V}$, $124.69 \mu\text{V}$, and $69.25 \mu\text{V}$, respectively. The standard deviation of the offset is $81.14 \mu\text{V}$ among the five circuits.

Fig. 4.16 illustrates the measured IRN of the proposed TD comparator. Based on the best

Table 4.1 Performance summary and comparison of the proposed PFD with prior-art publication

Reference	[20] ^a	[28] ^a	[27]	[24]		[25]	This Work
Tech. (nm)	350	180	130	130	350	250	350
Supply (V)	3.3	1.8	1.2	1.2	1.8	N.A	3.3
P _{avg} (mW)	0.0425	N.A	0.496	0.296	2.8	1.4	0.858
@f _{osc} (MHz)	@ N.A		@128	@128	@528	@500	@500
f _{MAX} (GHz)	1	2.5	2.94	2.5	N.A	1.53	1.32 ^a
PN ^b (dBc/Hz)	N.A	-113.5	N.A	N.A	-109.8	N.A	-136.7
Dead-zone	Free	Free	N.A	N.A	N.A	Present	12 ps
Blind-zone	N.A	N.A	61 ps	156 ps	Present	Present	22.7 ps
Glitch	Free	Free	Present	N.A	Free	N.A	Free
Area (mm ²)	0.002	0.004 ^c	0.04 ^c	N.A	0.045	0.09 ^c	0.0021
$\Delta\phi$ range	$\pm\pi$	$\pm\pi$	$\pm 2\pi$	N.A	N.A	$\pm 1.4\pi$	$\pm 2\pi$

^a Simulation results, ^b Phase noise (PN) at 1 MHz offset frequency, ^c Estimated from die micrograph

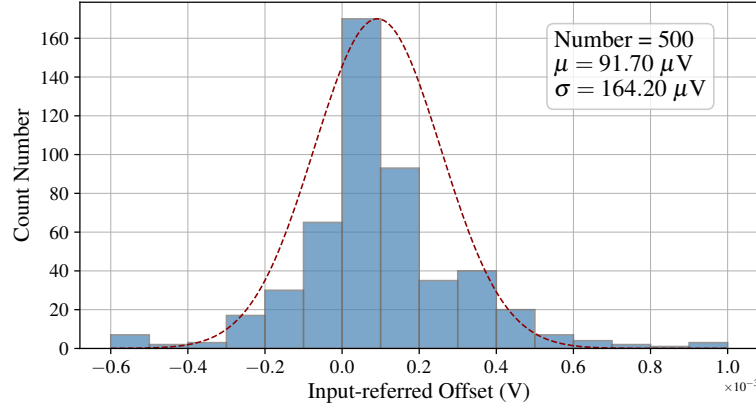


Figure 4.15 Histogram of the measured trip points for the proposed TD-comparator

gaussian CDF fit, the proposed comparator achieves $148 \mu\text{V}_{\text{rms}}$ noise. Table 4.2 summarizes the performance of the prototype TD-comparator and compares it to recently published designs. During normal operation, the comparator consumes $28.37 \mu\text{A}$ current from the 3.3 V supply. The detailed power breakdown of the TD-comparator indicates that VCOs dominate with 86.39% of the power, whereas the PFD and logic circuits consume only 2.77% and 10.84% , respectively. In comparison with the state-of-the-art, the proposed TD-comparator achieves lower offset, lower noise level with a reasonable speed at the cost of additional power and energy consumption.

Table 4.2 Performance summary and comparison of the proposed time-domain comparator with prior-art publications

Reference	Tech. (nm)	Supply (V)	Power (μ W)	IRN (μ V _{rms})	IRO (mV)	Speed (MHz)	Normalized Speed	Energy (pj/comp.)	Normalized Energy	Area (mm ²)	Architecture
This Work	350	3.3	93.65	148	0.081	2.7	32.97	34.6	188.5	0.01	VCO-based
TCASII'22 [73]	180	1.8	4	140	1.8	2.4	18.52	1.67	63.32	0.0057 ^b	VCDL-based
JSSC'19 [19]	40	1.1	N.A	380 ^a	N.A	10	10.22	N.A	N.A	0.0021 ^b	VCO-based
JSSC'20 [72]	40	1.1	55	100	N.A	4	4.09	13.75	1508	0.0037 ^b	VCO-based
ISSCC'08 [71]	180	1	1	150	N.A	1.4	20.56	0.714	107.3	0.02 ^b	V2T conversion
JSSC'11 [66]	180	0.6	0.13	65 ^a	1.82	1.2	27.3	0.11	50.03	0.003 ^b	VCDL-based
JSSC'18 [67]	90	0.5	0.567	N.A	4.22	1.4	10.76	0.405	453.9	0.009 ^b	VCDL-based
TVLSI'21 [68]	65	0.85	16.2	212.13 ^a	N.A	15	37.5	1.08	1136.8	0.003 ^b	VCO-based
JSSC'17 [69]	40	N.A	0.104	38 ^a	6.5 ^a	0.3	0.31	0.35	383.9	0.00054	Edge-pursuit
TCASII'20 [100]	180	1	0.028	N.A	0.6	0.052	0.76	0.54	81.1	0.00697	VCDL-based

^a Simulation results, ^b Estimated from die micrograph

Usually, long-channel technology nodes, and their high supply voltages, degrade the power efficiency of the design. Therefore, Table 4.2 contains a normalized speed and energy consumption to ensure a fair comparison among designs implemented in different technologies. Since TD-comparators operate in the same manner as digital intensive circuits, a good performance comparison can be made based on the characteristics of a single inverter in a chain of Fan Out 4 (FO4) models at a specific CMOS process [104]. Thus, the speed of each comparator listed in Table 4.2 is normalized by the delay of a single inverter in the middle of a FO4 chain at their same supply voltage and technology node. Likewise, the average energy required for state switching of that same single inverter is employed for the energy normalization [29]. The manufacturers' test results for certain technology and supply are derived from the International Technology Roadmap for Semiconductors (ITRS) [105] and the Predictive Technology Models (PTMs) [106]. According to the normalized speed and energy figures of merit, the proposed TD-comparator operates relatively fast and consumes a comparable energy compared to the prior art designs.

The most recently published TD-comparators have been applied in the development of successive approximation register (SAR) ADCs. Therefore, it is also intuitive to examine the design properties that might be supported by the proposed comparator if it were to be incorporated into a standard SAR ADC. Let's take a 12-bit SAR ADC with 2-V input for an example; the least-significant bit (LSB) is about 488.3 μ V. To ensure that the 3σ noise is within an LSB step, the IRN has to be lower than 163 μ V. Also, based on the ENOB

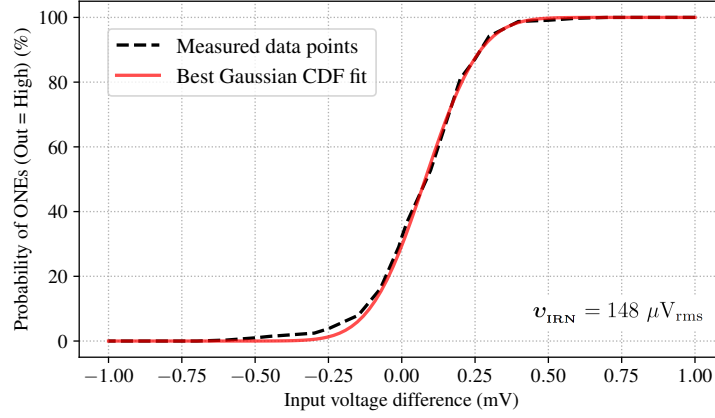


Figure 4.16 Measured IRN of the proposed TD-comparator. Probability of output “high” vs. differential input difference, and curve fitting to the normal CDF

estimation provided in [66] and [107], since the IRN induced by the proposed comparator is less than 0.5 LSB, an ENOB of more than 11 can be achieved. According to Fig. 4.6, for an input voltage difference of $488 \mu\text{V}$, the comparison time does not exceed 152 ns. Since the comparison time is limited to half of the clock period, the maximum clock frequency that can be tolerated by the comparator for this input difference is 3 MHz. Therefore, the proposed TD-comparator can support a maximum sampling rate of 200 kS/s in a 12-bit SAR ADC.

4.5.4 Technology Scaling Effect

Due to the time-domain operation of VCO-based comparators, they are well suited to process scaling, allowing them to achieve a faster operation and a higher resolution [19, 72, 73]. To further analyze the scaling impact, we estimate the performance of the proposed TD-comparator in advanced technologies by utilizing the technique described in [104]. Based on an accurate method, this work has developed polynomial approximations for the delay, energy, and power performance scaling factors for a targeted technology node and supply voltage (see equations (5)-(7) in [104]). In accordance with the same approach, we have derived these polynomial scaling approximations and corresponding coefficients for the 350 nm technology. As a result, the derived scaling factors, together with the provided data sets in [104] (Table 5), allow us to estimate and compare the performance of the proposed design under different technologies and supply voltages. For instance, in 90-nm CMOS technology with a 1.1 V supply voltage, the power consumption of the proposed TD-comparator can be reduced to $6.6 \mu\text{W}$ while consuming energy per comparison of 0.51 pJ/comp. at a conversion rate of 12.9 MHz. Also, the silicon area can be shrunk to 0.000662 mm^2 .

As scaling technology reduces the propagation delay of MOSFETs through shrinking parasitic

capacitance and minimum length, the DZ of the PFD and hence the comparison time of the proposed comparator are likely to be improved. Accordingly, the proposed design is expected to exhibit a marginal degradation of offset behavior in advanced technologies. Given the fact that the proposed TD-comparator delivers, on average, a 30 times lower offset than prior-art designs, it is reasonable to presume that the proposed comparator would retain its advantageous offset characteristic in a scaled-down process. The proposed architecture, however, may experience noise performance degradation in more scaled nodes, mainly due to the fact that the noise proportion of the total signal increases as voltage swing and power consumption are reduced. The operation of a closed-loop VCO-based comparator implies an inherent trade-off in terms of noise, since the level of noise decreases as the NOCs increase [19, 68, 72]. As a result, in advanced technologies, due to the use of VCOs and DZ effect, which allow adaptive configuration of the comparator noise, noise performance can be optimized at the cost of comparison time and power consumption [72].

4.6 Conclusion

In this paper, a TD-comparator is implemented and fabricated in a 350-nm CMOS process, in which the input and reference voltages are converted into frequency signals through the use of two identical VCOs followed by a PFD and a control unit. The design of a linear VCO with low phase noise performance is outlined. Furthermore, the developed PFD features glitch-free low noise and low power operation. An innovative circuit configuration is proposed for the PFD that minimizes the reset process and accelerates the pre-charge of the internal nodes. Taking advantage of these attributes, the proposed PFD exhibits a linear ϕ -V characteristics from almost -2π to 2π , with a minimal DZ and BZ of 12 and 22.7 ps, respectively. During the comparison, the oscillation of VCOs continues as long as the time difference remains within the PFD DZ. Hence, it is found that the comparator IRO and resolving time can be alleviated by adopting a minimal DZ PFD without requiring multiple oscillation cycles such as in previous works that limited the comparator's speed. The TD-comparator prototype attained an IRN of $148 \mu V_{\text{rms}}$ and an IRO standard deviation of $81.14 \mu V$. The proposed comparator consumes $93.65 \mu W$ at a conversion rate of 2.7 MHz under a 3.3-V supply voltage while occupying 0.01 mm^2 active area.

4.7 Acknowledgment

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CHAPTER 5 ARTICLE 3 : A WIDE-RANGE LOW-POWER THYRISTOR-BASED DELAY ELEMENT WITH IMPROVED TEMPERATURE SENSITIVITY

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5.1 Abstract

This brief describes an improved CMOS thyristor-based delay element (THDE) in which two current sources, digitally-controlled (DC) and voltage-controlled (VC), are implemented to demonstrate the design choice trade-offs and offer a wide range of delays. Both THDE designs show reduced temperature sensitivity while allowing an extended tuning range. Prototypes fabricated in a 0.35- μm CMOS process exhibit measured delay range of 26 ns-4.5 μs for DC-based delay element and 16 μs -5 ms for VC-based delay element. At their maximum delay amounts, the integrated THDEs consume 4.1 and 1.58 μW , respectively, from a 3.3 V supply. Also, the fabricated delay cells show a temperature sensitivity of 900 and 2710 ppm/ $^{\circ}\text{C}$, respectively, when operating at maximum delay.

5.2 Introduction

Variable delay elements are key building blocks in several VLSI applications, such as asynchronous systems, self-timed dynamic logic, phase-locked loops (PLLs), delay-locked loops (DLLs), and non-overlapping clock generators for switch capacitor circuits [82]. Different applications may have varying requirements in terms of delay range. When it comes to high-frequency applications, delays in nanosecond (ns) range are needed, while for low-power smart devices, asynchronous state controllers, or low-frequency pulse generators, the micro-to millisecond (μs to ms) range of delays are required [84, 108].

Several analog and digital methods can be used to implement a delay element. A series of all-pass filters is a purely analog solution whose biasing scheme consumes significant static

power [109]. RC delay and inverter chain are two other common and easy-to-design techniques that exhibit large variations in delay times under different supply voltages and temperatures. Moreover, these schemes have no tunability except to select the number of cells. Differential delay stages provide stable characteristics, while suffering from complex biasing circuitry, static power, and small delay limits. Variable delay elements can also be designed using the current starved and variable resistor techniques [110]. In these designs, however, the lack of steepness in the output signal results in a crowbar current passing through the following circuit. Further, the slow charging and discharging process leads to erratic delays at the edge of the input signal, since the initial condition will not be the same for successive delays. Utilizing positive feedback may resolve this issue by settling the output of the delay element after receiving the delayed signal; thus, the circuit can accept the next input immediately [82].

A CMOS thyristor-based delay element (THDE) is a promising alternative to conventional designs. As the major delay component is controlled by the current source, it shows a high power supply rejection ratio and low temperature sensitivity. Also, its positive feedback mechanism enables fast switching response and minimal static power consumption. A THDE was first introduced in [79] and then improved in several aspects over the following years. For instance, the charge sharing issue, the need for additional dynamic triggering to reduce shunt current, and the lack of matching between the two operating current sources contributed to fluctuations in the output pulse width [80, 84, 111]. However, most of these designs are intended to provide delays in the range of ns and do not produce large delays. Moreover, the THDEs generally have low temperature sensitivity when the delay range is small. However, the stability of the delay with respect to temperature variation is compromised when μs to ms delays are required.

This brief concerns a compact, wide-range, enhanced temperature sensitivity, and low-power CMOS thyristor-based delay elements. Two different current source configurations are presented, allowing the proposed design to cover a wide range of delays, while the trade-offs associated with each version are outlined. The remaining of this paper is organized as follows: Section II describes the architecture of the proposed thyristor-based delay element, as well as two current source designs, and discusses their advantages, design considerations, and performance trade-offs. Section III presents the measurement results, while the conclusion is drawn in Section IV.

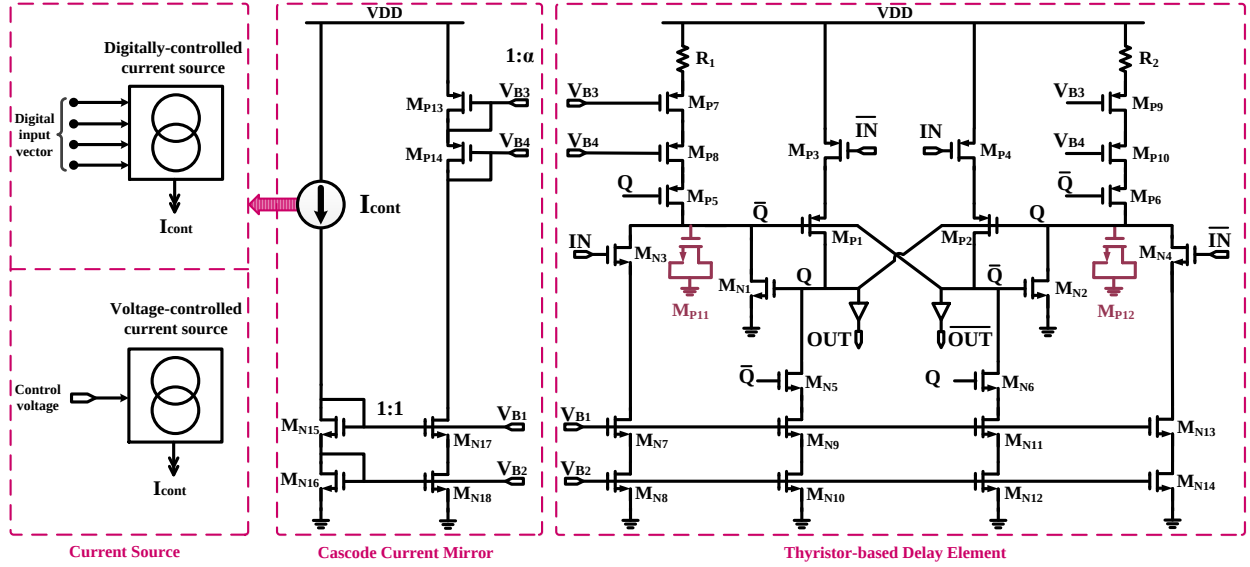


Figure 5.1 Proposed improved thyristor-based delay element

5.3 Circuit Description

5.3.1 Proposed Thyristor-based Delay Element (THDE)

Fig. 5.1 shows the circuit diagram of the proposed wide-range THDE with improved temperature sensitivity. The core of the design consists of two CMOS thyristors formed by the interconnected transistors M_{N1} - M_{P1} and M_{N2} - M_{P2} . These CMOS thyristors are triggered by a controllable current source to create the delay element. A cascode current mirror is used to reflect the controlling current, I_{cont} , to the circuit. The current mirroring ratios for the N-channel and P-channel transistors branches are 1:1 and 1: α , respectively, where $\alpha < 1$. In the following, the left half complementary circuit of the proposed THDE will be examined to describe the operation of the proposed structure.

Let us assume that M_{N1} and M_{P1} are turned off at the start point, which means that node Q is at GND potential and node $\bar{Q}$ is precharged to V_{DD} . Upon arrival of the rising edge of the input pulse signal, IN, the switch transistors M_{N3} and M_{P3} turn on and let the current flow to the core of the circuit. Thus, the voltage across the gate capacitance at node $\bar{Q}$ declines with respect to the applied current. When $\bar{Q}$ falls below $V_{DD} - V_{thp}$, M_{P1} becomes active and charges the gate capacitance on node Q. Once the threshold voltage, V_{thn} , is reached at this node, transistor M_{N1} turns on, generating a positive feedback through the thyristor structure M_{N1} - M_{P1} . This results in a rapid switching of the CMOS thyristor's state, and reducing the voltage at node $\bar{Q}$ to GND, while raising the voltage at node Q to V_{DD} . Consequently, the delayed rising edge of the input pulse signal appears at node Q and is reflected in the output

signal, OUT, after buffering. In a complementary manner, these triggering processes can be performed on the right half of the circuit in order to provide a falling edge delay.

Achievable delay duration is mainly determined by the charging and discharging times of the gate capacitance at nodes Q and $\overline{Q}$. It is because when IN is switched to high, the output signal will remain unchanged as long as these two nodes maintain their respective states. On the other hand, a sub-threshold leakage current may be drawn by M_{P1} and M_{N1} before the voltage at node $\overline{Q}$ drops below $V_{DD} - V_{thp}$ and at node Q raises above V_{thn} , respectively. In this case, the gate capacitance at node Q is charged erroneously, resulting in a slight voltage increase above GND. So, a buffer is required to sharpen the output pulse and prevent the flow of shunt current in subsequent blocks [84]. This undesired charging/discharging at nodes Q and $\overline{Q}$ also leads to an earlier occurrence of positive feedback in CMOS thyristors and a smaller amount of time delay. Besides, the subthreshold current can adversely affect design accuracy due to its high temperature and process sensitivity. The proposed design rectifies these limitations by using two additional transistor branches connected to nodes Q and $\overline{Q}$; a pull-down and pull-up transistor lines that couple the current source to the nodes Q and $\overline{Q}$ through M_{N5} and M_{P5} , respectively. Using $\overline{Q}$ to control M_{N5} ensures that the sub-threshold current of M_{P1} is sunk through M_{N9} - M_{N10} and avoids charging node Q. Also, the additional control over $\overline{Q}$ through M_{P5} mitigates the effects of possible leakage via M_{N1} . Furthermore, the pull-up current source results in the discharge of this instance with current of $(1 - \alpha) \cdot I_{cont}$ rather than I_{cont} through M_{N3} . This causes a slower discharging of capacitance at node $\overline{Q}$, allowing Q to remain at logic low for a longer period of time. Therefore, these interconnected branches reduce delay time limits, and unnecessary current sourcing or sinking. According to simulation results, the maximum achievable delay of the proposed THDE can be increased by a factor of $200\times$ when utilizing pull-up and pull-down current sources. Besides, the delay range of the circuit has been further improved by using transistors M_{P11} and M_{P12} , which function as capacitors and boost the capacitance values at nodes $\overline{Q}$ and Q, respectively.

Thanks to enhanced circuitry, simulation results indicate that the proposed THDE can produce an extensive range of delays from ns to ms. As mentioned earlier, thyristor-based delay approaches are generally less sensitive to temperature when dealing with ns delay ranges. Thus, to reduce the temperature sensitivity for the targeted wide range of delays, some considerations need to be taken. First, a proper simple method for temperature compensation is the use of a source degeneration resistor [112]. Therefore, two on-chip poly resistors, R_1 and R_2 , have been employed in the path of the pull-up transistor lines, which source current to the nodes $\overline{Q}$ and Q, respectively. Fig. 5.2 shows the temperature sensitivity of the proposed THDE with and without poly resistors at three delay values. Source degeneration resistors improve the temperature coefficient by factors of $2\times$, $14\times$, and $15\times$ for delay intervals of 26

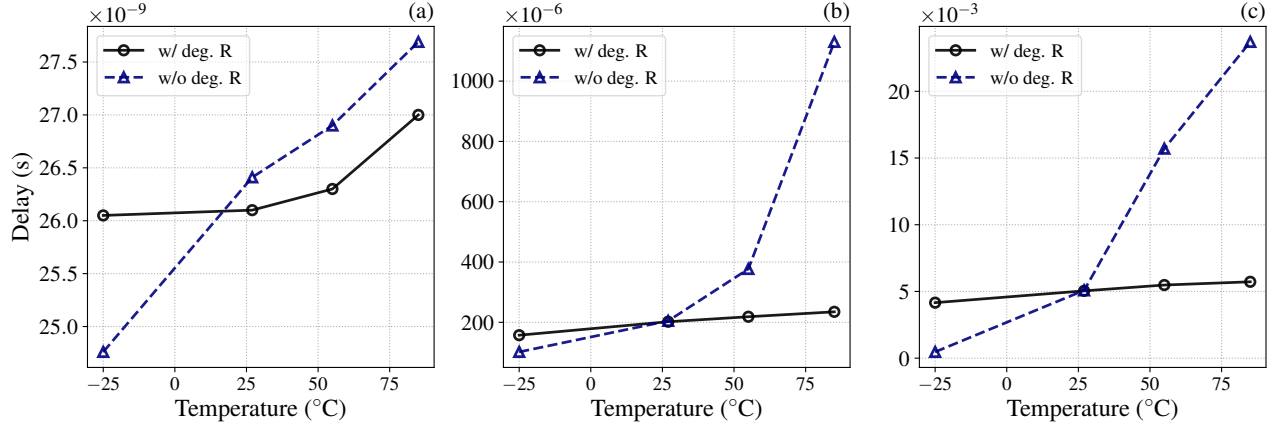


Figure 5.2 Output delay versus temperature with and without source degeneration resistors at (a) 26 ns, (b) 200 μ s, and (c) 5 ms

ns, 200 μ s, and 5 ms, respectively. Second, due to the fact that the proposed delay cell is directly governed by a current control, one of the main criteria for temperature compensation is the current source reference choice of implementation. Most of the current source designs are unable to retain their performance in a wide range of current. Consequently, we suggest two different current sources that cover different ranges of reference current while maintaining the tunability of the design and offering low sensitivity to temperature and process variations. Third, to obtain a delay amount in μ s to ms, most often a reference current with a relatively low output current value (e.g. 1-10 nA) is utilized [84]. However, circuits are more vulnerable to process variations and mismatches when operating at a very low current level. Therefore, the proposed circuit has been designed so that it is capable of providing large delay values with a moderate range of controlling current.

5.3.2 Voltage-controlled Current Source (VCCS)

Fig. 5.3(a) illustrates the temperature compensated VCCS which is adapted from the structure presented in [112]. The core of the VCCS circuit consists of M_{N1} , M_{P1} , M_{P3} - M_{P6} , and R_1 , which in [112] is driven by three off-chip bias voltages. The biasing scheme is modified in the proposed circuitry to be tuned by inserting a single controlling voltage, V_{cont} , into the gate of M_{N1} . Also, the employed biasing transistors resulted in a wider range of current compared to the design reported in [112]. As noted, a moderate range of current is selected in this work to cover μ s to ms extent of the delay. Fig. 5.4(a) shows the output control current of the VCCS versus its tuning voltage. A wide range of currents from 50 nA to 800 nA is achieved. It can be seen that the proposed scheme achieves a voltage tuning range ($TR_V = \frac{V_{cont_{max}} - V_{cont_{min}}}{V_{DD}} (\%)$) of 72.7%, which is $2.3\times$ better than the design in [112].

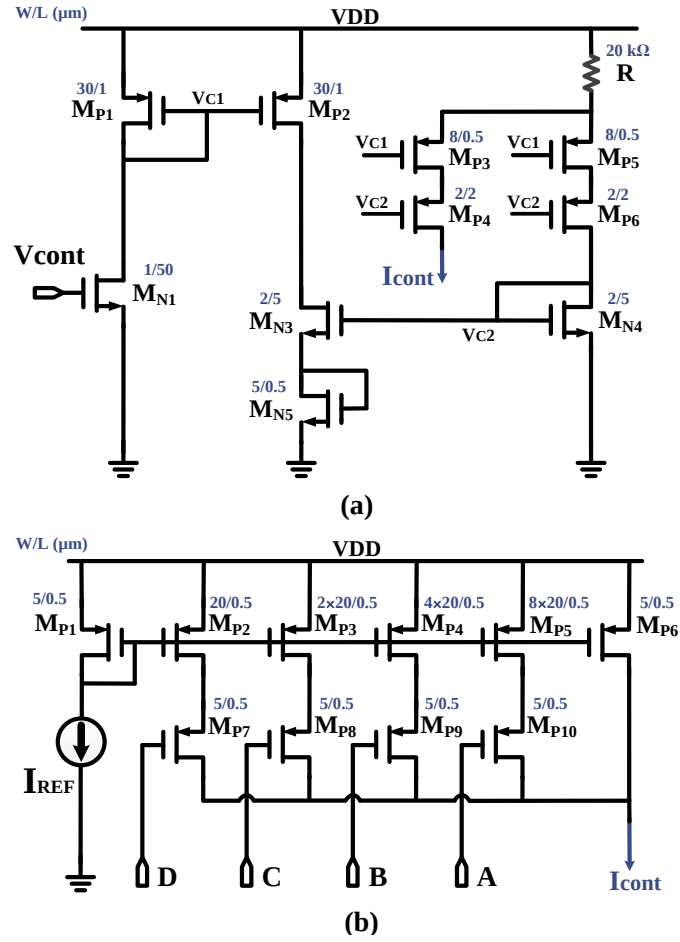


Figure 5.3 Circuit diagram of (a) the voltage-controlled current source, and (b) the digitally-controlled current source

5.3.3 Digitally-controlled Current Source (DCCS)

A digitally controlled delay element is proposed in [110] that allows the delay to be manipulated through digital means. A DCCS is employed in this design, as shown in Fig. 5.3(b), along with an inverter chain to provide the delay line. An ideal reference current, I_{REF} , and a group of pMOS transistors, M_{P1} - M_{P6} , are incorporated as current sources. As well, a 4-bit digital input vector controls this sourcing current through the use of four switch transistors of M_{P7} - M_{P10} . The ideal off-chip I_{REF} was used in [110] to reduce the dependency of the output delay on supply, process and temperature variations; however, it contradicts the purpose of integration.

The proposed THDE adopts this current source model while constructing its I_{REF} from the structure shown in Fig. 5.3(a) to accomplish a fully-integrated design. To provide a constant reference current, M_{N1} is replaced by a diode-connected nMOS, and the other MOS aspect

ratios are selected so as to achieve a current of $1 \mu\text{A}$. Fig. 5.4(b) presents the output control current of the DCCS with respect to the digital input vector. It can deliver control currents from $1 \mu\text{A}$ up to $50 \mu\text{A}$.

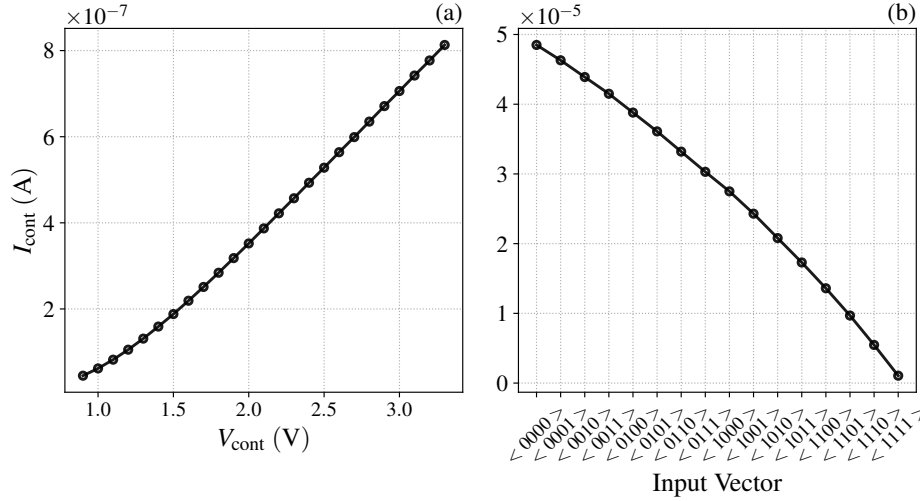


Figure 5.4 The output current of (a) VCCS, and (b) DCCS

5.4 Measurement Results

The proposed THDEs are implemented and fabricated using the AMS $0.35\text{-}\mu\text{m}$ CMOS process with a supply voltage of 3.3 V . The chip prototype is wire-bonded inside a 40 pins Dual in-line (DIP) ceramic package, and it is soldered onto a two-layer custom printed-circuit board (PCB) for experimental tests. The power rails are filtered using surface mount decoupling capacitors with values of $0.1 \mu\text{F}$ and $10 \mu\text{F}$. Also, the vacant space between the IO bond PADs and the core design is filled by decoupling capacitors inside the chip. The chip micrograph of the THDE prototypes is illustrated in Fig. 5.5.

For the sake of simplicity, we refer to the proposed THDE as “THDE_{VC}” when it incorporates the VCCS shown in Fig. 5.3(a), and as “THDE_{DC}” when it incorporates the DCCS shown in Fig. 5.3(b). Fig. 5.6(a) plots the output delay of the proposed THDE_{DC} against the binary input vector, as well as its variation with temperature. The output delay of 26 ns to $4.5 \mu\text{s}$ is obtained from a 4-bit digital input. For the maximum (max) and minimum (min) delay values, the measurement results indicate that, within the range of $-25 - 85^\circ\text{C}$, the variation in output delay is less than 9% and 2.6%, which corresponds to a temperature coefficient (or sensitivity S_T) of $900 \text{ ppm}/^\circ\text{C}$, and $240 \text{ ppm}/^\circ\text{C}$, respectively.

In Fig. 5.6(b), the output delay of the proposed THDE_{VC} as a function of the controlling input voltage is shown, along with its variance over temperature. Tuning V_{cont} from 0.9 V

Table 5.1 Process variation effect on the fabricated delay elements

σ/μ due to process spread (%)													
THDE _{DC}							THDE _{VC}						
Output delay	# of Chip						Output delay	# of Chip					
	I	II	III	IV	V	All		I	II	III	IV	V	All
26 ns	0.47	0.39	0.4	1.2	0.37	0.68	16 μs	3.19	2.1	3.3	1.62	2.23	3.8
200 ns	1.52	0.93	1.26	1.7	0.82	1.15	900 μs	5	4.14	7.3	3.9	4.87	5.68
4.5 μs	2.01	1.54	3.97	2.6	1.8	2.8	5 ms	9.68	6.55	10.9	5.54	9.2	8.5



Figure 5.5 Test bench setup and chip micrograph of the proposed THDEs

to 3.3 V provides a wide delay range from 16 μ s to 5 ms at nominal room temperature. For the max and min delay values, the measurement results show that, within the range of $-25 - 85^\circ\text{C}$, the variation in output delay is around 29% and 10%, which corresponds to a S_T of 2710 ppm/ $^\circ\text{C}$, and 965 ppm/ $^\circ\text{C}$, respectively. The measured power consumption of the proposed structures are shown in Fig. 5.7.

The measured accuracy of the proposed THDEs, which is defined as the standard deviation over the mean (σ/μ), is shown in Table 5.1 for the max, min, and nominal delay amounts for each circuit. Five available chips were measured, and 50 samples were collected from each chip for each delay value. It can be seen that the accuracy improves as the delay decreases. This is due to the fact that a lower output delay corresponds to a higher control current. And, since higher current values are attained from larger overdrive voltages of transistors, the impact of variations will be smaller compared to the nominal case. At the max delay amount, the measured standard deviations due to process spread for the proposed THDE_{DC} and THDE_{VC} are 2.8% and 8.5%, respectively.

5.5 Discussion

The performance of the prototype THDEs is summarized in Table 5.2, along with a comparison to previously published delay elements. Depending on the employed current source, the

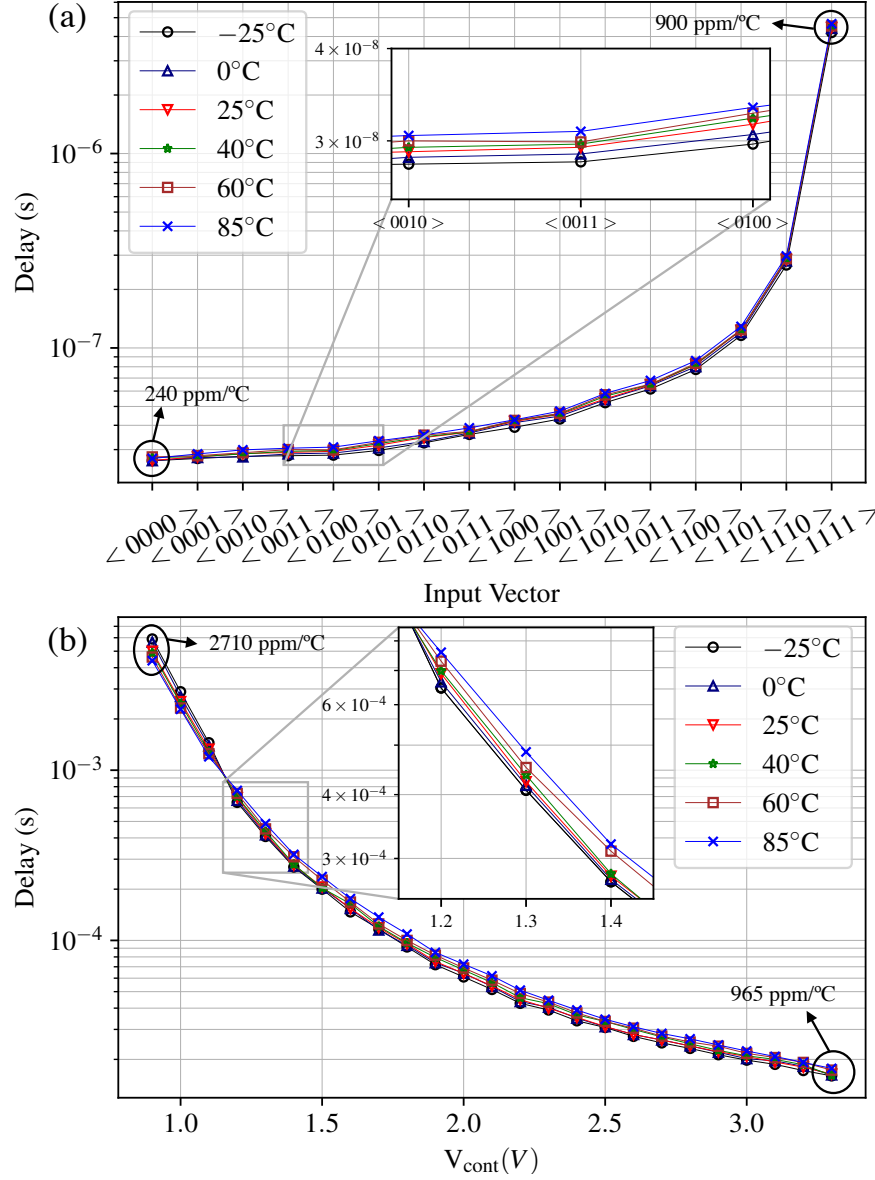


Figure 5.6 Measured delay time of the proposed (a) THDE_{DC}, and (b) THDE_{VC}

proposed delay cell is capable of providing a wide delay range between 26 ns and 5 ms, while showing low sensitivity to process and temperature variations.

At the same channel lengths as our employed technology, authors in [108] and [84] reported a wider delay range than the proposed design. This is attributed to the use of an ideal current source, which allows for any level of current and hence delay. It is also possible for the proposed THDE to provide a delay amount of more than 20 ms if supplied with a current of less than 10 nA at the cost of accuracy degradation. In [84], the threshold voltage of the PMOS transistor in the thyristor core is augmented by a diode-connected transistor in series with it. This results in an extension of the delay range since the required time for node $\bar{Q}$ to

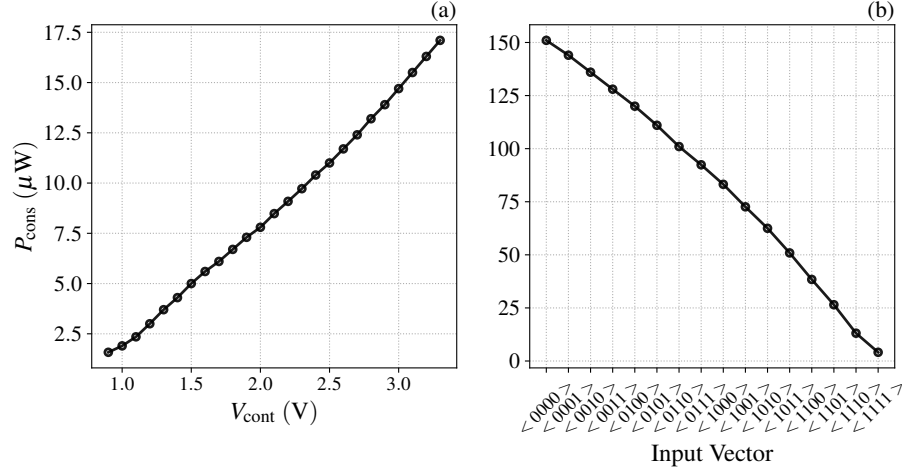


Figure 5.7 Measured power consumption of the proposed (a) THDEVc, and (b) THDEDc

be discharged to $V_{\text{DD}} - V_{\text{thp}}$ lengthens. However, this approach is only practical for providing delay at one edge of the input pulse and not at both rising and falling edges.

At delay amounts of 26 ns and 4.5 μs , the THDEDc prototype consumes a power of 151 μW and 4.1 μW , respectively. Also, the power consumption of the THDEVc is 17.2 μW and 1.58 μW at the delay values of 16 μs and 5 ms, respectively. As can be deduced from Fig. 5.7, the proposed designs dissipate the least amount of power when compared with the prior art delay cells. At 2 ms delay values, the design presented in [84] has a power consumption of 57 nW which is better than the proposed THDEVc power performance (1.9 μW). This property is achieved by a very low bias current of 1 nA. Without an ideal off-chip current source, such a low current reference leads to a significant degradation in delay accuracy. Thus, the performance of the design in [84] is limited when it comes to an integrated solution for controlling current.

In Table 5.2, the temperature and process sensitivity are reported at the maximum achievable delay amount of each delay circuit, which is the worst-case scenario due to the lowest amount of biasing current. In the range of ns, the proposed THDE is more accurate than other delay cells while its performance slightly degrades when the delay is increased to millisecond. Two digitally-controlled delay cells presented in [110] use a controlling current of 95 to 188 μA . Despite the fact that large control current is more resistant to environmental noise, these circuits are unable to achieve high precision because of the inherent disadvantages of the employed inverter-chain configuration. Consequently, the proposed THDEs have a wide range, low power, and high accuracy with a small silicon area and a low sensitivity to temperature drifts. Furthermore, the supply voltage sensitivity (S_V) of the proposed delay cell is less than 10% when operating with a delay range of nanosecond, however, it deteriorates for larger delay amounts.

Table 5.2 Performance summary and comparison of the proposed delay elements with prior-art publications

Reference		Tech. (nm)	Supply (V)	Delay Range	P_{dis}^a (μW)	$S_T^{a,b}$ (ppm/ $^\circ\text{C}$)	Accuracy ^a σ/μ (%)	Area (mm^2)	Architecture
This Work	THDE_{DC}	350	3.3	26 ns - 4.5 μs	4.1	900	2.8	0.0067	Thyristor-based DC
	THDE_{VC}			16 μs - 5 ms	1.58	2710	8.5	0.0056	Thyristor-based VC
Schell et al. [82]		90	1	5 ns - 1 μs	10	N.A	N.A	0.00036	Thyristor-based VC
Esmaeilzadeh et al. [108] ^c		350	3.3	1.5 ns - 19.6 ms	108	1871	51.6 ^e	0.007	Thyristor-based ^f
Saft et al. [84]		350	3.8	4 μs - 22 ms	0.057 ^d	4000 ^d	3.82 ^d	0.006	Thyristor-based ^f
Zhang et al. [80]		350	3.3	4 ns - 16 ns	310	517	N.A	N.A	Thyristor-based VC
Maymandi et al. [110]	type 1	180	1.8	2.05 ns - 2.4 ns	N.A	1081	24 ^e	0.005	Inverter-based DC
	type 2			220 ps - 370 ps		378	12.6 ^e	N.A	Inverter-based DC
Kim et al. [83]		110	0.6	25 ns - 720 ns	N.A	4375	18.6 ^e	N.A	Thyristor-based VC

^aAt max delay, ^b $S_T = \Delta t_d / (t_d \cdot \Delta T)$, ^cSimulation results, ^dAt 2 ms delay, ^eMax deviation/ μ , corner analysis, ^fUsing off-chip current source

5.6 Conclusion

We described in this brief the design and analysis of a compact, high-precision, and wide-tuning range CMOS thyristor-based delay elements. The conventional thyristor-based delay circuit has been improved by minimizing the leakage current at the main circuit nodes and its effect on the delay duration. Additionally, the temperature stability of the design is enhanced by using source degenerated resistors in current-supplying transistor lines, and incorporating two different tunable current source structures with low temperature and process sensitivities. Thus, the proposed delay circuit overcome limitations associated with delay range, power, and temperature. The THDE prototypes were implemented in the AMS 0.35- μm CMOS technology and powered from a 3.3 V supply. The measured overall delay range extended from 26 ns to 5 ms, with a temperature sensitivity ranging from 240 ppm/ $^\circ\text{C}$ to 2710 ppm/ $^\circ\text{C}$, and a power dissipation from 151 μW to 1.58 μW , respectively.

Acknowledgment

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CHAPTER 6 PROTOTYPE IMPLEMENTATION: TIME-BASED READOUT INTERFACE

The following sections provide complementary information regarding the proposed time-based readout interface discussed in CHAPTER 1. This chapter outlines the configuration and operation of this integrated readout circuit based on the proposed circuit designs presented in CHAPTERS 3, 4, and 5. Measurement and post-layout simulation results are also presented to verify the feasibility and performance of the proposed time-based I/O interface for the industrial load switch application.

6.1 Circuit Implementation

In this section, we discuss the system-level design of the target interface as well as the implementation of complementary sub-blocks such as the gate driver, the level shifter, the UVLO, the pulse generator, and the digital control logic.

This circuit has been implemented using a 0.35- μm High-Voltage AMS CMOS technology. It allows the integration of both high-voltage and low-voltage devices on a single chip, with operating voltages of 3.3 V, 5 V, 20 V, 50 V and 120 V. Following the application requirement, the high-voltage sub-blocks of the proposed interface were implemented utilizing 20-V and 50-V transistors to have a higher signal level and be compatible with the 12-V and 28-V needed power supplies. However, for designing the low-voltage sub-blocks, 3.3-V transistors were used to achieve higher speed and lower power consumption. Therefore, level-up/down shifter sub-blocks have been used for changing the voltage level.

The proposed integrated load switch I/O interface comprises three main stages. First, there is a gate driver stage, which is a high-voltage block used for commanding signal adaptation. Second, a readout stage to monitor and validate the real state of the load switch output. Third, a fault detection stage, that internally controls potential errors and disjoints the system if necessary. In the following detailed descriptions, design considerations, and circuit implementations of these stages will be outlined.

6.1.1 Monitoring and Readout Stage

Process monitoring is an essential part of any electronic interface as the sensing nodes are exposed to extreme and unpredictable conditions [113]. This stage connects directly to a sensing element and supplies signal conditioning necessary to obtain an accurate signal for

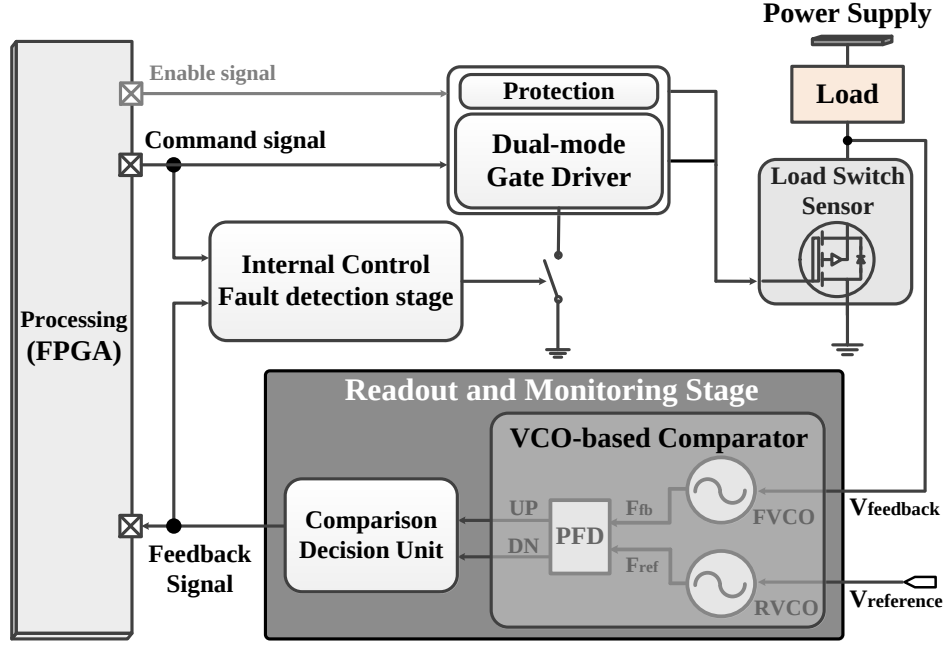


Figure 6.1 Block diagram of the proposed interface with monitoring stage

monitoring and control systems. Fig. 6.1 shows the proposed novel structure which allows adaptive operation of readout circuitry in a load switch application. In this configuration, the monitoring circuit is utilized to form a closed-loop frequency control system in order to readback and process the voltage and current at the load. Thereafter, the processed feedback signal will be sent to the processor (or FPGA). The signal will also be compared with the FPGA command signal (the signal that instructs the load switch to be on or off) through an internal control stage for the purpose of fault detection. In order to meet the readout requirements in the advanced electronic nodes, a time-based circuit technique is used for the design and implementation of the intended load switch interface.

According to Fig. 6.1, in the proposed time-based architecture, the switch information is inserted into the proposed TD-comparator, which is described in Chapter 4. This voltage-domain signal is converted into frequency (or time) information by adopted VCOs, whose structure is discussed in Chapter 3. Then, using the proposed PFD, the frequency-domain outcome is compared to a consistent and distinctive reference frequency. PFD output signals, which represent the frequency and phase difference between the VCO's output, will be inserted into a logic unit to send the appropriate decision signal to the processor and fault detection stage. As a result of the advantageous properties of the proposed comparator, a fully-integrated, low-power, high-speed, and small-area readback and monitoring circuit can be constructed without the use of passive components.

6.1.2 Internal Control and Fault Detection Stage

The other critical consideration in interface circuitry is to recognize the causes of sensor failure in order to mitigate the effects of off-nominal behavior. Sensor faults can be classified into several categories. Typically, a sensor fault can be defined as a deviation from the normal expected outcome in the observed signal without any anomalous conditions affecting the system. It is therefore imperative to establish an internal control stage that evaluates and verifies the feedback signal from the load switch.

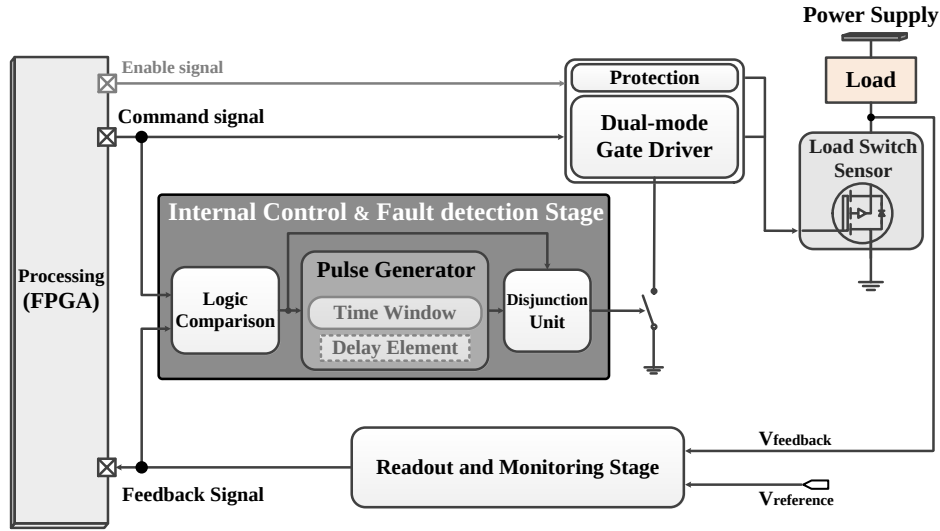


Figure 6.2 Block diagram of the proposed interface with internal control stage

A generic block diagram of the proposed internal fault detection stage with time-based circuitry is presented in Fig. 6.2. Towards achieving integration, we propose a new high-performance digitally-oriented design based on logic block, pulse generator, and delay elements. In this configuration, the readback data from the monitoring stage is compared with the command signal generated by the FPGA. In case of a fault, i.e., an unexpected output, these two signals are in conflict, requiring the internal control stage to trigger an action signal to shut down the entire system and switch off the load. Despite this, the industrial system may be subjected to environmental conditions that could result in unintentional faults. Therefore, the interface should be capable of recognizing actual faults while ignoring unintentional ones [114]. Consequently, an innovative current-controlled pulse generator based on the CMOS thyristor delay element is employed at this stage. The presented pulse generator can produce a stable pulse pattern from either a noisy, digital or analog input signal. Using the proposed wide-range thyristor-based delay elements (THDEs), explained in chapter 5, this design can provide an adequate waiting time window (t_{TW}) for the control stage before

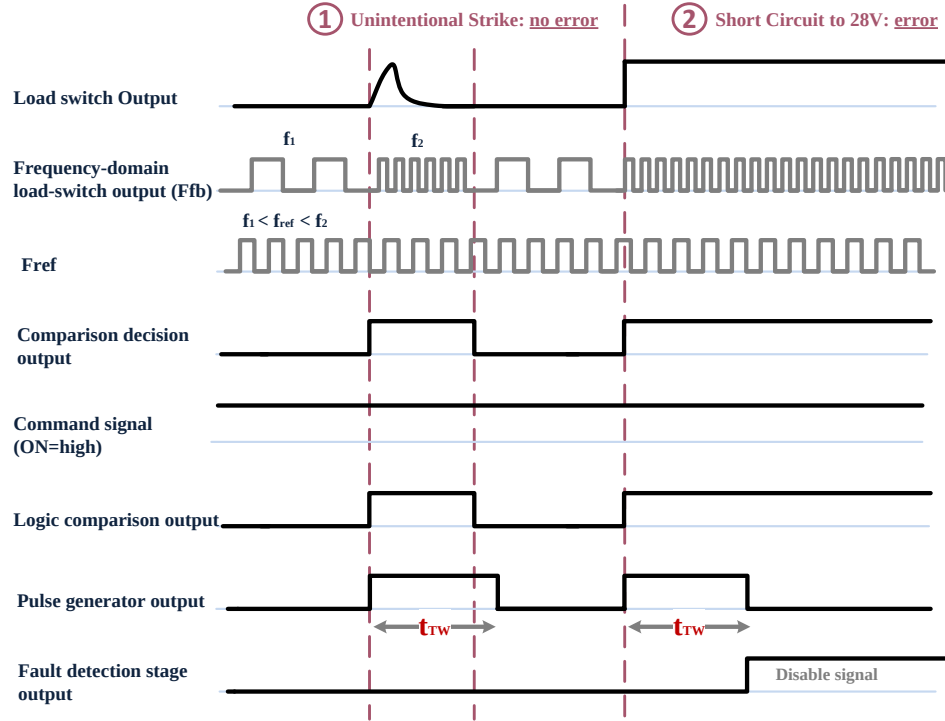


Figure 6.3 Timing diagram of the proposed Monitoring stage and Fault detection stage

it initiates an action. Thus, the system could differentiate an unintentional fault from an actual error. The timing diagram of the proposed monitoring stage and fault detection stage is shown in Fig. 6.3. This diagram illustrates conceptually how each sub-block operates in these two stages. It can be seen that in the event of an unintentional strike, the circuit continues to operate normally, while as a result of a genuine error, e.g. short circuit to VDD, the fault detection stage will send a disable signal to shut down the circuit. By utilizing this architecture, a programmable, high-speed, on-chip fault detection scheme with low power consumption and a small footprint can be realized. The detailed operation of the proposed pulse generator will be described in the following.

Thyristor-based Pulse Generator

A pulse generator can be used as an independent reference input signal source or as part of an integrated interface framework for providing the required control signal. According to our specific application requirement, a practical pulse generator must be duty-cycle tunable and able to deliver accurate pulses with a stable width. Fig. 6.4 illustrates the overall block diagram and schematic of the employed pulse generator. The design has been published in publication #6 listed in section 1.5, which is a peer-reviewed ISCAS conference paper.

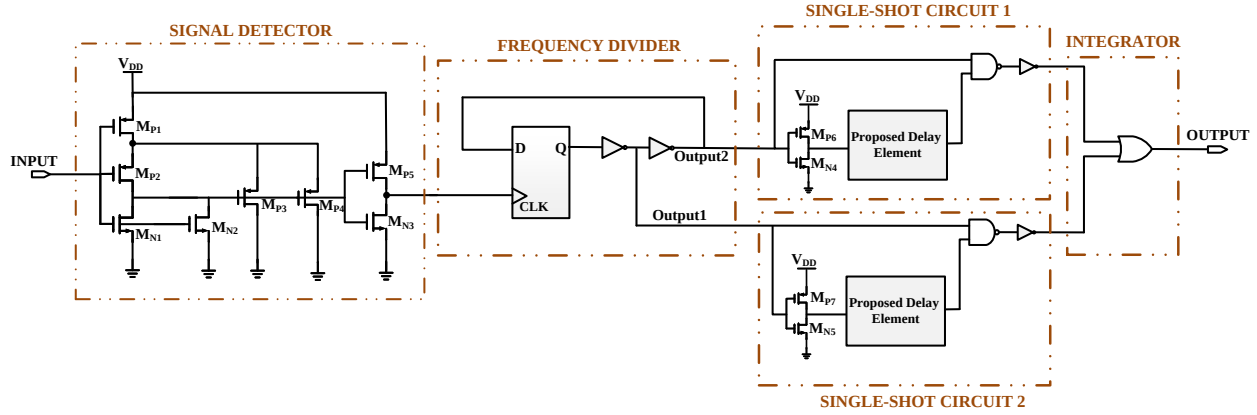


Figure 6.4 Schematic diagram of proposed CMOS thyristor-based pulse generator

At the first step, the signal detector receives the random input, whether it is arbitrary, noisy, or variable, and generates a clean and reliable output signal. Following this, the signal is divided by two using a one-stage frequency divider. The frequency dividing technique has been adopted in the design of a pulse generator to prevent overlapping of the output signals [78]. Next, the combination of two single-shot circuits with time-delay elements yields two positive edge-triggered pulse signals with consistent widths. This block incorporates the proposed CMOS thyristor-based delay cell, which is discussed in chapter 5. In the final step, an integrator circuit provides the output of the pulse generator, which is a pulse train whose width corresponds to the predetermined value of the delay cell time.

As a result of this structure, we are able to develop a fully integrated pulse generator circuit with a wide frequency range, input independent and capable of receiving noisy, random digital or analog inputs. On the other hand, the proposed THDE and its controlling current source realize a duty cycle adjustable square-wave generator. It should also be noted that the use of a low-power delay element directly impacts the energy efficiency and power efficiency of this pulse generator.

Table 6.1 Comparison of pulse generator with reported similar circuits

Reference	[74]	[75]	[76]	[77]	ISCAS'20 [108]	This work
Supply Voltage (V)	5	N.A	2	1.25	3.3	3.3
Technology (nm)	Off-chip	180	90	180	350	350
Minimum Frequency	500 Hz	2 MHz	N.A	N.A	25 Hz	50 Hz
Maximum Frequency (MHz)	0.015	40	0.0505	32.5	331	25 MHz
FoM (mW/MHz)	N.A	0.01	1.412	0.0307	0.0093	0.0072
Area (mm ²)	N.A	0.012	0.0354	N.A	0.018	0.007

Table 6.1 presents the performance summary of the proposed pulse generator and compares

it with recent relevant works. Compared to prior-art structures, the proposed one offers the widest frequency range and the best energy FoM ($= \frac{\text{Power}}{\text{Frequency}}$), which is the average power divided by the operating frequency. Fig. 6.5 illustrates the signals generated from the developed pulse generator. The signal detector receives a noisy analog input waveform and produces a clean pulse signal. Then, the frequency divider splits the initiated signal by factor 2 and generates two non-overlapping lagging and leading signals. According to the desired time delay value, the single shot circuit generates a pulse pattern based on the rising edge of the incoming signal. As a result, the output signals of single-shot circuits are integrated and provide a constant pulse signal as a final output. Based on the simulation scenario, the pulse generator is operated in a manner that takes a series of input triggers and explicitly converts them to uniform output pulses with the same amplitude and time duration of $500 \mu\text{s}$.

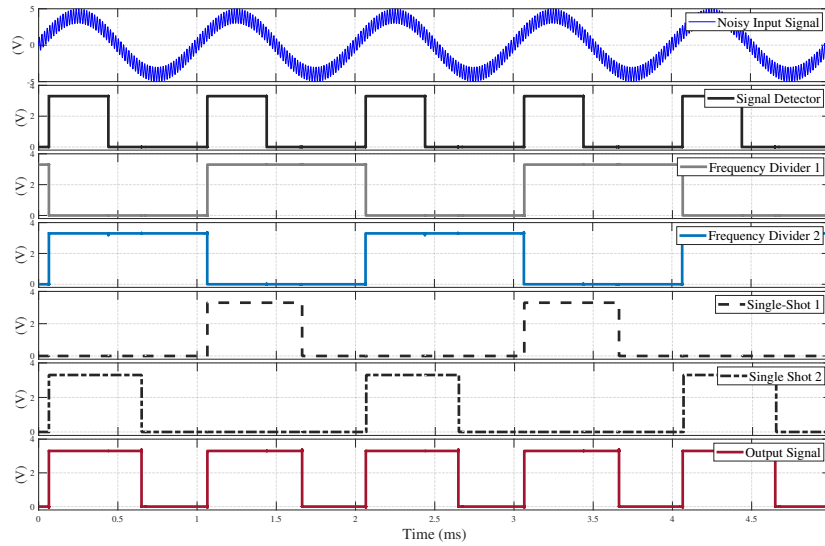


Figure 6.5 Post-layout transient simulation result of the proposed pulse generator

6.1.3 Versatility and Reconfigurability

Industrial I/O interfaces have been known as bulky interfaces. Considering the number of I/O interfaces and the need for redundancy within the industrial system (for safety reasons), these sensor interfaces present a major challenge in reducing the BoM as well as the silicon area over SoC/SiP. Therefore, the concept of versatility and reconfigurability is proposed to optimize the implementation of I/O blocks.

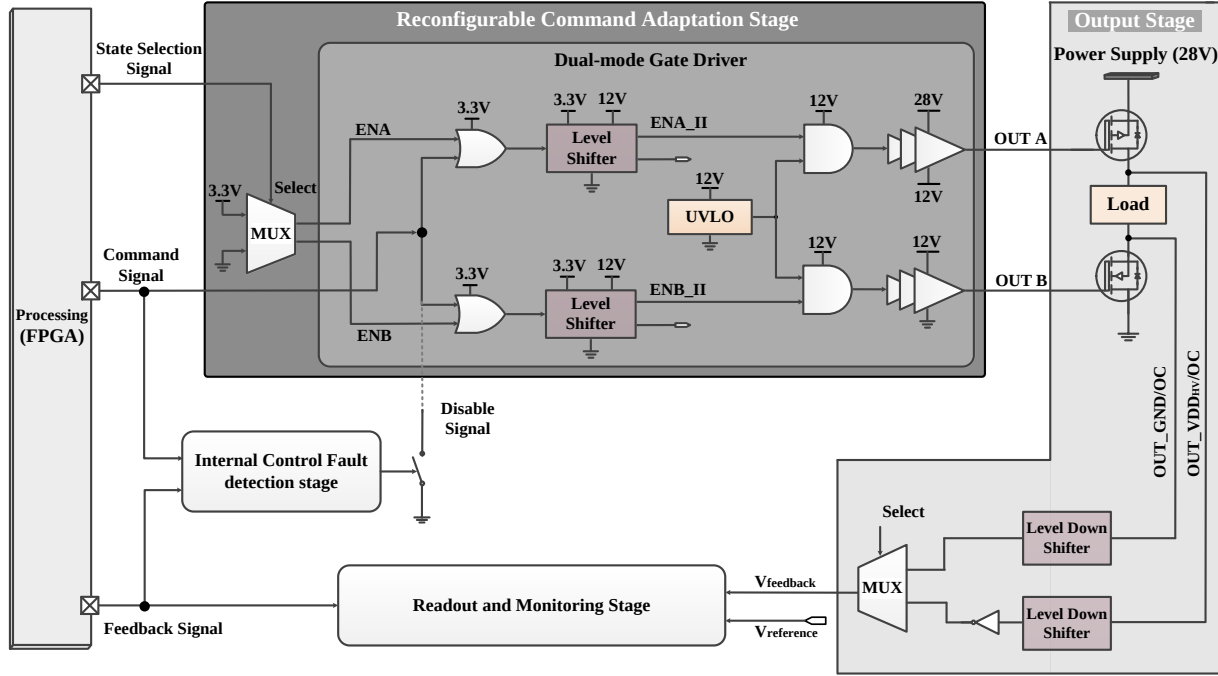
In the target application, the I/O interface essentially needs to operate in two states: VDD_{HV}/OC and GND/OC . When the load switch is located between the local ground and the load, the

output GND/OC interface is in charge of converting the command line into an external output with two possible states which are open circuit (OC) or GND. In the OC state, the load switch is in the off-mode and the external output presents an open circuit, while in the GND state, the load switch is in the on-mode and the output shows the system's ground. To validate the state of the output, the external output, which we refer to as the V_{feedback} in Fig. 6.1, and 6.2, will be inserted into a read-back circuit. Similarly, when the load switch is located between the supply voltage and the load, the output VDD_{HV} /OC interface converts the command line into an external output with two possible states which are OC or $VDD_{\text{HV}} = 28 \text{ V}$. For the OC state (load switch: off-mode), the external output shows an open circuit while for the VDD_{HV} state (load switch: on-mode), the output shows 28 V DC. Like the output interface, the same states are defined for the input interface while the input interface oversees driving a read line from an external input.

Consequently, one of our main objectives is to design a versatile I/O interface that can be reconfigured into both categories VDD_{HV} /OC and GND/OC. To this end, some additional considerations need to be taken into account, such as the design of an adaptable gate driver and the associated circuitry required to support such reconfigurability.

6.1.4 Gate Driver Stage

Fig. 6.6 shows the proposed versatile and reconfigurable interface intended for power load switches that can support different industrial modes of operation. Depending on the industrial demand, a select signal will be generated by the FPGA that determines the state of the interface, which is either VDD_{HV} /OC and GND/OC. A dual-mode gate driver network is employed as an ON/OFF control unit that includes some logic gates, level shifters, buffer chains, and Under Voltage Locked-Out (UVLO) to protect inputs against over/under voltage tolerances. The block diagram of the UVLO, its transient response with respect to VDD variation, and the hysteresis diagram are shown in Fig. 6.7. Fig. 6.8 circuit implementation of the pre-regulator and hysteresis control blocks of UVLO, and the level shifter. The output stage is modified to accommodate two high-voltage power MOSFET switches driving an off-chip load. The level of the load switch's output signal will be adjusted by level-down shifters. Then, one of these outputs will be selected to be sent to the next stage based on the select signal and operation state. As explained, the output result signals will be monitored by means of a readback stage using a time-domain conversion mechanism, and the decision signal will be issued to both the FPGA as feedback and the internal control unit for fault detection. In the event of an error, this unit provides a disable signal and shuts down the system using an isolated NMOS switch.



Truth table describing the logical operation of the command adaptation stage and the output stage

Interface State	Select signal ('1' = 3.3V)	Command ('1' = 3.3V)	ENA ('1' = 3.3V)	ENB ('1' = 3.3V)	OUT A ('0' = 12V)	OUT B ('1' = 12V)	OUT_VDD _{HV} /OC ('1' = 28V)	OUT_GND/OC ('1' = 28V)	V _{feedback} ('1' = 3.3V)
GND/OC	0	1	1	0	0	1	1	0	0
		0	1	0	0	0	1	1	1
VDD _{HV} /OC	1	1	0	1	0	1	1	0	0
		0	0	1	1 (28V)	1	0	0	1

Figure 6.6 Block diagram and truth table of the reconfigurable interface with dual-mode gate driver

6.2 Readout Interface Integration

This section provides the layout and chip designs for integrating the time-based interface components. The chip prototype designed for the fabrication and along with the post-layout simulation results are also discussed to verify the feasibility of the proposed load switch interface.

6.2.1 Core and Chip Design

Fig. 6.9(a) shows the complete layout design of the fully-integrated time-based load switch interface, including the core design, the I/O, and the power pads. Also, the die micrograph of the fabricated chip in 0.35- μm CMOS technology and the PCB board designed for the

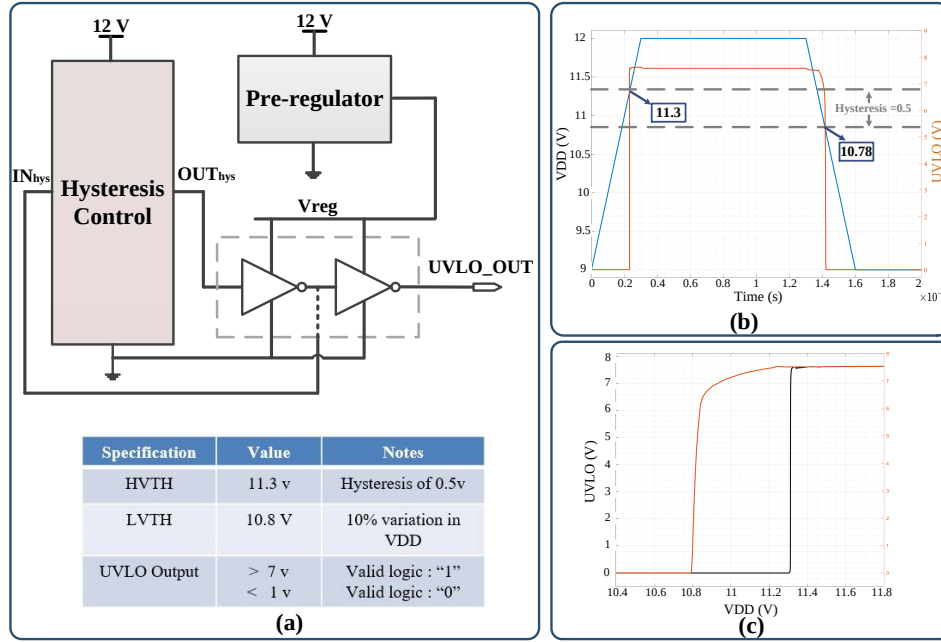


Figure 6.7 The UVLO: (a) block diagram, (b) transient response as result of VDD variation, and (c) hysteresis diagram

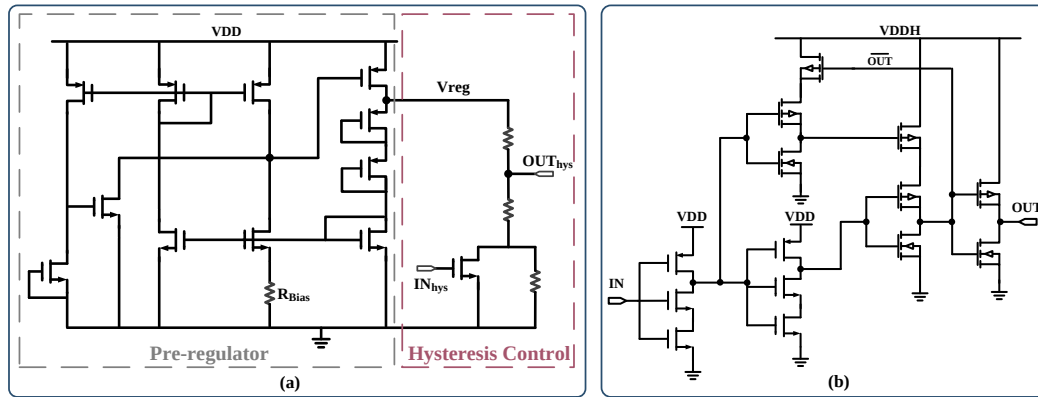


Figure 6.8 The schematic circuit of (a) pre-regulator and hysteresis control sub-blocks of the UVLO, and (b) level shifter

experimental test are shown in Fig. 6.9(b) and Fig. 6.9(c), respectively. The overall dimension of the core design is $650 \mu\text{m} \times 780 \mu\text{m}$; however, the total area without considering the empty area is 0.35 mm^2 . Fig. 6.10 illustrates the breakdown of area where the high-voltage side of the interface, i.e., the gate driver and the output stage occupy the majority of the chip area.

The padding has been assembled using the pad design provided by the technology. The vacant

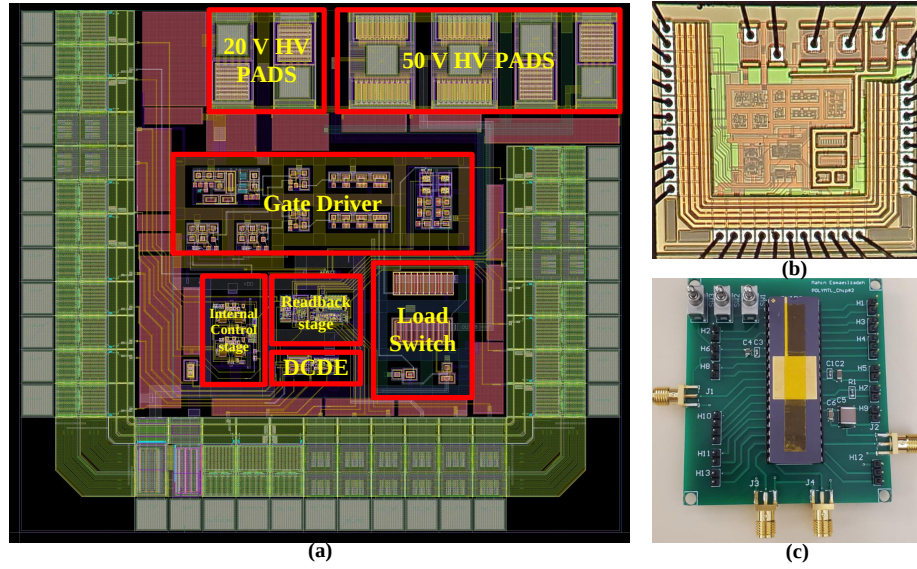


Figure 6.9 Fabrication Run: (a) Chip layout design of the Integrated load switch interface, (b) die micrograph of the fabricated chip, and (c) PCB design for experimental test

space between the IO bond PADs and the core design is filled by decoupling capacitors with the size of 5-25 pF connected between supply voltage nodes and ground. The complete chip dimension considering the padding is $1.54 \text{ mm} \times 1.78 \text{ mm}$. Five chips have been manufactured from this fabrication run and have been tested to evaluate the performance of the overall system.

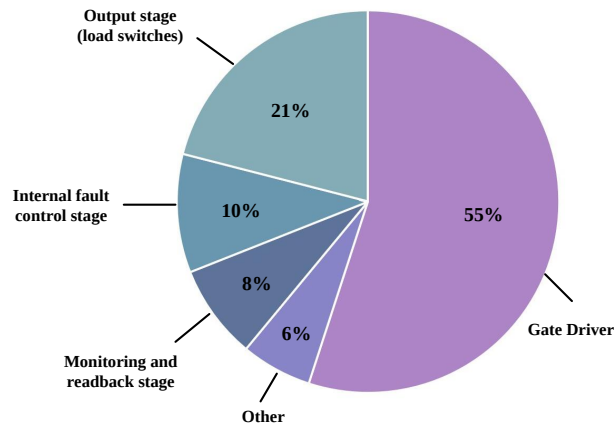


Figure 6.10 Breakdown of area for the proposed load switch interface

6.2.2 Post-layout Simulation and Measurement Results

The post-layout simulation result of the proposed load switch interface is provided in Fig. 6.11. This figure illustrates the detailed logical results of the main nodes in the command adaptation stage and the output stage for both interface states. As shown in the truth table of Fig. 6.6, based on the select signal for configuring the operation state of the interface, the command signal provided by the FPGA will be adapted accordingly for running the output stage.

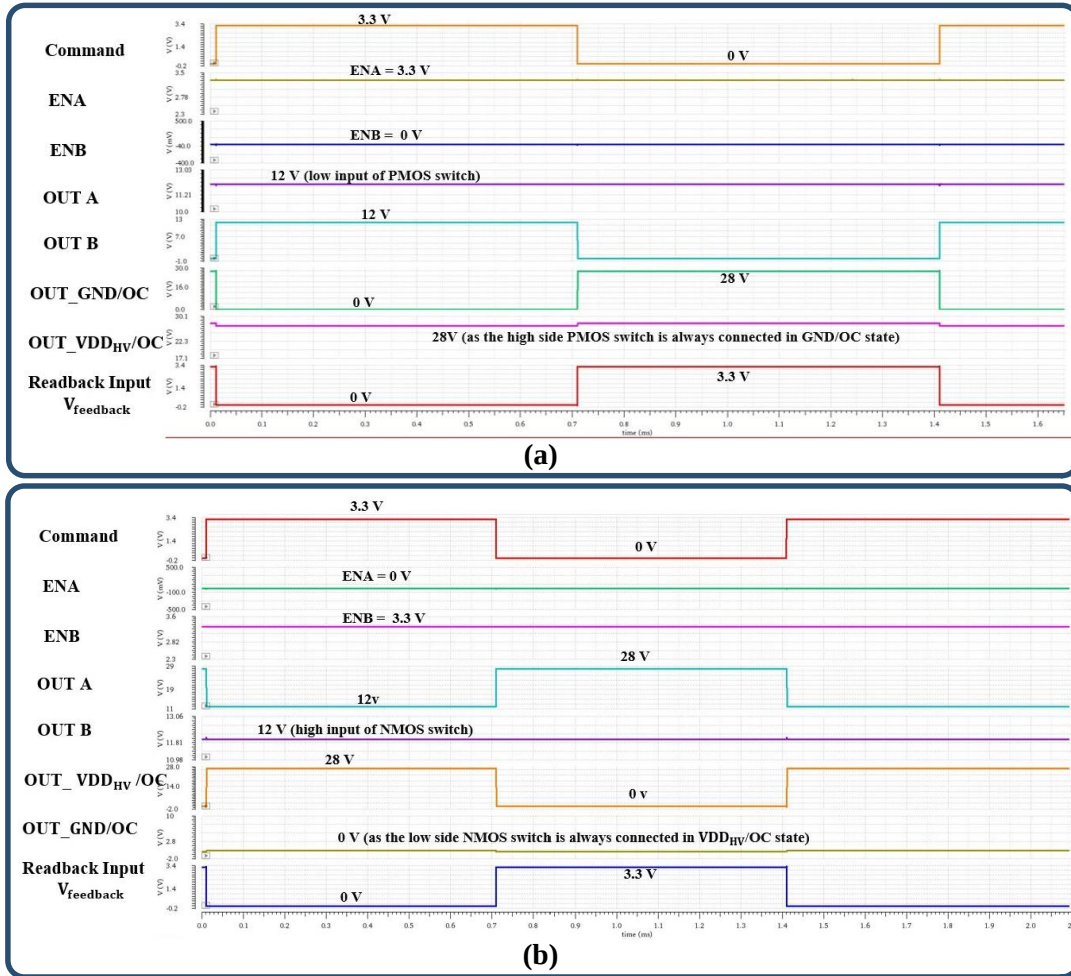


Figure 6.11 Post-layout transient response of the command adaptation (gate driver) and the output stages of the proposed load switch interface operating at (a) GND/OC state, and (b) VDD_{HV}/OC state

The measured transient response of the proposed time-based load switch interface is shown in Fig. 6.12, which demonstrates the functionality of the entire circuit. The combination of

the select signal and the command signal induces the gate driver to provide the appropriate signal to switch on or off the power MOSFET switches. The output of these switches is sent to a readback stage to be monitored and compared with a reference voltage using a time-based VCO-based comparator. The comparison decision will be inserted into the internal control stage and the pulse generator. Finally, in the presence of a fault or error, a controlling signal (disable signal) will be generated which freezes the operation of the entire circuit.

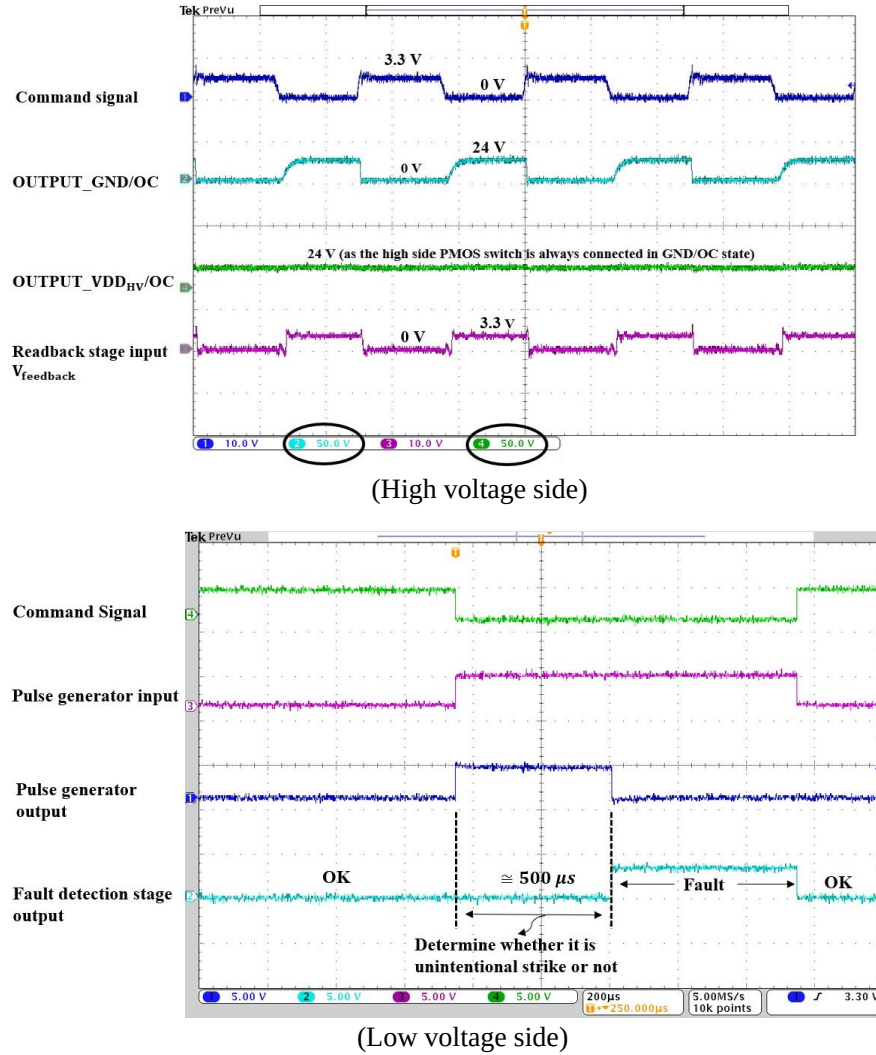


Figure 6.12 Measured transient response of the proposed load switch interface at GND/OC state

CHAPTER 7 GENERAL DISCUSSION

In recent years, time-based circuit mechanisms have become increasingly prevalent in electronic systems. A popular time-domain solution is VCO-based architecture, which enables a highly digital, and effectively scalable configuration. Due to the importance of these circuit techniques in advanced data acquisition systems, several time-based readout interface have been developed. In addition, the effect of sub-blocks on the overall performance of the system was also investigated, revealing the highly dependent relationship between the efficiency of the system and the one of the sub-blocks. Therefore, despite many previous contributions, developing new high-performance time-based circuit designs could lead to significant advances.

The main purpose of this thesis is analysis, characterization, designing, and validation of several time-based structures that considerably contribute to the overall performance of readout interfaces. These circuit elements have been implemented and fabricated in three tape-out runs of AMS-0.35 μm CMOS technology. For each of these fabrication runs, five chips were available to measure the performance of the proposed circuits. It was observed in the literature review that the VCO's nonlinearity and phase noise characteristics limit the performance of VCO-based sensor interfaces. This led us to propose a VCO architecture with improved linearity and low phase noise. An analytical model is derived in CHAPTER 3, providing closed-form expressions for the phase noise of the VCO. Based upon the proposed analysis, contributing noise sources and the phase noise limitations can be estimated. According to the state-variable MATLAB[®]/SIMULINK model of a time-based interface presented in CHAPTER 3, the low phase noise performance of the proposed VCO, -147.57 dBc/Hz at 1 MHz offset frequency, and the moderate constant gain of 4.7 MHz/V makes it a viable candidate for high-performance DC sensing applications. This stems from the fact that at a given input bandwidth and VCO gain, the phase noise performance of the VCO strongly limits the SNR of the system.

As shown in CHAPTER 2, a comparator can be used to readout the sensor data by comparing the input signal to a reference signal and generating a binary digital result. In view of the desired digital-oriented scheme, it has been demonstrated that TD-comparators offer a more energy efficient and scalable alternative to voltage-domain comparators, allowing higher time resolution. Since they are critical components of any readout circuit, they have received extensive attention and various contributions have been made to these recent attractive designs. For V2T conversion, it has been shown that VCOs are more advantageous than

VCDLs due to its inherent noise adaptation performance. However, the VCO is not the only effective building block of a TD-comparator. The PFD behavior, which is responsible for detecting and comparing the converted time/frequency information, has an additional influence on the performance of TD-comparators, which has been overlooked in the literature to the best of our knowledge. A fully practical PFD must be capable of detecting any frequency and phase differences between incoming inputs. However, the DZ and BZ are the main imperfections in the phase characteristics of the PFD, as their presence results in the PFD's incapacity to function when the phase differences of the input pulses are near zero or nearly 2π . Theoretical analysis in CHAPTER 4 shows that this shortcoming in a TD-comparison has several consequences, including lengthening the comparison time, degrading the IRO, limiting the resolution, and increasing the energy consumption. This is due to the fact that when the input phase difference is within these zones, the oscillation needs to continue until the $\Delta\phi$ gets out of the DZ or BZ, which results in a longer comparison time and greater power dissipation.

Having a high resolution and high speed readout interface requires a comparator with adequate performance in terms of offset, comparison time, and noise. To this end, we propose a VCO-based TD-comparator in CHAPTER 4 that overcomes the limitations of the prior art by employing two identical linear low phase noise VCOs (proposed in CHAPTER 3) and a low-noise PFD, with minimal DZ or BZ, free of glitches and unwanted one-shot pulses. Thanks to these exceptional characteristics, the proposed comparator achieved the minimum offset, the best normalized speed, comparable normalized energy and IRN, and high resolution without sacrificing comparison time, compared to prior-art recent TD-comparators.

An industrial I/O interface for a load switch platform is used to evaluate the capabilities of the proposed novel architectures. This application requires an interface to control a power supply switch of a load. Monitoring and processing the state of this power management switch is essential to provide a reliable signal that can be interpreted by a specific controller. However, load switch output voltage levels of '0' and '1' do not have a strict definition, as the output result may change during transmission. As a result, the proposed high-precision VCO-based comparator is a promising solution that can accurately read any state changes in the switch and translate them into an appropriate binary output signal for the controller or processor. As discussed in CHAPTER 6, this design not only enables the integrated implementation of the conventional discrete approach, but also provides several improvements to the readout circuit. There is, for example, a low power consumption due to the DZ mitigation and oscillation-adjustment provided by a control unit within the comparator circuit that disables the V2T conversions at the end of a comparison. High resolution operation can be achieved since any small difference between the feedback signal from the load switch and the fixed

reference signal can be read with an accuracy of $10\ \mu\text{V}$ in less than 700 ns conversion time.

Aside from monitoring the output of the load switch, it is imperative to detect the vulnerability of the load switch network to ambient hazards and any real or temporary system failures, which, based upon our review, has not been considered in the previous load switch schemes. Therefore, in the second part of this thesis, we suggest a compact, adjustable and robust fault control design capable of detecting discrepancies between the readback result signal and the command signal. The proposed circuit comprises a square-wave generator with a constant pulse-width presented in CHAPTER 6, a tunable delay element, and some logic gates. This method is advantageous due to its compact and simple architecture as well as the ability to distinguish between inadvertent and actual errors by providing a timing window through a predetermined delay value. The outcome of this stage is a disabling signal that ceases the operation of the entire system in the occurrence of an error. It is therefore necessary for it to be resilient against fluctuations in temperature and process. Towards this end, as shown in CHAPTER 5, an accurate model of a current-controlled delay cell based on CMOS thyristor is proposed. The temperature and process sensitivities of this DE are improved by reducing subthreshold currents, utilizing source degeneration resistors on-chip, and employing two different current sources that provide a range of current control while offering a low sensitivity to process and temperature variations.

Finally, the proposed SoC-based I/O interface IC is complemented by means of a driving path that enables communication between the processor and the load switch device by adapting the command signal. There are several degrees of reconfigurability built into this interface circuit; the specific configuration of the gate driver and the output stage of the load switch allows for a versatile scheme that is compatible with both modes of operation of the target industrial load switch system. In addition, the employed THDE can be programmed with a control analog or digital input in order to provide a desired timing delay by adjusting the duty cycle of the pulse generator. Furthermore, the operation of closed-loop VCO-based comparators implies an inherent adaptation to noise, since noise scales down with increasing NOCs. Having a certain freedom in the number of delay stages in the VCOs and the DZ of the PFD, we are able to tailor the comparator's characteristics, such as noise, speed, and power, with the minimum level of complexity, according to the target application.

As a consequence, it is worth noting that the proposed time-based circuit techniques are robust solutions with the highest integration, and wide dynamic range that can be adopted into other types of time-based sensor interfaces. Besides, the design of these high-precision, low power, low noise architectures is extensible and applicable to any feasible electronic circuit combinations.

CHAPTER 8 CONCLUSION AND RECOMMENDATIONS

In this chapter, we provide a summary of the major contributions, achievements, and publications originating from this thesis. Additionally, complementary considerations and methods are suggested for future work to develop a high-performance time-domain circuits suitable for advanced readout interfaces.

8.1 Summary of Works and Contributions

This thesis presents the design of a fully integrated high-precision time-based readout interface, based on a time-domain conversion mechanism, intended to be used in an industrial power electronic application. Time-based architecture has been applied to a load switch interface for the first time, which provides great flexibility in terms of integration, power consumption, technology scalability, and speed.

The circuit imperfections of each component can adversely affect the overall readout interface specifications; therefore, it is imperative to determine and alleviate them. In this work, several prototypes, including the improved proposed time-based circuits, were implemented in AMS 0.35- μm CMOS technology. As a fundamental building block of the interface, the design and analysis of a single-ended, low-noise, wide-tuning range ring VCO has been presented. The measured oscillation frequency shows a linear range from 0.01 to 9.37 MHz, representing a 199.5% frequency tuning range over a 2-V control voltage. At maximum frequency, the measured phase noise is -147.57 dBc/Hz at a 1 MHz offset frequency, while the power consumption is 0.9 mW with a silicon area of 0.005 mm². Moreover, we have discussed the impact of low phase noise VCOs on the performance of a PLL-based sensor interface using a MATLAB/SIMULINK model.

The proposed VCO has been adapted into a novel TD-comparator, where input and reference voltages are digitized into pulse signals containing frequency-domain information by using two identical VCOs. Following the pseudo-differential configuration of VCOs, there is a PFD which compares the duration of incoming pulses and a control unit that disables the TD comparator when the comparison decision has been made in order to prevent any further power consumption. The proposed PFD exhibits glitch-free low phase noise and low power characteristics. The innovative circuit configuration of this inventive PFD minimizes the reset process and accelerates the pre-charge of the internal nodes, leading to a linear ϕ -V characteristics from almost -2π to 2π , with a measured minimal DZ and BZ of 12 and

22.7 ps, respectively. Due to the fact that the proposed glitch-free PFD provides superior performance in terms of area, power, DZ/BZ, phase range, and noise, it is noteworthy that it is not only applicable to TD-comparator applications, but also to PLLs, DLLs, and CDRs.

In particular, we focused on the key trade-offs in designing the TD-comparator. The impact of the PFD's DZ and BZ, as well as the effect of the VCO's number of delay stages, phase noise, and number of oscillation cycles on the overall performance of the comparator are fully addressed. To the best of our knowledge, this is the first time that the performance of a TD-comparator is thoroughly examined with respect to its PFD characteristics. Several analytical models have been developed for different parameters of the comparator. Specifically, derivations of resolution and comparison time illustrate how the DZ and input voltage differences can affect the comparison time, which mainly determines clock frequency, sampling rate, and convergence speed in data conversion applications. As the oscillation of VCOs continues as long as the time difference between their outputs remains within the DZ, this study suggests that adopting a minimal DZ PFD can reduce the IRO, the energy per conversion, and resolving times of the comparator. Usually, calibration techniques are used to optimize the offset performance of the comparator. However, using more accurate circuitry when designing sub-blocks relaxes the requirement of the complex calibration techniques. The presented TD-comparator architecture benefits from the supreme advantages of the proposed VCO and PFD to attain an IRN of $148 \mu V_{\text{rms}}$ and an IRO standard deviation of $81.14 \mu V$. It dissipates $93.65 \mu W$ at a conversion rate of 2.7 MHz under a 3.3-V supply voltage while occupying 0.01 mm^2 active area.

The proposed comparator is used to configure a high-precision readback circuit in a load switch interface, where a monitoring circuit is employed to configure a closed loop feedback mechanism in order to receive and process load voltage/current information. Furthermore, this thesis includes another essential component of industrial I/O interfaces, namely an internal fault detection stage. The purpose of this internal control circuit is to secure the system by evaluating the result signal of the monitoring stage against the main command signal and to ignore temporary errors that are due to short-term incidents. The specifications of this stage are achieved through the design of an adjustable pulse generator based on a proposed CMOS thyristor-based delay element (THDE). This tunable delay cell allows the square wave generator to control the pulse width with minimal energy consumption in the system. Post-layout simulation results demonstrate that a stable constant output pulse width can be achieved while the fall-time of the generated pulse can be varied by adjusting the control current of the delay element. The proposed THDE features a small area, high-precision, and wide tuning range, which has been improved by minimizing the impact sub-threshold leakage current at the main circuit nodes. The temperature stability of the

design is further enhanced by the use of source degenerated resistors in current-supplying transistor lines as well as the incorporation of two different tunable current sources with low temperature and process sensitivities. The measured overall delay ranges from 26 ns to 5 ms, with a temperature sensitivity of 240 ppm/°C to 2710 ppm/°C, and a power dissipation from 151 μ W to 1.58 μ W, respectively. The suggested current-controlled pulse generator comprising the proposed THDE can operate within a frequency range of 50 Hz to 25 MHz with a power consumption of 1.5 to 181 μ W, respectively.

For completeness, the load switch I/O interface structure is equipped with a dual-mode gate driver and an output stage. These blocks are configured in a manner that is compatible with the different requirements of industrial operation states. Consequently, the proposed load switch interface provides exceptional characteristics such as integration, reconfigurability, versatility, and time-based implementation for its readout and control circuits. Moreover, as a result of the proposed architecture, the traditional bulky discrete configuration of the load switch system has been eliminated, and the SWaP-C qualification, which is highly desirable in an industrial application because of the large number of I/O modules, has been achieved.

It is worth mentioning that the proposed circuits are not designed for use exclusively in a load switch interface, since some simpler designs with less demanding characteristics might be adequate in this case. The results of this research led to the development of a common interface circuitry for DC sensing applications, as well as circuit-level enhancements to the fundamental building blocks. The supreme advantages of the proposed time-domain designs make them compatible with a variety of other readout interfaces as well.

8.2 Future Research

Toward the improvement of the objectives achieved in this thesis, some recommendations are presented for future research.

The proposed structures have been designed, fabricated, and tested in a 350-nm CMOS process which is a relatively old technology with a high supply voltage of 3.3 V. Usually, time-domain circuits are considered to be advantageous with low supply voltages in advanced processes. Despite the fact that the long channel node and the high supply voltage result in lower circuit noise and larger output swings, they are incompatible with the time-based techniques criteria regarding area and power consumption. Therefore, advanced scaled-down technology may provide more flexibility when implementing the proposed time-based circuits and evaluating their enhanced performance.

It is likely that the same architecture in a more scaled node would suffer from VCO's phase

noise degradation, mainly due to a smaller voltage swing. However, the operation of closed-loop VCO-based comparators implies an inherent trade-off with respect to noise, as the noise scales down with an increasing number of oscillation cycles (NOCs), and it is referred to as self-scalability of comparator noise. VCOs' outputs overcome the jitter effect as the NOC increases depending on the ΔV_{in} input. As a result, in advanced technology, the number of delay stages in VCOs and the amount of the PFD's DZ, which allow adaptive configuration of the comparator noise, can be adjusted in order to achieve optimal noise performance for the system at the cost of speed and power consumption.

In a closed-loop time-based comparator, the common-mode and supply noise sensitivities of a single-ended VCO can be reduced by taking proper layout design considerations and placing two identical oscillators close together to make noise appear as a common mode perturbation on oscillation frequencies. The reduction in device size, however, may make the matching and layout design more challenging. Therefore, the use of a differential ring VCO could mitigate the degradation of comparator noise in advanced technologies since it offers better common-mode noise rejection and lower sensitivity to substrate and supply noise. It is important to note that the phase noise performance of this device has to be optimized by minimizing the tail current noise.

The major power and area consuming block of the proposed TD-comparator is the VCO. Thus, a low power version of the proposed ring-VCO described in publication #4, i.e., the peer-reviewed NEWCAS conference paper, might improve power performance at the expense of weakening robustness and phase noise.

A current-limiting circuit is another critical requirement of a load switch platform that is not addressed in this thesis. The load switch's output current needs to be limited to a safe value (5 A in the target industrial application) by the current limitation circuit. This requirement may be met by combining a resistor sensing protection scheme with the proposed fault detection stage.

Interestingly, the proposed time-based circuit techniques can be used to design and fabricate a general PLL-based sensor interface that has the greatest similarity to the proposed readback circuit. A resistive-bridge sensor can be utilized as a sensing element, while a multi-bit implementation of the PFD and DAC in a feedback loop must be designed.

Some circuit-level considerations might use in the future work to improve the proposed architectures. For instance, a rail to rail input swing configuration for the VCO, design of a temperature variation independent band-gap reference for the delay cell tuning. Also, the proposed pulse generator incorporating the improved temperature compensated THDE can be tested after fabrication to access the measurement results.

8.3 Publications

1. M. Esmailzadeh, M. Ali, A. Hassan, M. Nabavi, B. Gosselin and M. Sawan, "A Tunable CMOS Thyristor-Based Pulse Generator for Integrated Sensor Interface Applications," 2020 IEEE International Symposium on Circuits and Systems (ISCAS), 2020, pp. 1-5, doi: 10.1109/ISCAS45731.2020.9180572.
2. M. Esmailzadeh, M. Ali, A. Hassan, Y. Audet and M. Sawan, "Low-Power High-Accuracy VCO-Based Comparator for Sensor Interface Applications," 2020 18th IEEE International New Circuits and Systems Conference (NEWCAS), 2020, pp. 254-258, doi: 10.1109/NEWCAS49341.2020.9159801.
3. Mahin Esmailzadeh, Yves Audet, and Mohamad Sawan, "TIME-DOMAIN COMPARATOR AND PHASE FREQUENCY DETECTOR," U.S. Patent, No. US 63/228,245, 2 Aug 2021.
4. M. Esmailzadeh, Y. Audet, M. Ali and M. Sawan, "A Low-Phase-Noise CMOS Ring Voltage-Controlled Oscillator Intended for Time-Based Sensor Interfaces," in IEEE Access, vol. 10, pp. 101186-101197, 2022, doi: 10.1109/ACCESS.2022.3208273.
5. M. Esmailzadeh, Y. Audet, M. Ali and M. Sawan, "A Low-offset VCO-based Time-domain Comparator Using a Phase Frequency Detector with Reduced Dead and Blind Zones," in IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, Early Access, doi: 10.1109/TCSI.2022.3227802.
6. M. Esmailzadeh, Y. Audet, M. Ali and M. Sawan, "A Wide-range Low-power Thyristor-based Delay Element with Improved Temperature Sensitivity," in IEEE Transactions on Circuits and Systems II: Express Briefs, 2023, Early Access, doi: 10.1109/TC-SII.2023.3245562.

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