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**POLYTECHNIQUE MONTRÉAL**
affiliée à l'Université de Montréal

# High signal-to-noise ratio successive approximation analog to digital converters

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Thèse présentée en vue de l'obtention du diplôme de *Philosophiæ Doctor*
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**POLYTECHNIQUE MONTRÉAL**
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Cette thèse intitulée :

**High signal-to-noise ratio successive approximation analog to digital converters**

présentée par **Masoume AKBARI**
en vue de l'obtention du diplôme de *Philosophiæ Doctor*
a été dûment acceptée par le jury d'examen constitué de :

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## DEDICATION

*To my Mother, in loving memory of my Father,*
*To my Family...*

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# RÉSUMÉ

Les systèmes d'acquisition de données nécessitent des convertisseurs anaologique numérique (CAN) multicanaux, offrant de hautes performances et des larges bandes passantes. Ces besoins ont abouti à la conception de structures hybrides. Les CAN à registre d'approximations successives avec mise en forme du bruit (NS-SAR) ont montré des performances très intéressantes en termes d'énergie/surface en combinant les avantages des CAN à registre d'approximations successives et ceux à modulateurs delta-sigma ($\Delta\Sigma$Ms). Étant compatibles avec de haut niveau d'intégration technologique, les CAN NS-SAR resteront une solution prometteuse dans l'avenir. Améliorer les performances des CAN NS-SAR sans augmenter la complexité de la conception des circuits et des techniques d'étalonnage est une exigence primordiale. D'autre part, les CAN incrémentiels hybrides (IADC) à partage de matériel et multi-étapes ont présenté les meilleures performances pour les applications multicanaux en ajoutant plusieurs avantages aux $\Delta\Sigma$Ms. Les principaux facteurs qui limitent l'efficacité des IADC sont la bande passante étroite, la grande consommation d'énergie des intégrateurs basés sur l'amplificateur à transimpédance (OTA) des quantificateurs à plusieurs bits, le taux élevé de suréchantillonnage (OSR) et la complexité des architectures hybrides.

Cette thèse contribue à ce sujet en proposant deux architectures de CAN basées sur des CAN NS-SAR. Premièrement, l'architecture de mise en forme du bruit à plusieurs étages (MASH) améliore l'ordre de mise en forme du bruit (NS) des CAN NS-SAR, en ajoutant une deuxième étape avec des exigences de conception assouplies et, sans excès significatif de complexité et de consommation d'énergie supplémentaires. Ce CAN est implémenté en technologie ST-28nm FD-SOI, réalisant une opération de NS de quatrième ordre avec un rapport signal sur bruit et sur distorsion (SNDR) de 75 dB et un taux de suréchantillonnage (OSR) de 10 avec une bande passante de 100 kHz. Deuxièmement, l'utilisation de la structure MASH NS-SAR proposée dans un mode incrémental en deux étapes augmente l'ordre de NS à six et atteint une résolution adéquate pour un système d'acquisition de données multicanal combinant les avantages des IADC multi-étapes, le CAN NS-SAR et la topologie MASH. Les structures proposées dans cette thèse sont caractérisées par un OSR requis plus faible, des quantificateurs SAR à faible puissance et un retour d'erreur (EF) basé sur un amplificateur à faible gain au lieu de filtres à boucle d'intégration en cascade (CIFF) basés sur des OTA de haute performance. Une simulation à l'aide d'un macro-modèle dans Cadence Spectre® a été réalisée pour vérifier l'idée proposée. De plus, des simulations basées sur SIMULINK®, modélisant les imperfections des circuits, et les équations analytiques dérivées prédisent les performances ainsi que la consommation d'énergie de l'architecture proposée.

# ABSTRACT

High channel-density data acquisition systems require high-performance and wide-bandwidth multi-channel analog to digital converters (ADCs). This demand resulted in an approach to designing hybrid structures. Noise-shaping successive approximation register (NS-SAR) ADCs have shown power/area-efficient performance combining the advantages of SAR ADCs and delta-sigma ($\Delta\Sigma$) modulators. Being technology scaling friendly, NS-SAR ADCs will remain a promising solution in the future. Improving the performance of NS-SAR ADCs without increasing the complexity of circuit design and calibration methods is a crucial requirement. On the other hand, multi-step hardware-sharing hybrid incremental ADCs (IADCs) have presented the best performance for the multi-channel applications, adding several advantages to $\Delta\Sigma$Ms. Narrow bandwidth, high power consumption of the operational transconductance amplifiers (OTA)-based integrators and multi-bit quantizers, high oversampling ratio (OSR), and complex hybrid architectures limit the efficiency of IADCs.

This thesis contributes to this topic by proposing two ADC structures based on NS-SAR ADCs. First, multi-stage noise-shaping (MASH) architecture enhances the NS order of NS-SAR ADCs, adding a second stage with relaxed design requirements without significant additional complexity and power consumption. This ADC is implemented in ST-28nm fully depleted silicon-on-insulator (FD-SOI) technology, achieving a fourth-order NS operation with an signal-to-noise-and-distortion-ratio (SNDR) of 75 dB and OSR of 10 at a bandwidth of 100 kHz. Second, using the proposed MASH NS-SAR structure in a two-step incremental mode augments the NS order to six and achieves a resolution suitable for the multi-channel data acquisition system combining advantages of multi-step IADCs, NS-SAR ADCs, and MASH topology. Lower required OSR, low-power SAR quantizers, and low-gain amplifier-based error feedback (EF) instead of OTA-based cascaded integrator feedforward (CIFF) loop filters address the limitations of hybrid multi-step IADCs. A macro-model simulation in Cadence Spectre® was performed to verify the proposed idea. Furthermore, SIMULINK-based simulations, modeling the circuit imperfections and the derived analytical equations, predict the proposed architecture's performance and power consumption.

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# LIST OF SYMBOLS AND ABBREVIATIONS

| | |
|---|---|
| ADC | Analog-to-Digital Converter |
| CaNS | Cascaded Noise Shaping |
| CC | Common Centroid |
| CCP | Cross-coupled Pair |
| CDAC | Capacitive Digital-to-Analog Converter |
| CDS | Correlative Double Sampling |
| CIFF | Cascaded-Integrator Feed-Forward |
| CMOS | Complementary Metal-Oxide-Semiconductor |
| CRFF | Cascade-of-Resonators Feed-Forward |
| DAC | Digital-to-Analog Converter |
| D-Amp | Dynamic Amplifier |
| DCL | Digital Cancellation Logic |
| DEM | Dynamic Element Matching |
| DNL | Differential Non-linearity |
| DP | Differential Pair |
| DR | Dynamic Range |
| DSM | Delta-Sigma Modulator |
| DWA | Data Weighted Averaging |
| EF | Error Feedback |
| ENOB | Effective Number of Bits |
| FD-SOI | Fully Depleted Silicon on Insulator |
| FIA | Floating Inverter Amplifier |
| FIDA | Floating Inverter Dynamic Amplifier |
| FIR | Finite Impulse Response |
| FoM | Figure-of-Merits |
| FPNS | Fully Passive Noise Shaping |
| FRC | Feedforward Residue Compensation |
| FS | Full Scale |
| IADC | Incremental Analog-to-Digital Converter |
| INL | Integral Non-linearity |
| IO | Input/Output |
| LSB | Least Significant Bit |
| LVT | Low Threshold Voltage |

| | |
|---|---|
| MASH | Multistage Noise Shaping |
| NNR | Noise-shaping Noise Reduction Ratio |
| NS-SAR | Noise Shaping Successive Approximation Register |
| NTF | Noise Transfer Function |
| OA | Op-amp |
| OSR | Oversampling Ratio |
| OTA | Operational Transconductance Amplifier |
| PSD | Power Spectral Density |
| PVT | Process, Voltage, and Temperature |
| RVT | Regular Threshold Voltage |
| SAR | Successive Approximation Register |
| SFDR | Spurious-Free Dynamic Range |
| SMASH | Sturdy Multistage Noise Shaping |
| SNC | Sampling $kT/C$ Noise Cancellation |
| SNR | Signal-to-Noise Ratio |
| SNDR | Signal-to-Noise-and-Distortion Ratio |
| SQNR | Signal-to-Quantization Noise Ratio |
| STF | Signal Transfer Function |
| TI | Time Interleaved |

# LIST OF APPENDICES

# CHAPTER 1 INTRODUCTION

## 1.1 Motivation

Nowadays, there is increasing interest in multi-channel analog-to-digital converters (ADCs) for high-channel density data-acquisition systems. Multiplexing offers significant power, size, and cost savings using fewer ADCs per system. Instrumentation applications, such as portable lab equipment [1], wearable [2], implantable systems, and smart sensors for internet of things (IoT) applications [3], require ADCs with high accuracy, bandwidth, and linearity. However, power-hungry components with rigid specifications are required to design high-performance structures, which reduce the power-efficiency of ADCs, especially for battery-powered applications [4, 5]. Such requirements are not easily satisfied with conventional ADCs because of the speed-resolution-power trade-offs. Therefore, this thesis proposes two new architectures combining the advantages of different types of ADCs to relax these trade-offs. Also, a power-bound analysis is proposed to estimate the performance of these hybrid structures.

## 1.2 Problem Statement

The Schrier figure-of-merit ($FoM_S$)[1] of various published solutions is summarized in Fig. 1.1 to study noise-shaping SAR (NS-SAR) ADCs efficiency. Three classes of ADCs, i.e., NS-SAR ADCs, delta-sigma modulators ($\Delta\Sigma$Ms), and incremental $\Delta\Sigma$Ms are considered. In this study, ADCs published at the International Solid-State Circuits Conference (ISSCC), the VLSI Circuit Symposium, and the Journal of Solid-State Circuits (JSSC) from 2010 to 2020 are considered [6]. As depicted in Fig. 1.1(a), for the FoMs better than 175 dB, NS-SAR ADCs show a promising performance regarding the larger Nyquist bandwidth, while the FoMs of the $\Delta\Sigma$Ms are mainly distributed below 170 dB. Figure 1.1(b) shows that the NS-SAR ADCs interestingly provide a better FoM at lower oversampling ratio (OSR) values. Since they offer a multi-bit quantization using a SAR ADC, lower OSR could be employed to meet the dynamic range (DR) requirements. On the other hand, larger required OSR values for $\Delta\Sigma$Ms and incremental $\Delta\Sigma$Ms limit their achieved bandwidth. In terms of footprint, as illustrated in Fig. 1.1(c), utilizing NS-SAR ADCs seems to be a relatively inexpensive solution. NS-SAR ADCs, compared to two other types of ADCs, i.e., $\Delta\Sigma$Ms and incremental ADCs (IADCs), appear to be a technology scaling-friendly approach, as

[1] $FoM_s = SNDR + 10log(\frac{Bandwidth}{Power})$

observed in Fig. 1.1(d). As the digital part of the NS-SAR ADC can be implemented in a low supply voltage domain, NS-SAR ADCs offer better FoMs at lower power consumption, as illustrated in Fig. 1.1(e). According to Fig. 1.1(f), NS-SAR ADCs have not presented a promising signal-to-noise-and-distortion-ratio (SNDR) yet. However, they achieve acceptable FoMs when it comes to other mentioned factors. The limited achieved SNDR is mainly because of the following reasons; 1) higher-order NS-SAR ADCs with boosted SNDR have not comprehensively been studied yet, and 2) NS-SAR ADCs suffer from the charge loss in their passive filters.

Considering the above discussion, exploring a new NS-SAR ADC with higher noise-shaping order, boosting the SNDR while maintaining low power consumption is an open topic in this domain. Also, an analytic study is required to estimate the power consumption of NS-SAR ADC, considering the effect of non-idealities similar to what has been done for conventional Nyquist ADCs, i.e., flash, pipeline, SAR, and ΔΣ-based IADCs [7–9].

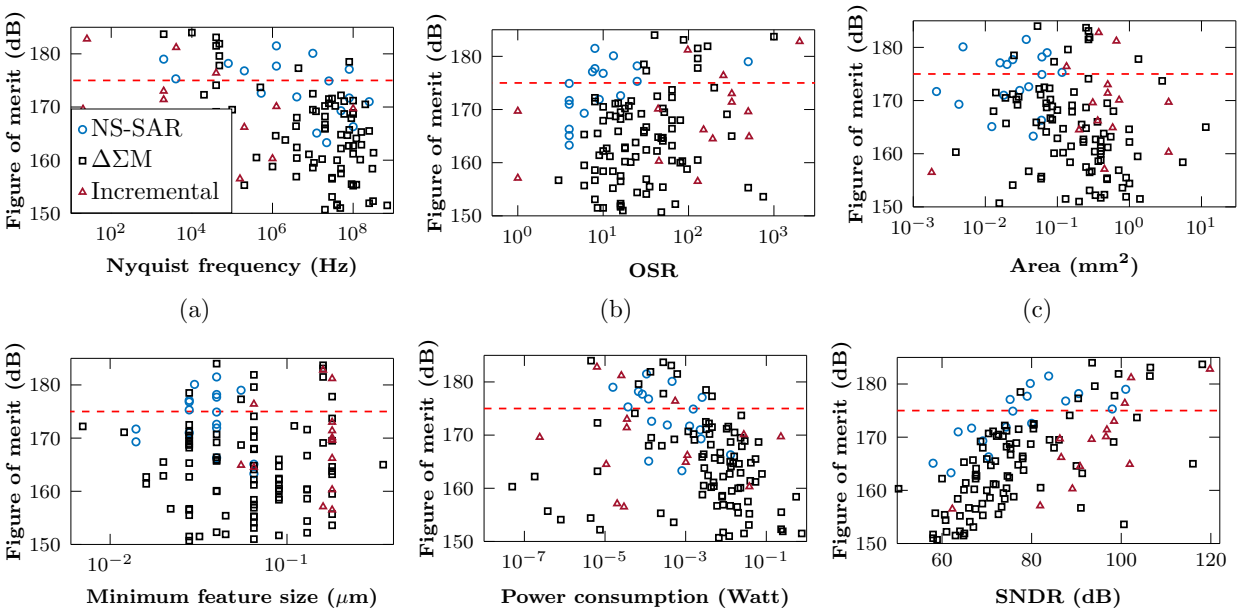



Figure 1.1 Comparing efficiency of NS-SAR ADCs with ΔΣMs and IADCs in terms of different design parameters; $FoM_S$ versus (a) Nyquist frequency, (b) Oversampling ratio (OSR), (c) Chip area, (d) Technology minimum feature size, (e) Power consumption, and (f) Signal-to-noise-and-distortion-ratio (SNDR)

## 1.3 Research Objectives

To tackle the problem mentioned in Section 1.2, we propose in this thesis two hybrid structures and an analysis to estimate the power-bound of the proposed ADCs. The main objectives of this thesis are listed as follows:

1. The first objective aims to increase the noise-shaping order of NS-SAR ADCs without increasing the order of the FIR filter. This strategy avoids causing signal attenuation while limiting the number of comparator inputs and mitigating the need for boosting the op-amp gain to compensate for signal attenuation. High-level modeling and analysis estimate the performance of the proposed MASH 2-2 NS-SAR ADC considering the main non-idealities effects. This analysis is then used to determine the specifications of the implemented sub-blocks.

2. The second strategy benefits from the advantages of the first objective to exploit a power-efficient incremental NS-SAR ADC, which does not suffer from the high power consumption of operational transconductance amplifier (OTA) based integrators and multi-bit flash-based quantizers. The aim is to improve resolution and power/area efficiency to meet the needs of high-performance multi-channel instrumentation applications. Therefore, the first solution is used in incremental mode, leveraging a two-step incremental mode conversion technique.

3. The third objective seeks to determine the power-bound of the NS-SAR ADCs based on analyzing the effect of thermal noise, capacitor mismatch, and CMOS technology minimum feature size. This analysis can be used as a strategy to design the NS-SAR ADCs, achieving the two first objectives in this thesis.

## 1.4 Claimed Contributions

Seeking the mentioned objectives resulted in four following listed publications proposing two ADC architectures and a power-bound analysis based on the second one.

1. Akbari, Masoume, and Mohamad Sawan. "Analog-to-digital conversion device comprising two cascaded noise-shaping successive approximation register analog-to-digital conversion stages, and related electronic sensor." U.S. Patent No. 11,152,950. 19 Oct. 2021.

2. M. Akbari, M. Honarparvar, Y. Savaria and M. Sawan, "OTA-Free MASH 2–2 Noise Shaping SAR ADC: System and Design Considerations," 2020 IEEE International Symposium on Circuits and Systems (ISCAS), 2020, pp. 1-5,

   doi:10.1109/ISCAS45731.2020.9180832.

3. M. Akbari, M. Honarparvar, Y. Savaria and M. Sawan, "OTA-Free MASH Two-Step Incremental ADC based on Noise Shaping SAR ADCs," 2020 18th IEEE International New Circuits and Systems Conference (NEWCAS), 2020, pp. 138-141, doi: 10.1109/NEWCAS49341.2020.9159802.

4. M. Akbari, M. Honarparvar, Y. Savaria and M. Sawan, "Power Bound Analysis of a Two-Step MASH Incremental ADC Based on Noise-Shaping SAR ADCs," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 68, no. 8, pp. 3133-3146, Aug. 2021, doi: 10.1109/TCSI.2021.3077366.

The first two publications, i.e., a patent and a peer-reviewed ISCAS conference paper, along with one chapter of the thesis containing the unpublished material related to the proposed prototype implementation, contribute toward meeting the first objective. A MASH 2-2 NS-SAR ADC is proposed comprising two similar stages of second-order amplifier-based NS-SAR ADCs to obtain a fourth-order noise shaping performance. This architecture removes the need for increasing the order of the FIR filter and the amplifier gain for enhancing the NS-order of the ADC. Also, compared to $\Delta\Sigma$, it is not required to employ power-hungry OTAs and flash-based multi-bit quantizers, at a high OSR value. The proposed MASH structure is less complex than $\Delta\Sigma$-based topologies since, benefiting from the EF-NS-SAR properties, no additional DAC and subtractors are required for extracting the residue and feeding it to the second stage of the MASH structure.

As discussed in CHAPTER 6, modeling the proposed ADC by a code in MATLAB confirms that the second stage needs components with more relaxed specifications and power consumption compared to those of the first stage. This feature justifies adding the second stage to obtain a higher NS-order with no significant power and complexity penalty. In order to reduce the complexity and extra hardware required for the MASH structure and save power, the op-amp in the first stage simultaneously amplifies the residue and samples it on hold capacitors used to transfer it to the second stage. The proposed ADC implemented in the ST-28nm FD-SOI CMOS process achieves in post-layout simulations an SNDR of 75 dB over a 100 kHz signal bandwidth and OSR of 10, with dual supply voltages of 1.8 V and 1 V. Compared to prior NS-SAR ADCs, it uses lower resolution SAR quantizers and a less complex architecture. The MATLAB code confirms that using a data weighted averaging

calibration method suppresses the harmonics power due to the DAC capacitors mismatch observed in the power spectral density of the proposed ADC. The prototype chip has been designed and submitted for fabrication but will be delivered with delay after completing this thesis. Based on measurement results, a fairer comparison with the state-of-the-art NS-SAR ADCs will be made later.

The third publication, i.e., a peer-reviewed NEWCAS conference paper, proposes an architecture to achieve the second objective. The idea is to use the first proposed ADC in a two-step incremental mode to enhance its resolution for multi-channel applications. Benefiting from the advantages of the first proposed ADC, the proposed sixth-order multi-step architecture achieves wider bandwidth comprising a lower OSR value without suffering from the high-power consumption caused by OTAs and multi-bit flash-based quantizers when compared with the prior IADCs. A smaller number of comparators makes it efficient regarding power dissipation and area. Since imperfections in the $\Delta\Sigma$ mode are reflected in the incremental mode, similar effects of non-idealities are expected for both proposed ADCs.

The fourth publication, i.e., a TCAS-I journal paper, proposes an analytic process to calculate the power-bound of the second proposed ADC, achieving this thesis's third objective. This analysis provides the effect of three factors of thermal noise, capacitor mismatch, and minimum feature size of CMOS technology on the performance of the proposed IADC. The derived equations predict better performance for the proposed NS-SAR IADC compared to a conventional $\Delta\Sigma$-based IADC with similar specifications. Comparing the calculated power consumption with the prior work's experimental results confirms that the proposed analytic method is applicable to estimate the power consumption of conventional amplifier-based NS-SAR ADCs. It can also be used for NS-SAR ADCs in $\Delta\Sigma$ or incremental mode with multi-stage and multi-step topologies designed in various CMOS technologies. Furthermore, it indicates the dominant factors that determine the power consumption according to the targeted resolution, power supply, and sampling capacitor size.

## 1.5 General Organization of the Thesis

A comprehensive literature review focuses on the main challenges of incremental ADCs and NS-SAR ADCs in CHAPTER 2. It discusses the main drawbacks and techniques to overcome them.

Three chapters of this hybrid thesis are based on three publications to obtain mentioned objectives in CHAPTER 1. There is also a complementary chapter containing the unpublished material.

The first publication is a peer-reviewed conference paper, presented in CHAPTER 3, mainly explores a new architecture to increase the noise-shaping order of NS-SAR ADCs without increasing the filter order. A MASH 2-2 structure comprising two similar second-order NS-SAR ADCs is proposed to obtain the first objective. This chapter describes the proposed topology and provides the behavioral model and macro-model simulation results.

The second publication presented in CHAPTER 4 is also a peer-reviewed conference paper seeking to achieve the second objective and address the OTAs and multi-bit flash-based quantizers problems of conventional IADCs in CHAPTER 2. The proposed ADC in CHAPTER 3 in a two-step incremental mode to improve the resolution make it suitable for multi-channel applications. System-level structure and macro-model implementation of the proposed architecture are discussed. Also, MATLAB/SIMULINK simulation results for the behavioral model of the proposed ADC are presented. The supplementary material provides the time-domain analysis of the IADC operation and the macro-model simulation results.

In CHAPTER 5, the third publication, which is a journal paper, is presented. The third objective is achieved by proposing an analytic process to estimate the power bound of the second proposed ADC in CHAPTER 4. This chapter generalizes the equations derived in CHAPTER 4 and employs them to obtain the required equations to estimate the proposed IADC power bounds limited by thermal noise, mismatch, and CMOS process. The proposed method results can also estimate the power consumption of conventional amplifier-based NS-SAR ADCs.

CHAPTER 6 provides further information to verify the feasibility of the proposed MASH 2-2 NS-SAR ADC discussed in CHAPTER 3. The most critical circuit imperfections are described and modeled using a code in MATLAB. This chapter then discusses the circuit-level and layout implementation and considerations along with the post-layout simulation results of the proposed ADC.

CHAPTER 7 provides a general discussion on the proposed ADC structures and power bound analysis. It describes the main features of the proposed works. The conclusion, main contributions of this research, and suggestions for future work are all drawn in CHAPTER 8.

# CHAPTER 2 LITERATURE REVIEW ON ANALOG TO DIGITAL CONVERSION METHODS

In this section, conventional ADC architectures are compared, and some fundamental trade-offs in ADC design are explored. Also, a literature review on ADCs for multi-channel applications is presented. Fig. 2.1 shows the structure of the discussed conventional ADCs.

One of the rudimentary types of ADCs is Flash which compares sampled input to all decision levels in parallel. The conversion speed is fast but requires $2^B - 1$ comparators with challenging offset managing for $B > 6$ bit applications. However, successive approximation register (SAR) ADCs usually employ only one comparator to determine the bits sequentially. So, the conversion time increases proportionally with $B$. The linearity of SAR ADCs is determined by the digital to analog converter (DAC), and comparator noise is a significant issue for $B > 10$. Therefore, the redundancy method is used to relax the design specifications. Redundancy alleviates errors caused by insufficient settling time, as more precise sampling rate is required. Pipeline and time-interleaved (TI) ADCs have been introduced to achieve higher conversion speeds. In pipeline structures, matching analog and digital front-end gains is a critical issue that is sometimes addressed through calibration. On the other hand, $\Delta\Sigma$Ms obtain higher resolutions by employing oversampling and noise shaping techniques. The performance of $\Delta\Sigma$Ms is typically set by DAC and the first stage of the loop filter.

Choosing the ADC architecture depends on the specific application's speed, resolution, and power requirements. According to Fig. 2.2, categorizing ADC architectures concerning resolution and bandwidth exhibits a fundamental trade-off between these two metrics. In higher resolution applications at low bandwidths, delta-sigma modulators ($\Delta\Sigma$Ms) are dominant, followed by successive approximation, pipeline, and flash ADCs.

The current trend is mixing and matching the conventional options in designing hybrid ADC architectures, for example, embedding a SAR ADC in $\Delta\Sigma$Ms to design NS-SAR ADCs, or pipelining SAR ADCs as pipe-SAR ADCs. Fig. 2.3 and Fig. 2.4 quantify the speed-resolution-power trade-off for the conventional and hybrid state-of-the-art ADCs using the data from [6]. As expected, Flash and TI ADCs achieve the widest bandwidth, i.e., half of the Nyquist frequency, consuming the most considerable amount of power. However, SAR ADCs have the minimum power consumption. Considering sub-Mega Hertz bandwidth, most of the SAR ADCs' power consumption is less than 1 $\mu W$ but with SNDR limited to 80 dB, which is lower than other types of ADCs. $\Delta\Sigma$Ms achieve the highest resolution in incremental mode with mid-level power consumption but the maximum Nyquist frequency of 1 MHz. Also,

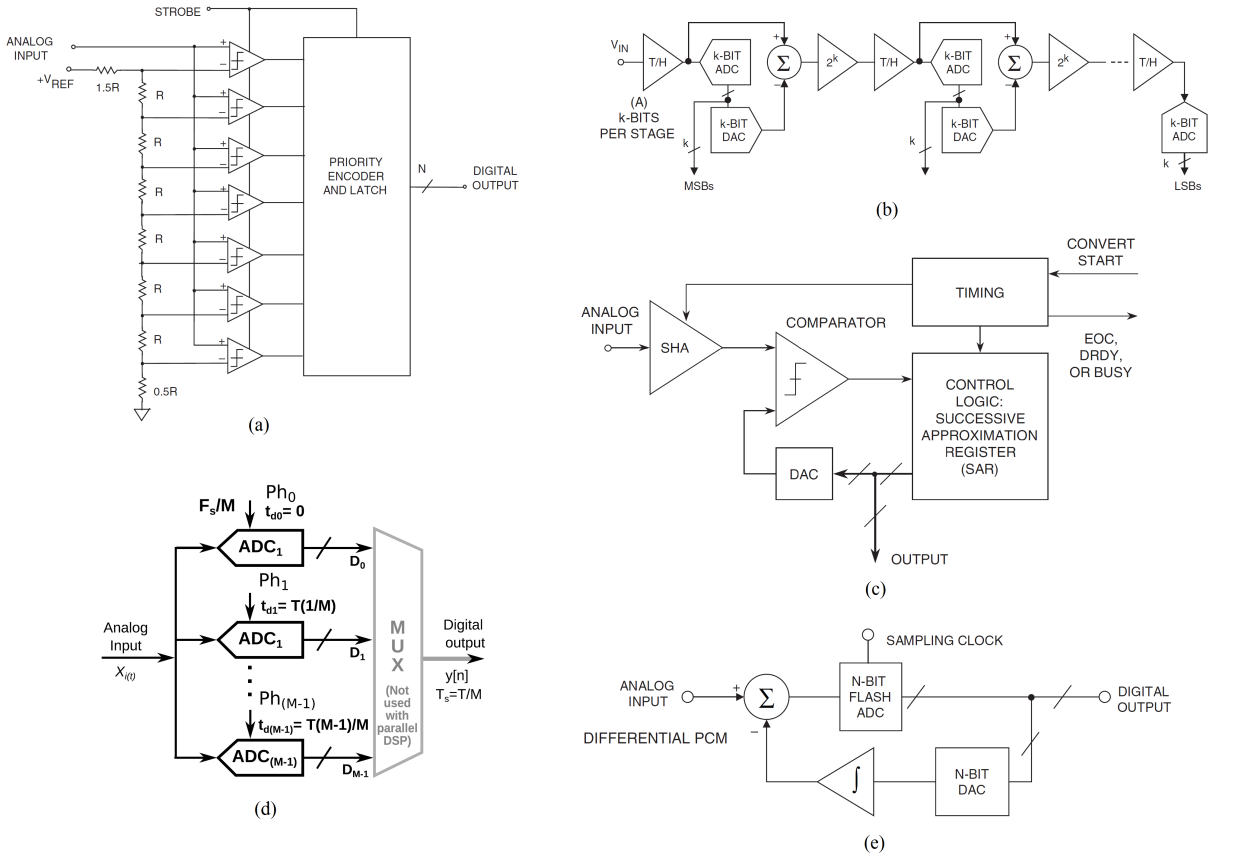



Figure 2.1 Structure of the conventional ADCs. (a) Flash, (b) Pipeline, (c) SAR, (d) Time interleaved (TI), (e) Delta-sigma modulator ($\Delta\Sigma$M) [10] (©[2005] IEEE)

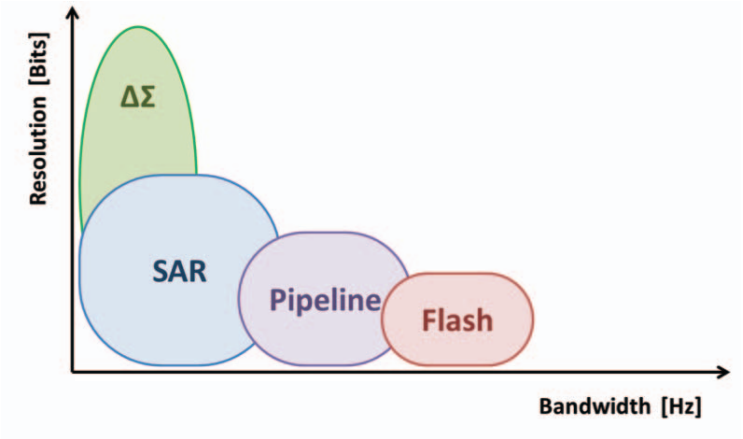



Figure 2.2 Overview of conventional ADC architectures [11] (©[2015] IEEE)

ΔΣMs obtains the speed of most of the pipeline ADCs with better performance in terms of resolution and power. For sub-Mega Hertz bandwidth applications, the hybrid NS-SAR ADCs present SNDR values close to that of ΔΣMs with significantly lower power consumption. Nevertheless, the pipe-SAR structures have benefited from SAR ADC's advantages to achieve higher resolution consuming less power at the same speed.

This thesis targets the sub-Mega Hz bandwidth applications, which moves the focus from Flash, pipeline, and TI architectures to SAR, ΔΣ, incremental, and NS-SAR ADCs.

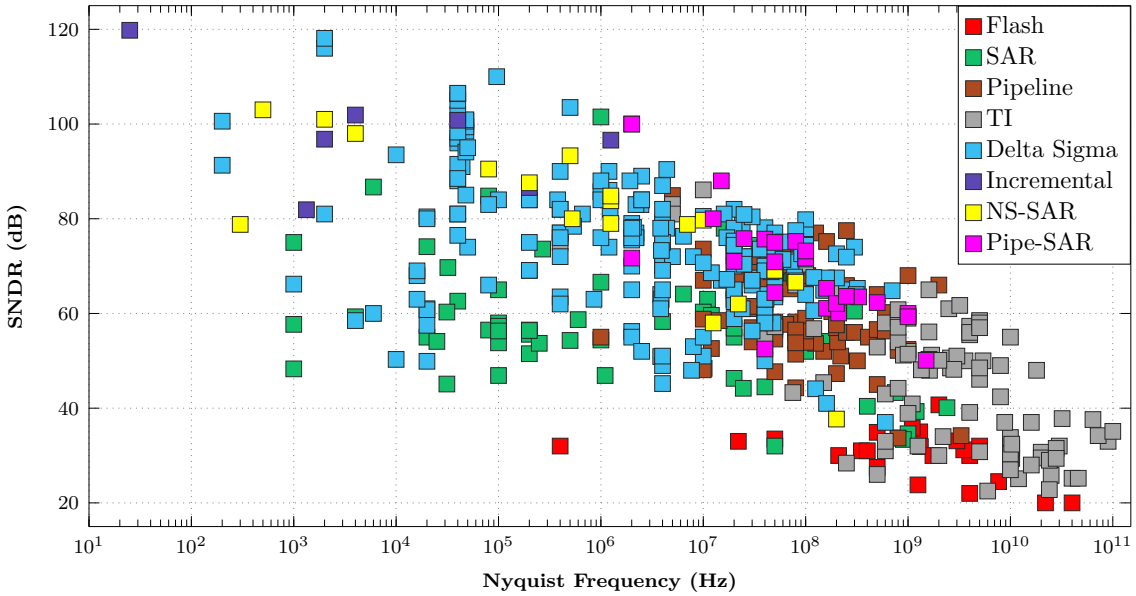



Figure 2.3 Survey of resolution (SNDR) versus Nyquist frequency for various ADC architectures with data compiled from 2021 online survey [6]

The main types of ADCs that are used widely for multi-channel applications are presented in the following section. The advantages and limitations of using these topologies will be discussed to find a way to mitigate some of these limitations to achieve a high-performance structure. Successive approximation register (SAR) ADCs have demonstrated the best energy efficiency in moderate resolution converters because of mostly digital components and few active components. They are popular in multiplexed systems because they have low latency and fast response even to a full-scale input step without settling issues. However, the power efficiency and bandwidth are degraded as the resolution increases. It is due to two following main reasons. First, the DAC capacitance doubles by a 1-bit increase in resolution; thus, extra power is required to drive this large capacitance. A larger DAC also causes mismatch and settling error and decreases the speed of ADC. Second, the input-referred noise of the comparator becomes more significant, so the power-hungry pre-amplifier should be considered

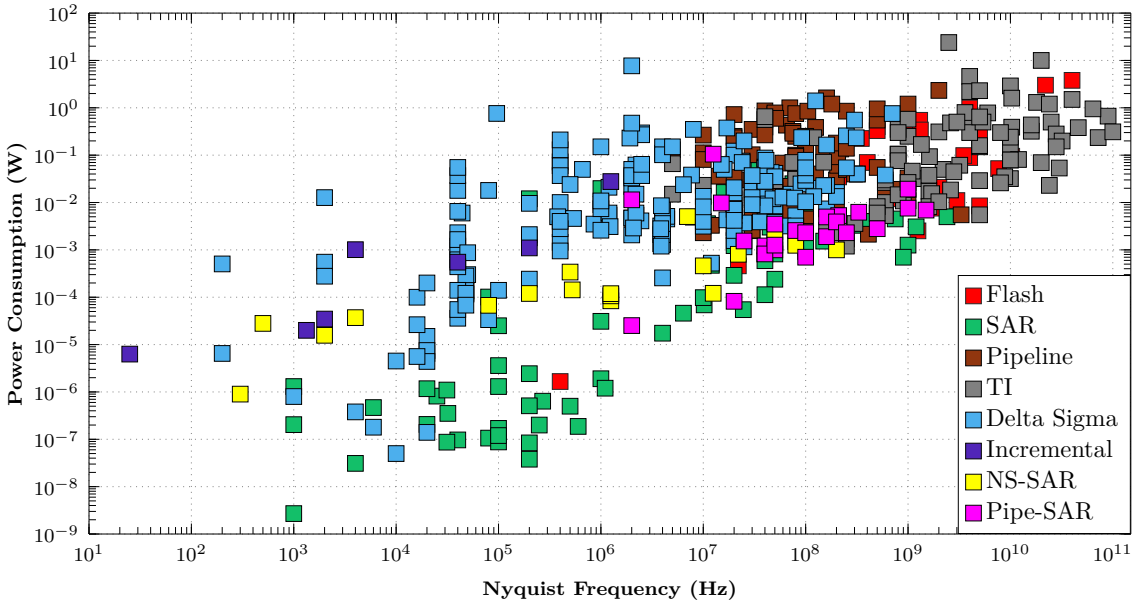



Figure 2.4 Survey of power versus Nyquist frequency for various ADC architectures with data compiled from 2021 online survey [6]

in the design to suppress this noise [12]. The resolution of SAR ADC can be increased to 18-bit using calibration and dithering; however, it makes the circuit more complex [13]. Dual-slope and delta-sigma ($\Delta\Sigma$) ADCs can achieve higher resolution than SAR ADCs. Therefore they are used for instrumentation applications. However, the energy-efficiency of dual-slope ADCs is poor and they are slow since their resolution is linearly dependent on conversion time [14]. In contrast, $\Delta\Sigma$ ADCs can achieve high resolution in less time by using oversampling and noise-shaping, making them more energy-efficient. $\Delta\Sigma$Ms are usually used in incremental mode, as an incremental ADC, for instrumentation applications [3, 15–17].

## 2.1 Previous Contributions on Incremental ADCs

In this section, the concentration is on incremental ADCs (IADCs). It gives an overview of the concept of IADC and different suggested techniques in the literature to extend their accuracies, such as extended counting and two-step IADCs. Incremental analog-to-digital converters (IADCs) are excellent in low-frequency, high-accuracy sensor interface applications. IADCs benefit from noise shaping to achieve high-resolution performance using an embedded $\Delta\Sigma$ modulator. However, they provide a sample-by-sample conversion similar to Nyquist rate ADCs by periodically resetting the $\Delta\Sigma$ modulator. This feature makes IADCs efficient in multi-channel applications where an individual ADC is multiplexed between sev-

eral channels. IADCs have advantages over ΔΣMs, such as simpler decimation filters [17], less latency, better immunity to idle tone, and higher stability. First-order IADCs (IADC1) have the best noise performance but consume high power. It is because of the high number of clock periods ($2^N$) for performing one conversion to achieve an N-bit resolution [18]. The higher-order single loop IADCs achieve the same SQNR with improved power efficiency; however, they are prone to instability. Multi-stage-noise-shaping (MASH) architecture has also been used to extend the accuracy of IADCs. This method requires extra hardware, which makes the circuit complex. The primary concern about the MASH structure is the noise leakage resulting from the mismatch between analog, and digital circuity [19].

The operational transconductance amplifiers (OTA) used in the first loop of ΔΣ-based ADCs consume considerable power to obtain a high gain, high speed, and stability in high-resolution configurations [20]. Fig. 2.5 depicts the schematic of the IADC presented in [21] that employs a slicing technique to decrease the first OTA power consumption. However, using the weighting function impacts this method's effectiveness and cannot handle the DAC mismatch errors induced by a multi-bit quantizer [20].

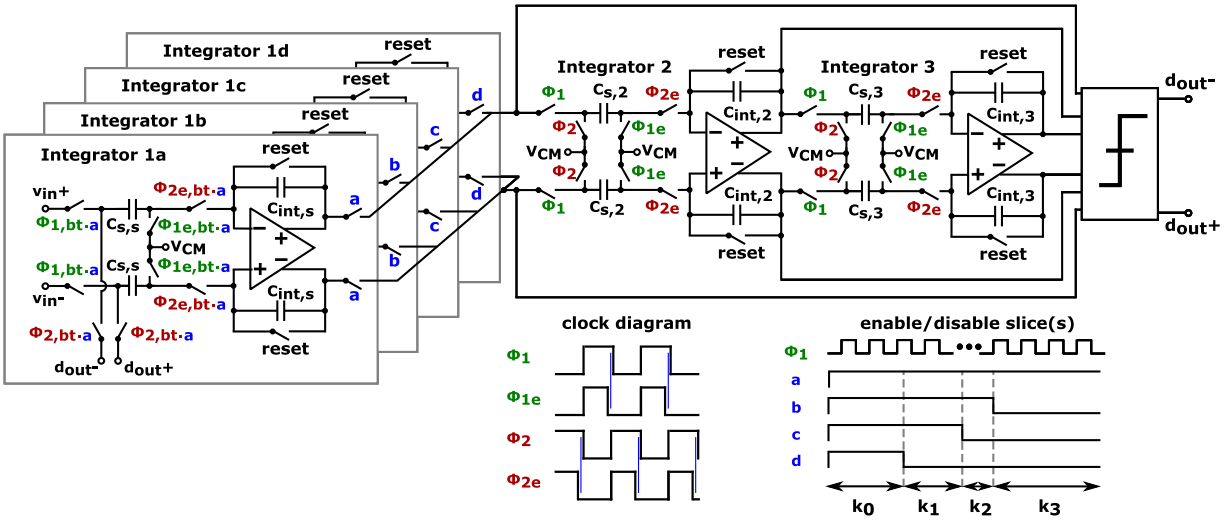



Figure 2.5 Overview over the implemented modulator including integrator slicing presented in [21] (©[2019] IEEE)

Hybrid and multi-step structures have been utilized to improve the power efficiency and performance of IADCs. A combination of ΔΣ-based IADC and zoom SAR ADC has been presented in [5] to achieve 20-bit resolution. Fig. 2.6 demonstrates the block diagram of the zoom ADC. A 6-bit SAR ADC performs a coarse conversion to determine the approximate zoom range for the 15-bit fine IADC.

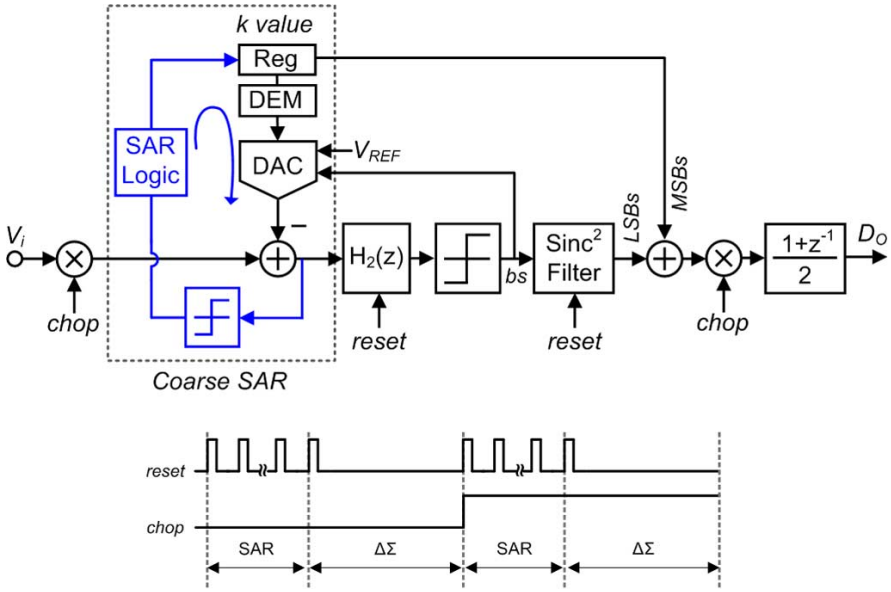



Figure 2.6 Block diagram of a zoom IADC presented in [5] (©[2013] IEEE)

Besides, multi-step extended counting and multi-step higher-order IADCs are mainly based on further digitizing the residue voltage of coarse quantization. Despite employing the techniques mentioned above, the OTA-based integrators still limit the efficiency of IADCs. An overview of these two types of hybrid IADCs is presented in the following sections.

### 2.1.1 Multi-step Extended Counting IADCs

This idea was first presented as feedforward residue compensation (FRC) in 1998 [22]. This method extends the resolution of Nyquist rate converters by applying an oversampling modulator loop as shown in Fig. 2.7.

Extended counting IADCs are implemented in two types [17]. 1) Using a Nyquist rate ADC such as a power-efficient cyclic or SAR ADC, which performs the fine quantization by sampling the residue voltage before the reset pulse. 2) Using hardware sharing. Fig. 2.8 displays an example of the first type, along with its simplified timing diagram. The residue stored at the output of the last integrator is sampled and held by a SAR ADC before the reset pulse clears the voltage. Then it will be digitized by the SAR binary search. For attaining a high resolution, the SAR ADC resolution should be high (for example, 11-bit); thus, additional power is required for driving the large input capacitance of the SAR [1].

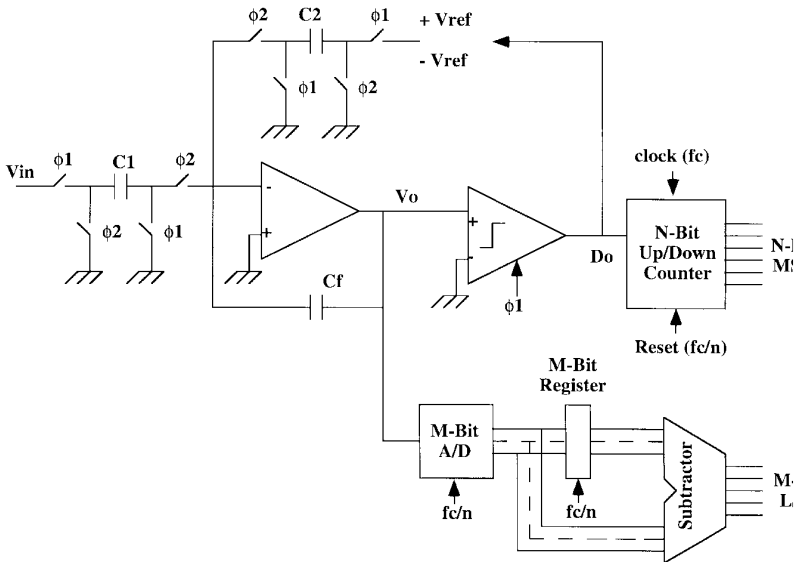



Figure 2.7 First-order FRC architecture introduced in [22] (©[1998] IEEE)

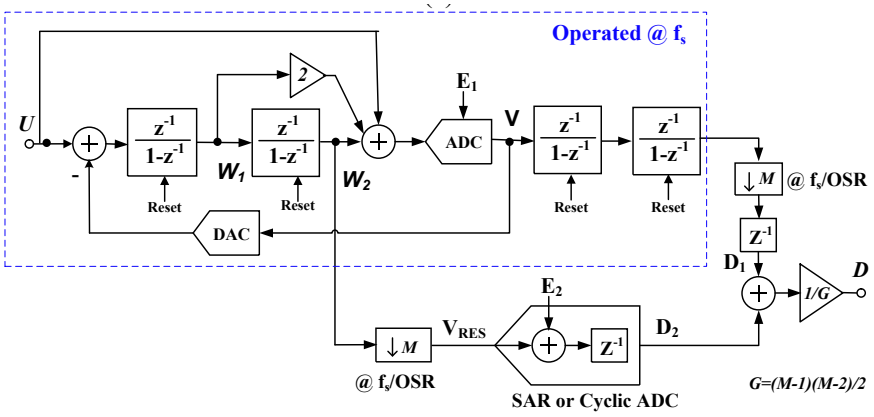



Figure 2.8 Prior art of extended counting IADC using a Nyquist-rate ADC [1] (©[2010] IEEE)

In hardware sharing extended counting schemes, the conversion is performed in two steps instead of cascading two ADCs. They mainly operate as an IADC in the first step, and then the IADC is reconfigured as a Nyquist rate ADC in additional steps/steps. Fig. 2.9 illustrates an example in which the IADC1 operates as the coarse ADC in the first step, and the residue voltage is stored in the integrator. In the second step, the fine quantization is performed by reconfiguring the circuit as a cyclic ADC in the second step [23]. In [24], the first step is an IADC1 with 31-level quantizer with OSR of 32. A cyclic ADC works for another 8 clock period in the second step. It suffers from more parasitic introduced by complex design and mismatch and gains error between stages, which requires extra calibration.

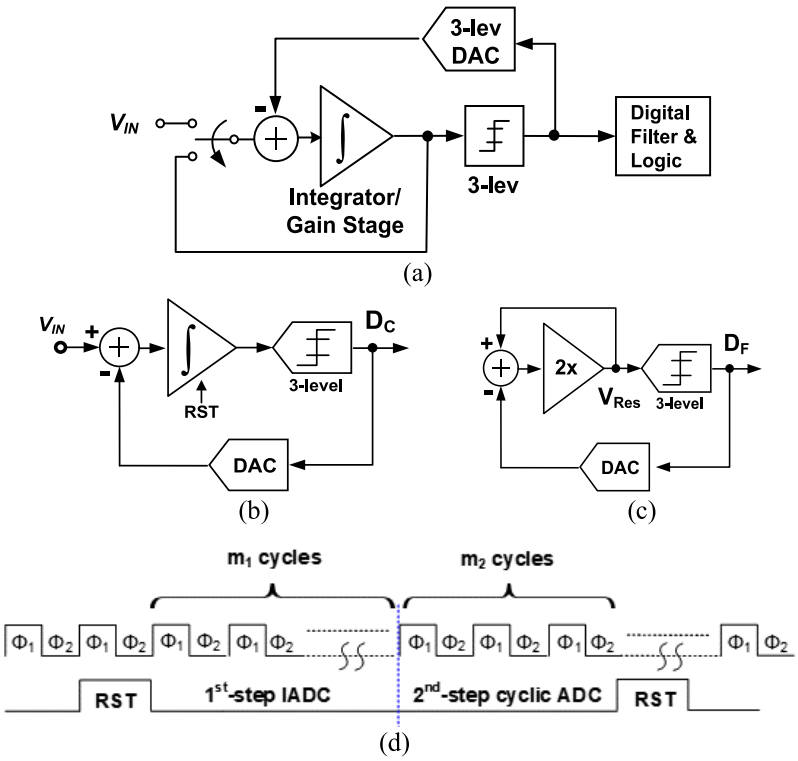



Figure 2.9 Prior art of IADC with extended counting using hardware sharing [23, 24] (a) An IADC1 with hardware-reusing extended counting, (b) First step: configured as a first-order IADC for coarse quantization, (c) Second step: extending the accuracy by reconfiguring as a cyclic ADC, (d) Timing diagram ( [25] ©[2021] IEEE)

Two other examples of this type of ADC use the multi-slope extended counting and extended binary counting in additional steps. A 16-bit IADC is presented in [26] using multi-slope extended counting. A first-order IADC (IADC1) operates in the three-step conversion cycle. It is reconfigured as multi-slope ADCs in two extra steps. The performance of the introduced IADC is better than a second-order IADC while using only one active integrator in its circuity.

Another multi-step extended counting IADC utilizing one integrator has been introduced in [25] and shown in Fig. 2.10. In the first step, it works as an 8-bit IADC1 using an FIR feedback and OSR of 256. In the second step, a 10-bit $2C$ SAR ADC is employed to quantize the residue of the first step. However, the accuracy and linearity of $2C$ DAC are limited by the non-idealities.

The circuit complexity is the main problem of the discussed ADCs comprising the extended counting method. Furthermore, the linearity of the Nyquist ADC limits the overall linearity of the ADC.

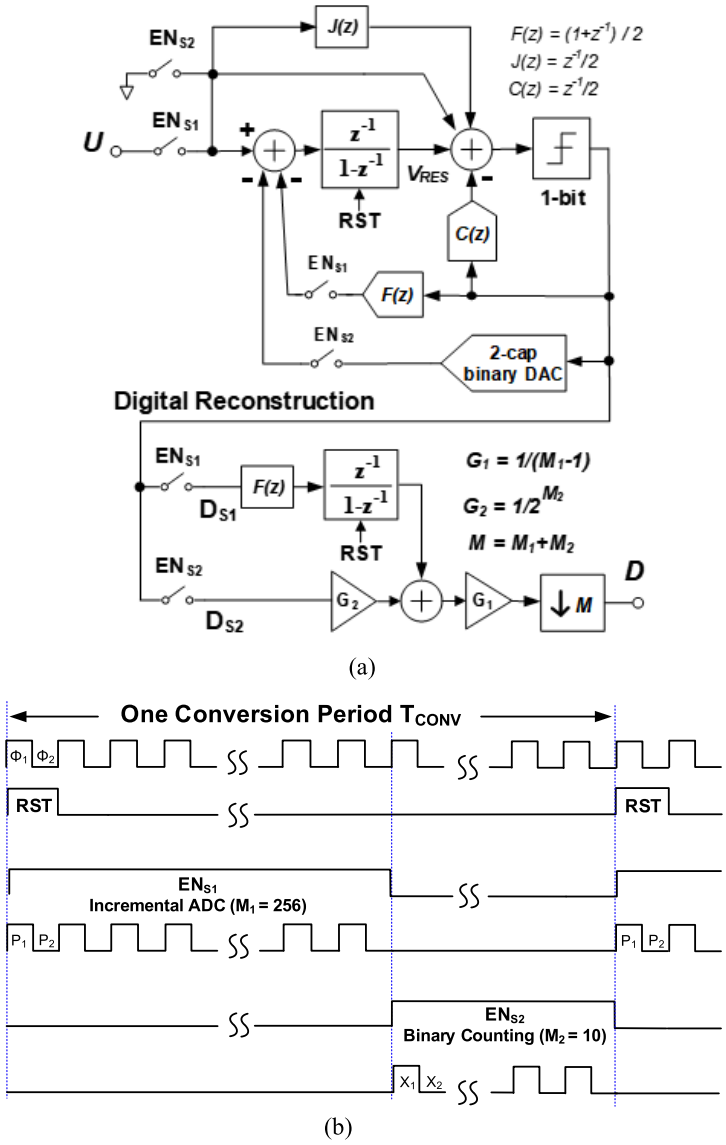



Figure 2.10 (a) System-level z-domain block diagram of the IADC1 with SAR binary extended counting, (b) Simplified timing [25] (©[2021] IEEE)

### 2.1.2 Multi-step IADCs

The higher SQNR in IADCs can be achieved by increasing the OSR and modulation order. The latter method is more effective; however, it requires extra op-amps. The main concern in higher-order modulators is the stability that needs a higher-resolution internal quantizer to make it stable. These requirements increase the complexity and power consumption of the structure. In the multi-step IADC method, each conversion cycle includes separate steps. It obtains higher-order performance by reusing hardware, thus enhancing the power efficiency.

Fig. 2.11 shows the z-domain model of a two-step IADC2 used in [27–29]. In the first step, with $M_1$ clock periods, the circuit is used as a conventional IADC2 (Fig. 2.11(b)). The residue voltage, $V_{res}$, resulted at the end of the first step after $M_1$ cycles. It is stored in the second integrator ($INT2$) as follows:

$$V_{res} = W_2[M_1] = \sum_{k=1}^{M_1-1}\sum_{i=1}^{k-1} U[i] - \sum_{k=1}^{M_1-1}\sum_{i=1}^{k-1} D_1[i] \tag{2.1}$$

The $INT2$ holds the residue voltage to be used for the fine quantization in the next step. The second step, which lasts for $M_2$ cycles, performs the fine quantization by reconfiguring the analog modulator and the digital filter, as shown in Fig. 2.11(c).

$INT2$, which holds the residue voltage, stops sampling. The residue voltage is fed into the $L$-level quantizer and then to the first integrator ($INT1$). $INT1$ is reset and then samples the residue voltage stored in $INT2$. This structure works like a MASH 2-1 and cancels the error of the first step IADC2. After the two steps of conversion, the signals are given by:

$$\begin{aligned}\widetilde{U} &= \frac{2}{(M_1)\cdot(M_1-2)\cdot(M_2-1)}\cdot\ E_2 \\ &= \frac{2}{(M_1-1)\cdot(M_1-2)}\cdot\Big(\sum_{k=1}^{M_1-1}\sum_{i=1}^{k-1} D_1[i] - \frac{1}{M_2-1}\sum_{i=1}^{k-1} D_2[i]\Big)\end{aligned} \tag{2.2}$$

where $\widetilde{U}$ is the average of the input signal during $(M_1+M_2)$ cycles, and $E_2$ is the error signal of the second step operation. The equivalent quantization error after the two-step conversion can be achieved as follows:

$$E_{21} = \frac{2}{(M_1-1)\cdot(M_1-2)\cdot(M_2-1)}\cdot\frac{V_{FS}}{L-1} \tag{2.3}$$

As shown in [28], the optimum $OSR = M = M_1 + M_2$ of this two-step structure is achieved when $M_1 = 2M_2 = 2M/3$. The results presented in this work show that the SQNR of this two-step IADC is 7 dB lower than the SQNR of a single-loop IADC3. However, it achieves a noise-shaping performance one order higher than that of a single-loop IADC2. The energy efficiency is improved significantly, and switching hardware between two steps is done only by an additional timing control. Therefore, this circuit is simpler than prior hardware-sharing extended-counting structures. Fig. 2.12 shows another example of using this method. In the first step, this work uses a MASH 2-1 IADC with different quantization bits in each stage and reconfigures the structure to an IADC2 in the second step. Simulink simulation results show that this structure achieves an SQNR close to a 5-th order IADC.

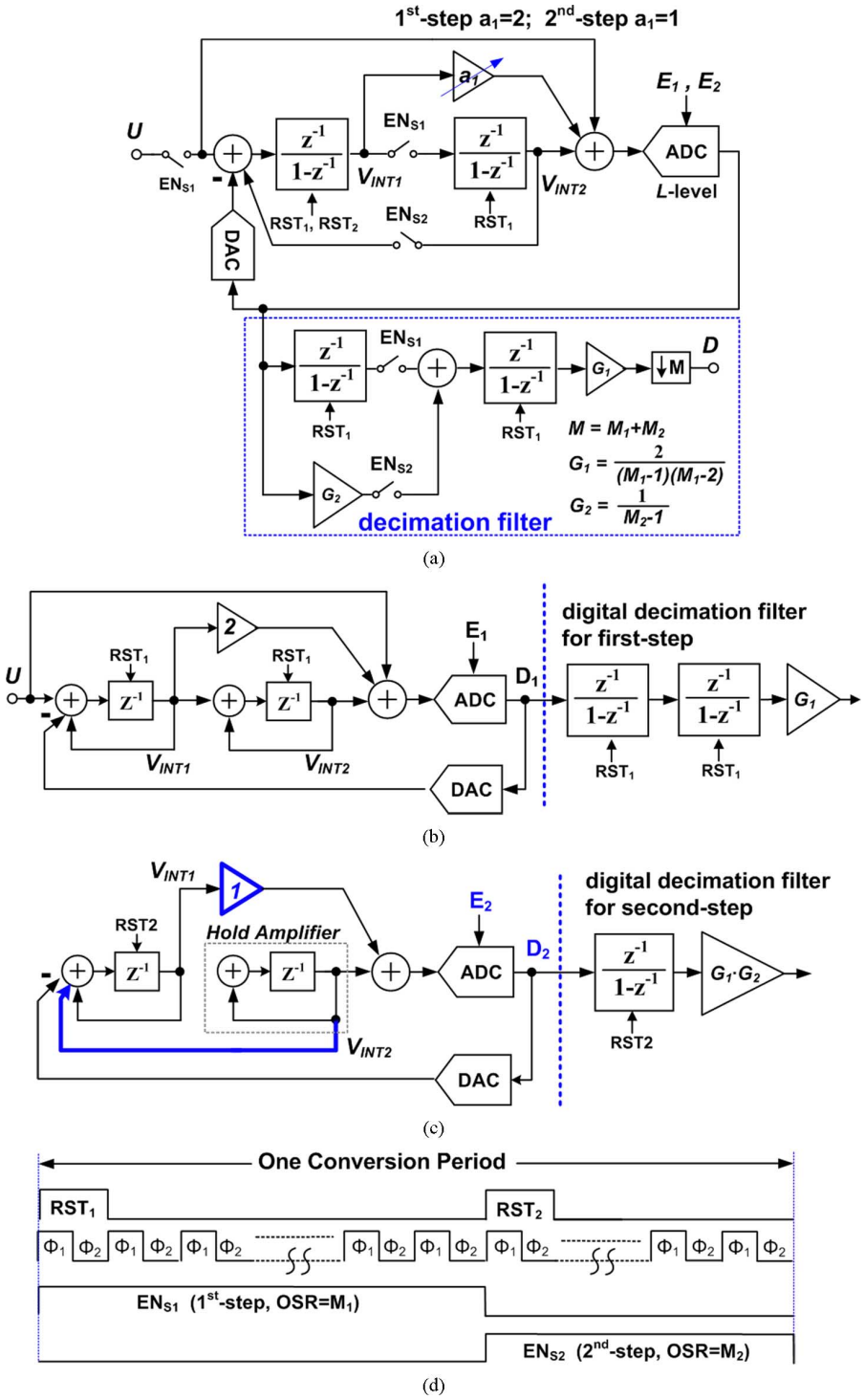



Figure 2.11 (a) Prior art of two-step I-ADC [28] (©[2015] IEEE), (b) First step: second-order IADC, (c) Second step: reconfigured as a first-order IADC to achieve one extra order of noise shaping, (d) Timing diagram

The multi-step method efficiently decreases the area and power consumption, compared to single-loop high-order IADCs, by reusing the hardware [30, 31]. However, as can be seen, they still suffer from the power and area cost of the OTA-based integrators and flash-based quantizers. For instance, the structure shown in Fig. 2.12 uses three OTA-based integrators in the first step. It also needs four comparators to implement two required flash-based quantizers.

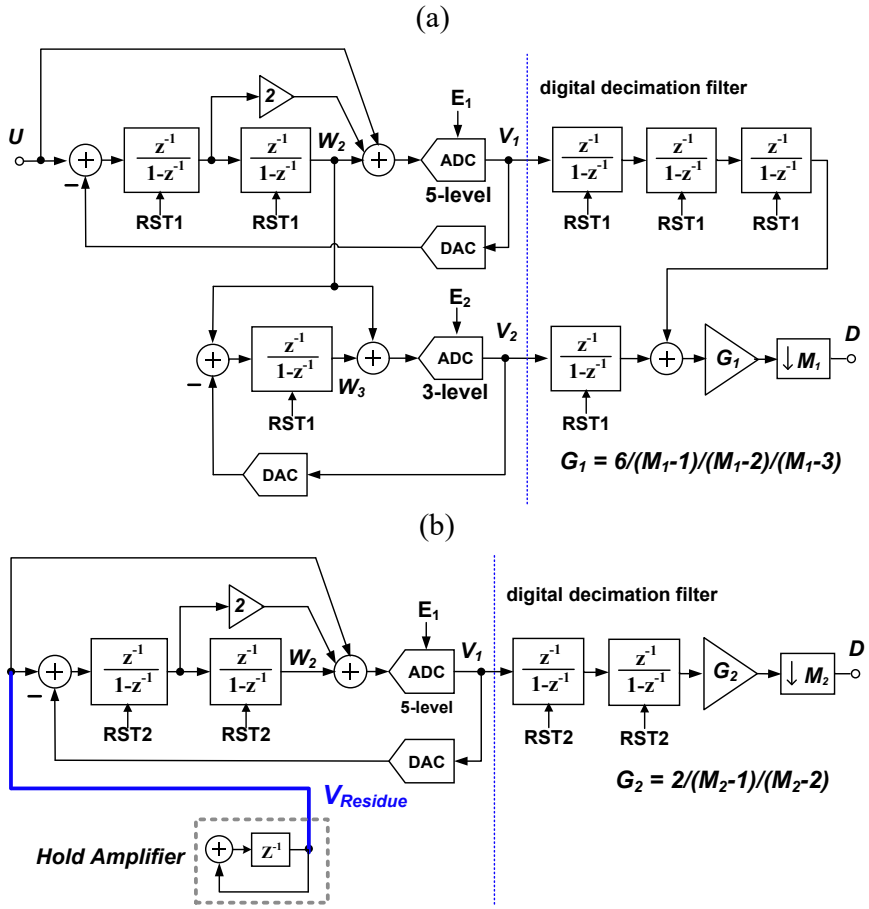



Figure 2.12 A MASH IADC in a two-step operation [30] (©[2015] IEEE); (a) $1^{st}$-step: a 2-1 MASH IADC, (b) $2^{nd}$-step: an IADC2

## 2.2 Previous Contributions on Noise-Shaping SAR ADCs

This section describes the noise-shaping SAR (NS-SAR) ADCs, their operation, and their features, which make them proper to be utilized instead of conventional $\Delta\Sigma$ modulators in several architectures, including IADCs. NS-SAR ADCs have employed the oversampling,

and noise-shaping techniques used in $\Delta\Sigma$ modulators to suppress the in-band quantization noise [12, 18, 19, 22, 26]. This technique improves the resolution without increasing the size of the capacitor array. The first step for accomplishing noise shaping in SAR ADCs is accessing the quantization error. SAR ADCs generate residue voltage on the capacitor array at the end of each internal conversion cycle. This residue voltage is considered the quantization noise. The residue of the last conversion cycle in conventional SAR ADCs is discarded at the following conversion; however, it is fed into the input in NS-SAR ADCs to realize the noise shaping. This idea was first expressed in 2012 [12] gaining a first-order noise shaping function. A passive FIR filter and an opamp-based IIR filter are applied in the feedback path to process the residue voltage, $V_{RES}(z)$, as is shown in Fig. 2.13. This process generates the $Y(z)$, which then will be quantized after summing with the input signal, $V_{IN}(z)$. A pair

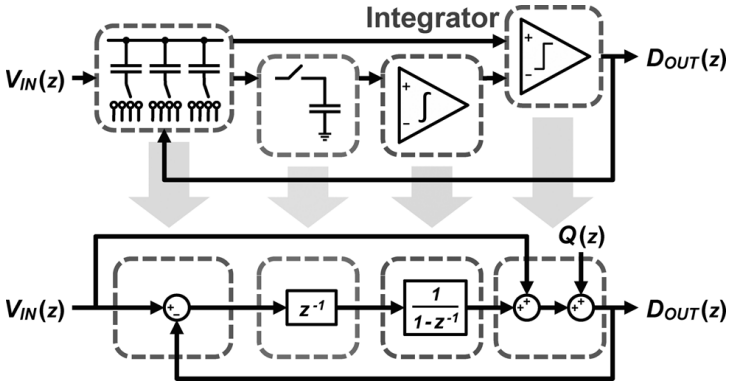



Figure 2.13 Noise shaping SAR ADC by cascading FIR/IIR filter [12] (©[2012] IEEE)

of two-capacitor arrays realize the two-tap FIR filter; however, the IIR filter is constructed using a simple, single-stage op-amp with a feedback capacitor. These two filters cause the main drawbacks. The OTA-based integrator limits the scaling merits of this ADC, and the FIR filter adds noise and an extra area to the circuit. The attenuation in residue signal due to transferring voltage between capacitors also causes noise leakage. Therefore, this structure cannot realize a perfect first-order noise-shaping.

Fully Passive NS-SAR (FPNS-SAR) was introduced to remove the OTA-based integrator limitation [32–36]. The first fully passive noise-shaping SAR ADC was described in [32] which was OTA-free and robust to PVT. However, the noise-shaping order was limited to first-order, with an NTF zero at 0.5. Several structures have been published in the literature to increase the noise shaping order and improve the NTF zero location. The structure presented in [34] is a novel $2^{nd}$-order NS-SAR ADC that achieves both high resolution and high power efficiency; however, it provides limited SQNR improvement of 9.5-dB and an NTF

zero at 0.75. As shown in Fig. 2.14, it uses two passive integrators to integrate the residue of a 9-bit SAR twice and feed the first and second integrated results to a 3-path comparator for dynamic summation and quantization. Besides, new techniques such as dynamic non-overlapping clock generators and tri-level majority voting (MV) are used to reduce power and noise further.

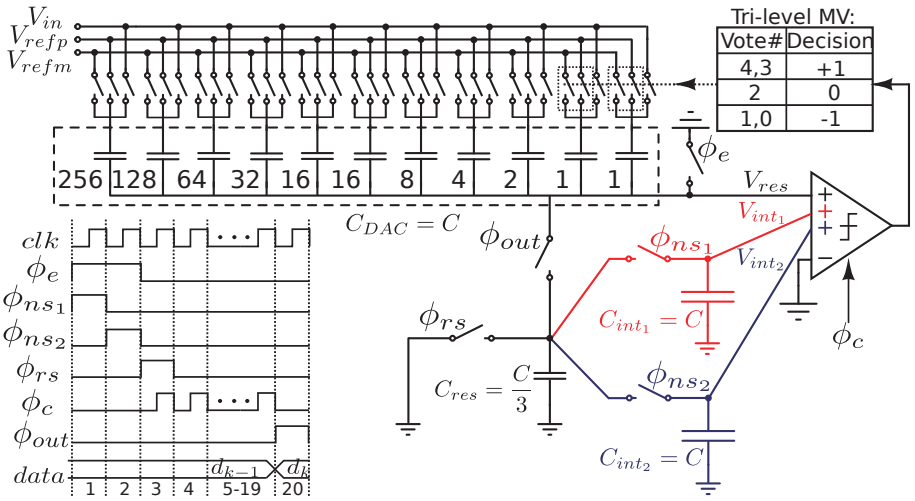



Figure 2.14 Prior art of a second-order FPNS-SAR ADC with tri-level majority voting [37] (©[2019] IEEE)

The comparator inputs provide the passive gains, $1 : 4 : 16$, to compensate for the signal attenuations caused during the residue signal transfers through the passive filter. The NTF zeros of the NS-SAR ADC are determined by the ratios of $C_{DAC}$, $C_{int1}$, $C_{int2}$, and $C_{res}$. The resulted NTF of this NS-SAR ADC is $(1 - 0.75 \cdot z^{-1})^2$.

In [36], a higher noise-shaping order is achieved. It uses a passive error feedback structure and a third-order passive filter, as shown in Fig. 2.15. Higher-order passive filters are a power-efficient way to achieve a higher noise-shaping order. The passive filter used in this work has charge- rotating capacitor, $C_1$, and two history capacitors, $C_{3,4}$. This passive filter is high speed and introduces a low thermal noise. A higher number of history capacitors can be increased to achieve a higher order of filtering.

Recently a fourth-order NS-SAR has been published, which does not need the calibration [38]. The time-interleaved (TI) method is used to increase the bandwidth of ADC limited by the SAR ADC. As illustrated in Fig. 2.16, the architecture is complicated and needs a 6-input preamplifier for the comparator. The resulted NTF of this NS-SAR ADC is $(1 - 0.5 \cdot z^{-1})^4$. The NTF zero at 0.5 shows a signal attenuation, which causes noise leakage.

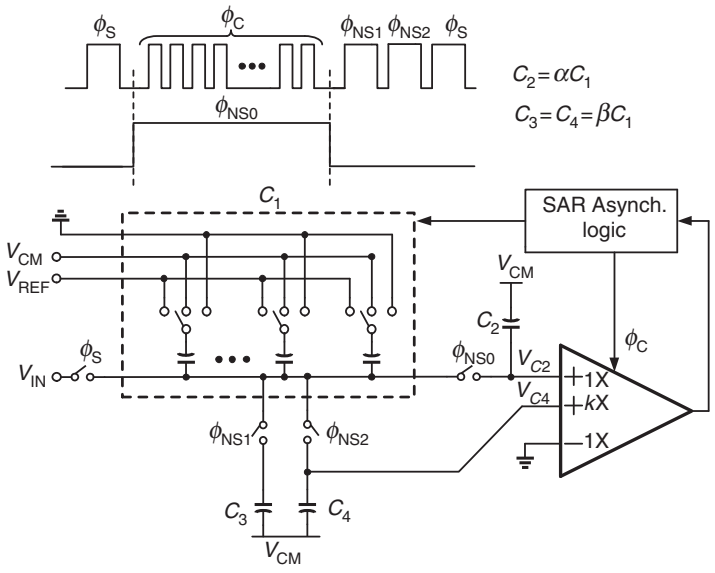



Figure 2.15 A third-order FPNS-SAR ADC described in [36] (©[2017] IEEE)

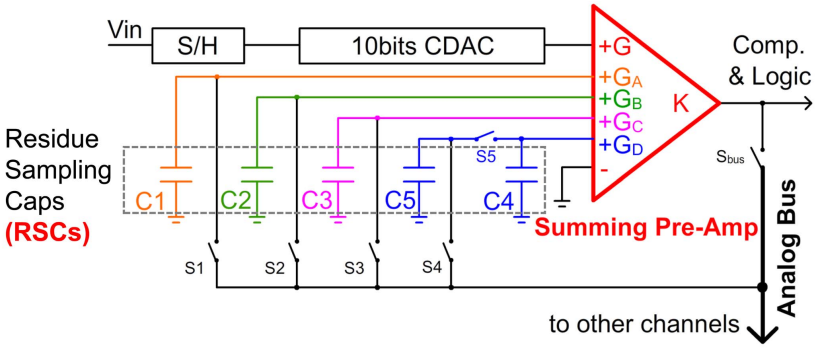



Figure 2.16 Structure of each channel of a calibration-free forth order TI-FPNS-SAR ADC [38] (©[2019] IEEE)

Another type of NS-SAR ADC is based on the passive filter and dynamic amplifier (D-Amp). The attenuation in signal is compensated using an amplifier with relaxed specification instead of multi-path complex comparators. A second-order NS-SAR ADC was presented in [39] as shown in Fig. 2.17. This work can achieve optimized NTF using a dynamic amplifier. A background calibration is also presented to mitigate the PVT variations. It achieves an ENOB of 13 bits using a 9-bit SAR ADC. This structure has the lowest leakage in the literature and uses an error feedback structure, making it simpler than other reported NS-SAR ADCs. However, the optimization technique is significantly effective in lower OSR values ($< 10$). The other limitation of this structure is the low noise-shaping order. As discussed for the

fully passive structures, increasing the noise-shaping order using higher-order filters increases the signal attenuation. This attenuation can be mitigated by boosting the gain of D-Amp, which is not an energy-efficient solution.

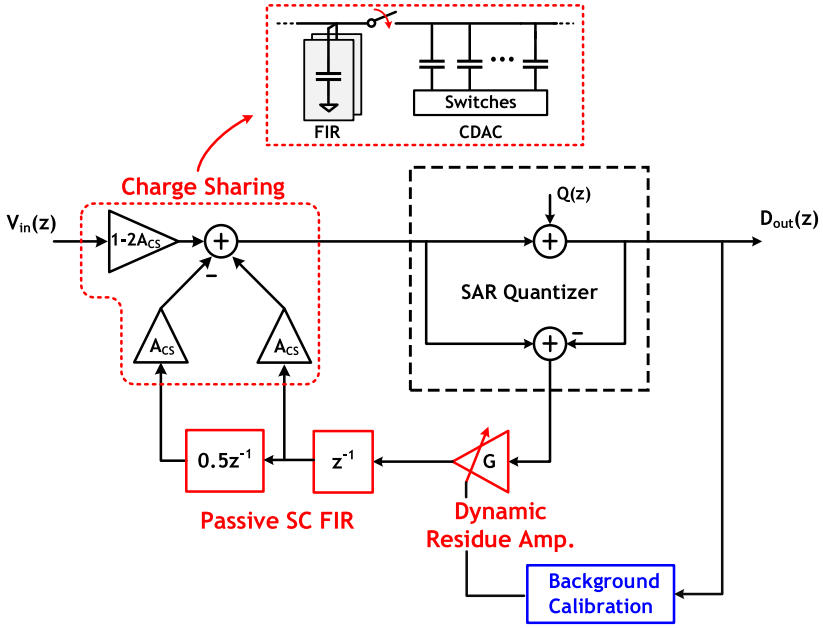



Figure 2.17 Linear model of a second-order NS-SAR ADC along with its background calibration [39] (©[2018] IEEE)

In [40], a cascaded-NS-SAR framework was presented to achieve a high-order noise-shaping, as shown in Fig. 2.18. Using a two-phase settling technique improves the efficiency of static residue amplification without degrading robustness. It also employs a ping-pong FIR filter to simplify the switching logic and reduce the charge-sharing phases.

A dynamic closed-loop residue amplifier was used for the first time to design an integrator-based NS-SAR ADC in [41]. The introduced amplifier is robust and improves the performance of the loop filter.

Recently, more complex structures have been introduced to achieve better performance in integrator-based NS-SAR ADCs. In [42], a feedback summation has been realized through capacitor-stacking along with employing buffers to mitigate the charge loss in loop-filter capacitors.

On the other hand, [43] presents an error feedback-cascaded integrator feedforward (EF-CIFF) structure that combines an error-feedback loop filter with a CIFF one. Fig. 2.20 demonstrates that this structure has combined capacitor-stacking with a $kT/C$ noise cancel-

lation technique to decrease the CDAC capacitor size. The noise cancellation technique is based on creating a replica of the sampling noise, which is utilized to cancel the original one during a conversion, as illustrated in Fig. 2.21. However, the circuit design non-idealities make the cancellation imperfect.

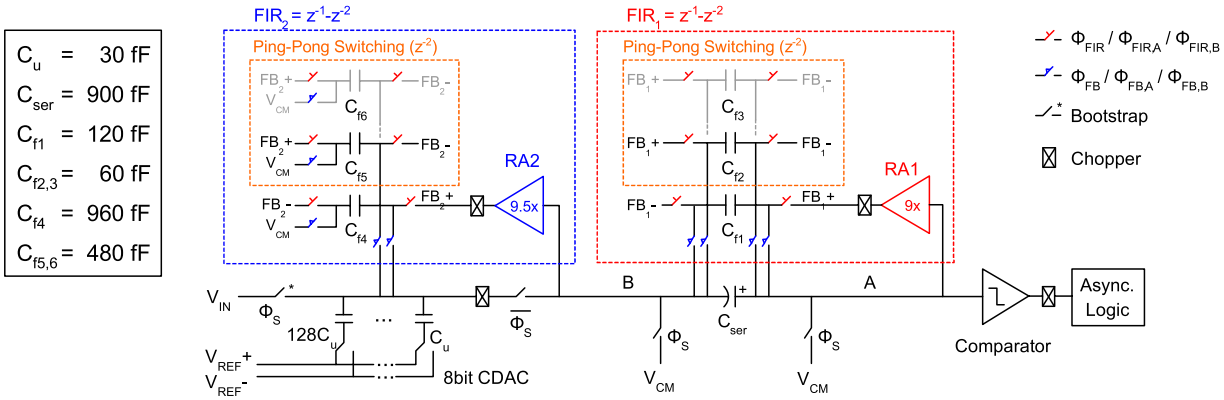



Figure 2.18 Schematic of the prototype CaNS SAR ADC presented in [40] (©[2020] IEEE)

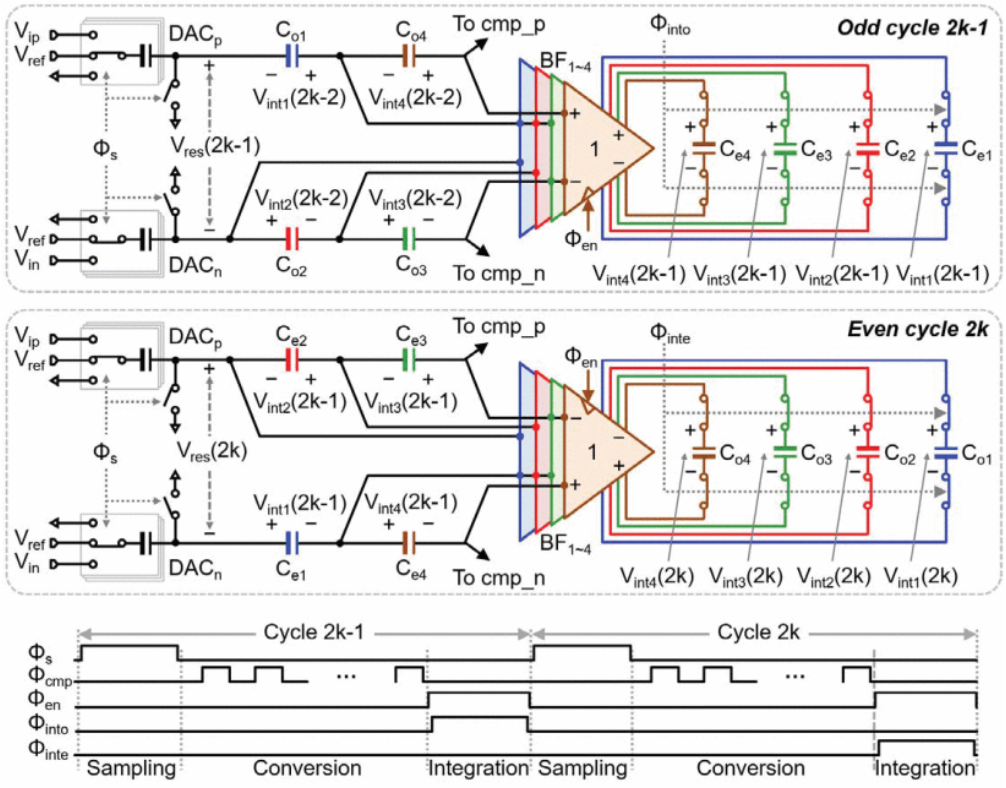



Figure 2.19 Schematic of the NS-SAR ADC using capacitor stacking and dynamic buffering presented in [42] (©[2021] IEEE)

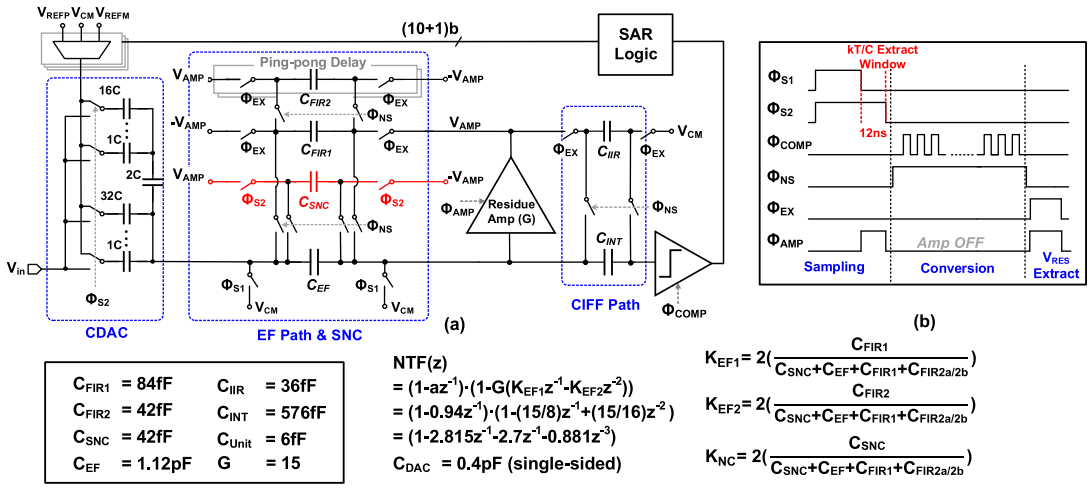



Figure 2.20 (a) Top-level schematic, and (b) overall operation timing diagram of the NS-SAR ADC presented in [43] (©[2021] IEEE)

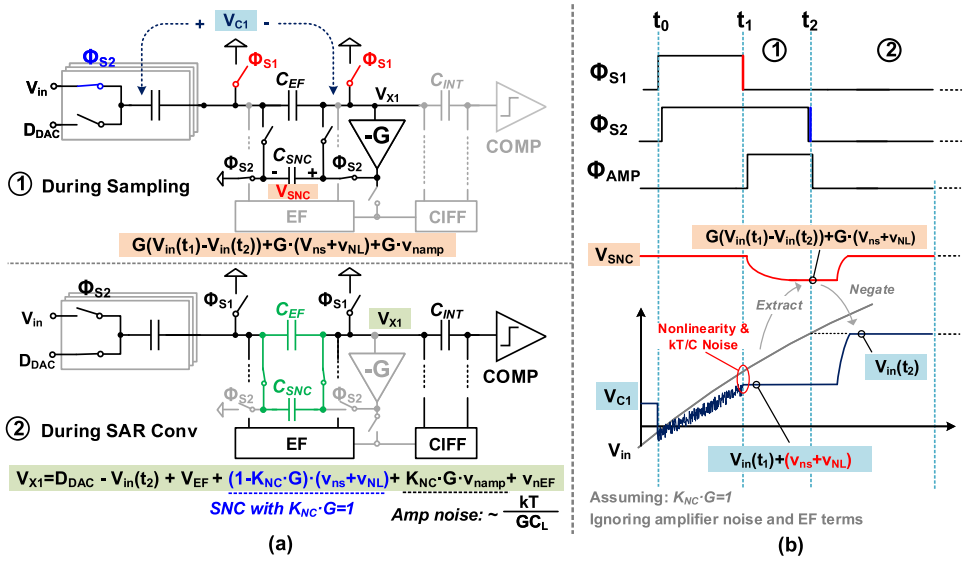



Figure 2.21 (a) Detail operation of the sampling $kT/C$ noise cancellation (SNC) technique, and (b) timing diagram with signal analysis presented in [43] (©[2021] IEEE)

In order to balance the NS sharpness, robustness and complexity, a combination of the EF and cascade-of-resonators feed-forward (CRFF) has been employed in [44] as depicted in Fig. 2.22. Also, using a push-pull buffer-in-Loop technique mitigates the sampling noise.

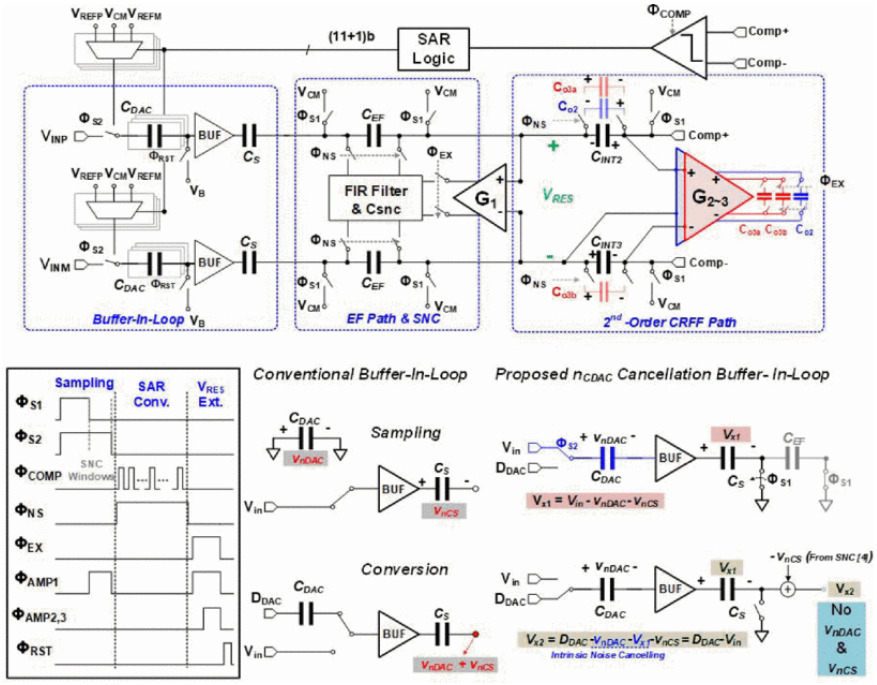



Figure 2.22 Circuit diagram of the the NS-SAR ADC and the noise-mitigated buffer-in-loop technique presented in [44] (©[2022] IEEE)

## 2.3 Summary on State-of-the-art Analog to Digital Conversion Methods

The main trade-offs in designing ADCs are discussed in this chapter. Also, a comparison between the conventional structures is presented based on the performance of the state-of-the-art ADCs. This comparison provides an overview of different types of ADCs performance that helps the designer to explore the suitable type for a specific application. Two types of high-performance ADCs, i.e., $\Delta\Sigma$-based IADCs and NS-SAR ADCs, as two options for the targeted application were studied in this chapter. Although $\Delta\Sigma$-based IADCs offer several advantages compared to $\Delta\Sigma$Ms, their bandwidth is limited by the high required OSR. The OTAs and multi-bit flash-based quantizers also degrade their power efficiency. NS-SAR ADCs mitigate similar problems in $\Delta\Sigma$ ADCs by removing OTAs and using a low-power SAR ADC as a quantizer. Therefore, they can achieve moderate resolution and high bandwidth at low OSR values, even less than 10. However, achieving NS performance better than second-order is challenging. It requires implementing higher-order filters, which cause charge loss. Employing buffers and amplifiers can degrade the power efficiency and linearity. The introduced noise cancellation methods make the ADCs structures complex. Therefore, two proposed hybrid architectures are discussed in the following sections to mitigate mentioned limitations, along with a power-bound analysis to predict the proposed ADC performance.

# CHAPTER 3 ARTICLE 1 : OTA-FREE MASH 2-2 NOISE SHAPING SAR ADC: SYSTEM AND DESIGN CONSIDERATIONS

The following sections are the reproduction of an accepted and presented article in 2020 IEEE International Symposium on Circuits and Systems (ISCAS). Also, a granted US patent based on this idea has published which is presented in the Appendix. However, CHAPTER 6 discusses the effect of non-idealities, circuit implementation, and post-layout simulation results for this proposed ADC.

- Article 1 : M. Akbari, M. Honarparvar, Y. Savaria and M. Sawan, "OTA-Free MASH 2–2 Noise Shaping SAR ADC: System and Design Considerations," 2020 IEEE International Symposium on Circuits and Systems (ISCAS), 2020, pp. 1-5,

  doi:10.1109/ISCAS45731.2020.9180832 [45].

- Akbari, Masoume, and Mohamad Sawan. "Analog-to-digital conversion device comprising two cascaded noise-shaping successive approximation register analog-to-digital conversion stages, and related electronic sensor." U.S. Patent No. 11,152,950. 19 Oct. 2021 [46].

## 3.1 Abstract

A multi-stage noise shaping (MASH) analog to digital converter (ADC) architecture is presented in this paper. This architecture combines the features of noise shaping SAR (NS-SAR) with the MASH scheme to achieve a higher order noise shaping. This ADC does not suffer from the complexity issue of conventional MASH delta sigma ($\Delta\Sigma$) structures, and it does not require operational transconductance amplifier-based analog integrators. It also exhibits a high resolution and moderate bandwidth while using a low oversampling ratio (OSR). These merits make the introduced architecture suitable for large number of applications, such as internet of things (IoT) and biomedical devices. The paper proposes MATLAB behavioral models along with macro models used to simulate the presented architecture to show the efficiency of the proposed ADC featuring a signal-to-quantization-noise ratio (SQNR) of 105 dB for an OSR of 10 at a sampling frequency of 10 MHz.

## 3.2 Introduction

Recently, there has been a demand for analog-to-digital converters (ADCs) in high-channel-density data-acquisition systems for biomedical and instrumentation applications [47, 48]. Successive approximation register (SAR) ADCs are popular in multi-channel applications because of their low latency and fast response. They have been widely used in energy-efficient applications due to their simplicity and power efficiency. SAR ADCs, however, are suffering from significant noise of the comparator, as well as extra power needed to drive a large capacitor DAC array. Therefore, such ADCs are barely used for more than 10-12 bit resolution.

Noise shaping SAR (NS-SAR) ADCs correspond to a hybrid architecture that embeds an SAR ADC in the delta sigma modulator ($\Delta\Sigma$M) structure to address the efficiency degradation of SAR ADCs [12]. This approach has several advantages. First, the comparator noise, DAC mismatch, and settling error voltage are shaped along with the quantization noise using the feedback loop filter [49]. Second, the SAR ADC operates as a multi-bit quantizer using only one comparator, and therefore the NS-SAR gains high accuracy using only a moderate OSR, which helps mitigating the power dissipation. By contrast, the flash-based quantizer in conventional $\Delta\Sigma$Ms necessitates $2^N - 1$ comparators for $N$-bit quantization, which costs power and area [39, 50]. Third, the SAR ADC quantizes the input signal and extracts the residue using the same DAC. This feature removes the error generated from the residue extraction that exists in classic error feedback (EF) $\Delta\Sigma$Ms, which also makes the structure simpler.

The first NS-SAR ADC has been introduced in [12], in which the noise of the comparator is decoupled from the ADC. However, using an operational transconductance amplifier (OTA)-based integrator, as well as noise contribution of the finite impulse response (FIR) filter, limits its performance. Therefore, a fully passive noise-shaping SAR (FPNS-SAR) ADC has been introduced in [32]. The idea is to feed the residue voltage of the SAR ADC back to the input voltage to shape the quantization noise in each conversion cycle. It is implemented using a few capacitors that transfer the error signal using charge sharing. Consequently, it achieves higher resolution using smaller capacitances compared to that of conventional SAR ADCs [32]. The architectures proposed in [33–36] tried to optimize the zero location of the noise transfer function (NTF) and to increase the noise shaping order in a FPNS-SAR. However, the main concern is the attenuation of the error signal in lossy fully passive filters, which degrades the dynamic range [39]. This effect was partially compensated using a multi-input comparator with different input gains, which provides multiple feedback paths for the error signal. Dynamic amplifiers (D-Amp), combined with a passive filter, were then used

to address this issue [39, 51]. The D-Amp is not as complex as the amplifiers used in the conventional $\Delta\Sigma$Ms.

Recently, a fourth order time interleaved NS-SAR ADC has been introduced in [38]; however, most prior art solutions are limited to lower order noise-shaping. Increasing the order of the passive filter enhances the order of noise-shaping [36]. However, it raises losses in the filter, which leads to increase the number of comparator inputs that makes the FPNS-SAR structure more complicated. Boosting the gain of an embedded D-Amp to compensate for signal attenuation is possible, but it is not a power-efficient solution. The MASH topology is a well-known solution to obtain higher-order modulators with low order and stable $\Delta\Sigma$Ms. However, the extra required hardware to extract the error of the first stage and feed it to the next stage makes MASH $\Delta\Sigma$ structures complicated. For instance, a DAC must be used to convert the output signal to an analog signal that can be subtracted from the quantizer input voltage. This process may make the design less accurate.

In this paper, we propose a MASH 2-2 structure based on an NS-SAR ADC that has less complexity. That mitigates concerns about inaccuracies caused by extra hardware when compared with previously reported solutions, since the analog error signal of the first stage exits on the SAR DAC at the end of each conversion. A fourth-order noise shaping performance is obtained by cascading two second-order NS-SAR ADCs with no need for power-hungry OTAs. The remainder of this article is organized as follows. The proposed topology is described in Section 3.3. Behavioral model simulation results, as well as macro-model simulation results are presented in Section 3.4. Conclusions are drawn in Section 3.5.

## 3.3 Proposed Multi Stage Noise Shaping SAR ADC

### 3.3.1 System Level Implementation

The block diagram of the proposed MASH NS-SAR structure is shown in Fig. 3.1. Each stage is based on an error feedback NS-SAR ADC. It consists of a SAR ADC used as a quantizer and a second-order FIR filter [39]. The FIR filter is implemented using delay blocks in the feedback path. The signal attenuation factors resulting from the injection of the error to the input are expressed by gain blocks $F_1$ and $F_2$ for the input signal and FIR output signals, respectively. The gain $G$ represents the D-Amp gain.

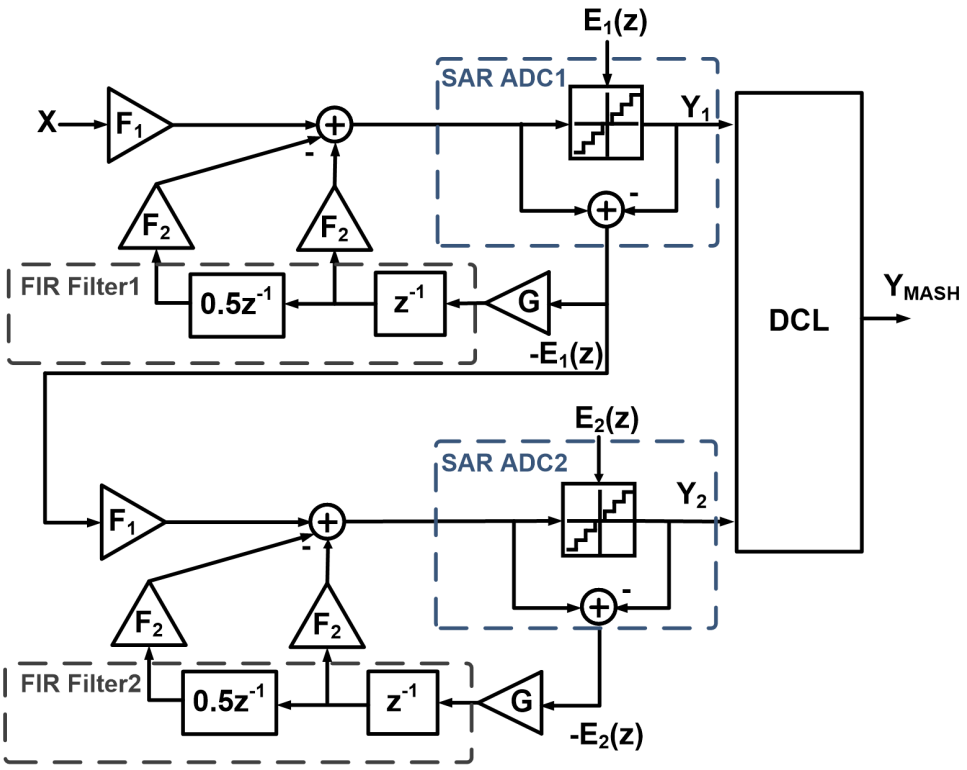



Figure 3.1 System level implementation of the proposed MASH NS-SAR ADC

The output of the first stage is expressed with (3.1) where NTF and STF stand for the noise transfer function and the signal transfer function.

$$Y_1(z) = STF_1 \cdot \ X(z) + NTF_1 \cdot E_1(z) \tag{3.1}$$

$$STF_1 = F_1 \tag{3.2}$$

$$NTF_1 = 1 - G \cdot \ F_2 z^{-1} + 0.5 \cdot \ G \cdot \ F_2 z^{-2} \tag{3.3}$$

where $F_1$ and $F_2$ are determined using the ratio of C-DAC and the value of FIR filter capacitors as discussed in the following section. The coefficients $F_1$, $F_2$ and $G$ are set to 0.875, $\frac{1}{16}$ and 32 respectively, resulting in $NTF_1 = (1 - z^{-1})^2$. Using a suitable digital cancellation logic (DCL), the quantization noise of the first stage is canceled, and the overall output is given by (3.4)

$$Y_{MASH}(z) = X(z) + \frac{1}{0.875^2} \cdot (1 - z^{-1})^4 \cdot E_2(z) \tag{3.4}$$

where $X(z)$ is the input signal of the ADC and $E_2(z)$ is the quantization noise of the second stage.

### 3.3.2 Macro-model Implementation

The macro-model implementation of the proposed topology and its timing diagram are shown in Fig. 3.2 and Fig. 3.3, respectively. Since the two stages are similar, the second stage is not depicted due to a lack of space, and a single-ended topology is shown for simplicity. The SAR ADC performs as an 8-bit quantizer. It consists of a 9-bit capacitance DAC array, a logic binary search module, and a binary to decimal converter to provide an analog equivalent of the output signal.

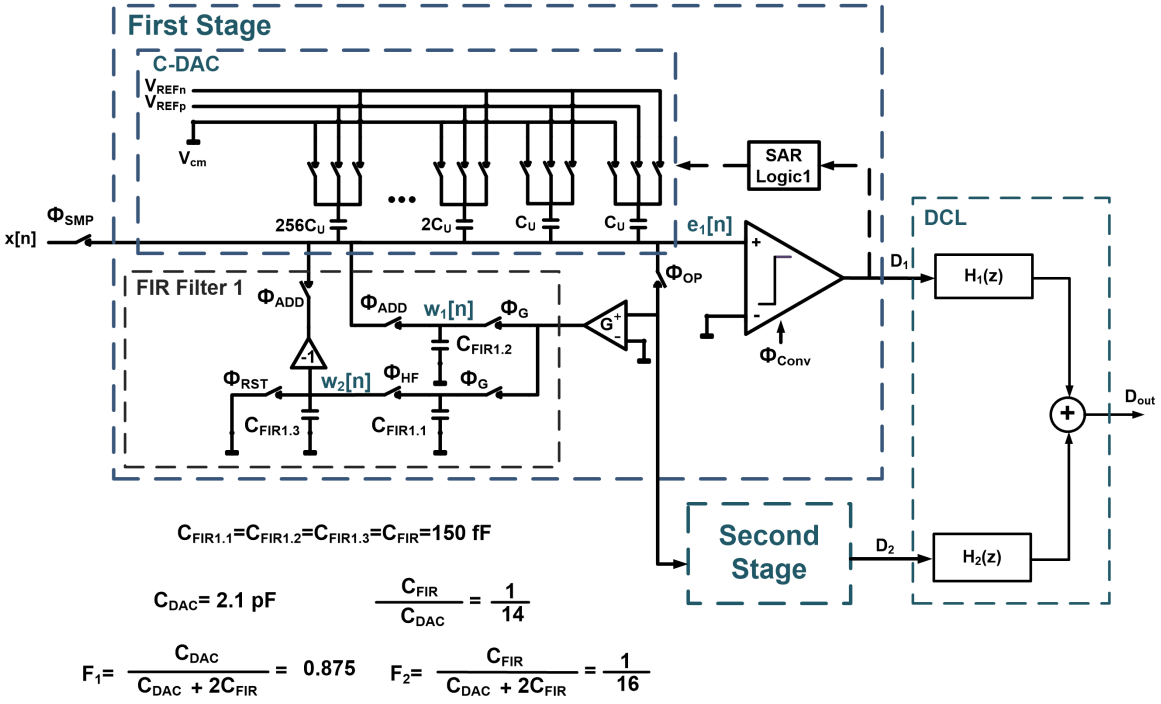



Figure 3.2 Macro-model implementation of the proposed MASH NS-SAR

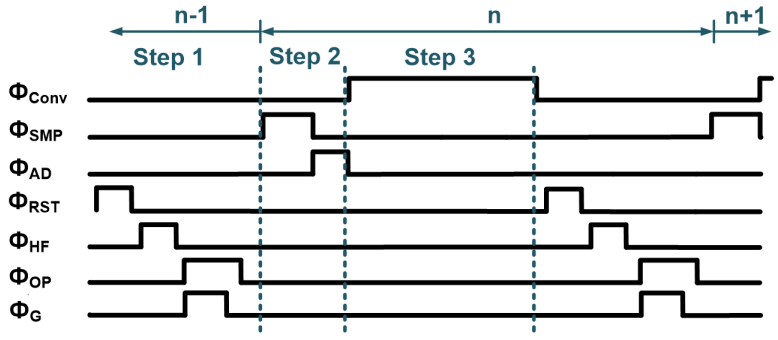



Figure 3.3 Timing diagram for the macro-model implementation of the proposed ADC

According to the timing diagram, the operation in each cycle includes three main steps, which are explained as follows; 1) Processing the residue voltage of the previous cycle by the FIR filter and D-Amp, 2) Sampling the input signal and injecting the processed residue voltage to the input voltage, 3) Digitizing the input signal along with the shaped residue voltage and producing the new residue voltage.

The transfer function of the FIR filter is $H_F(z) = z^{-1} - 0.5z^{-2}$, which is implemented using a switched capacitor circuit that consists of three equally sized capacitors. At the beginning of the $(n-1)$-th cycle, the amplified residue voltage of the previous cycle ($G.e_1[n-2]$) is on $C_{FIR1.1}$ and $C_{FIR1.2}$ capacitors. The $C_{FIR1.3}$ gets reset first, and then it stores half of the voltage of $C_{FIR1.2}$ ($0.5G.e_1[n-2]$). This operation realizes the second term of $H_F(z)$. Then, the dynamic amplifier is activated with $\phi_{OP}$ that charges $C_{FIR1.1}$ and $C_{FIR1.2}$ to the $G.e_1[n-1]$ voltage. In order to realize the second term of $H_F(z)$, $C_{FIR1.1}$ holds its charge and shares it with $C_{FIR1.3}$ and C-DAC in the second step. Considering the D-Amp gain ($G = 32$), the FIR filter output voltages are $w_2[n] = 32e_1[n-1]$ and $w_3[n] = 16e_1[n-2]$ at the end of the first step. The gain of -1 is achieved by employing the cross-coupled connection in a fully-differential design. In the second step, the C-DAC samples the input signal and then connects to $C_{FIR1.2}$ and $C_{FIR1.3}$. Figure 3.2 also shows the definition of attenuation factors that result from this step. Setting $\frac{C_{DAC}}{C_{FIR}}$ to 14 results in adding the processed residue voltages to the input signal as expressed in (3.5)

$$x'[n] = 0.875 \cdot \ x[n] + 2 \cdot \ e_1[n-1] - e_1[n-2] \tag{3.5}$$

where the $x'[n]$ is the voltage on the C-DAC at the beginning of the third step of the ADC operation. The $e_1[n]$ signal after digitizing the $x'[n]$ signal can be expressed as follows

$$e_1[n] = 0.875x_1[n] - D_1[n] + 2e_1[n-1] - e_1[n-2] \tag{3.6}$$

The overall operation of both stages of the MASH structure is the same. At the end of a conversion cycle, the sample-and-hold transfers the error signal of the first stage, i.e. $e_1[n]$ to the next stage ($\phi_{OP}$). This process delivers the error with one period delay, which must be considered in the DCL design.

The main concern in the design of MASH architectures is the noise leakage caused by mismatch between the analog loop filter and the digital cancellation logic. This error is mainly due to the OTA performance in conventional $\Delta\Sigma$Ms, or resonators gain coefficient variation in VCO-based $\Delta\Sigma$Ms [52, 53]. In the proposed MASH topology, any variations in D-Amp gain and the ratio between C-DAC and FIR capacitors change the NTF coefficients. How-

ever, this issue can be addressed by applying a background calibration [39], which controls the parameter of $G$ to compensate variations in the capacitor ratio.

### 3.4 Simulation Results

Behavioral simulations in MATLAB/SIMULINK, as well as macro-model simulations were carried out to demonstrate the effectiveness of the proposed ADC.

The impact of two design parameters i.e. OSR and SAR number of bits were first characterized with MATLAB. A behavioral time-domain model was then developed in the same environment. Finally, macro-model simulations were performed to check the feasibility of the proposed architecture. The behavioral model was implemented as a single-ended model in SIMULINK. The 9-bit SAR ADC that was modeled includes a comparator, a DAC, and some SAR logic. The DAC is modeled using gain blocks instead of capacitors, and the SAR logic is modeled based on logic gate models. Since there is no capacitor to store the residue voltage in this model, the error is extracted using the subtraction operation of the comparator block input and the DAC output. In Fig. 3.4, the NTF of the proposed scheme is compared to the NTF plots of three prior state-of-the-art works. For instance, in [36] and [38] the FPNS-NS SAR method is exploited together with a multi-input comparator in their respective structure. However, [39] and our proposed ADC use a D-Amp and a standard two-input comparator. The NTFs of two first mentioned ADCs show that they do not suppress efficiently the quantization noise at lower frequencies, while the third and fourth-order noise-shaping do work at higher frequencies. Although [39] is a second-order NS-SAR structure; it yields a better performance at low frequencies compared with those of proposed in [36] and [38]. It is worth mentioning that the improvement achieved in [39] using zero optimization of the NTF is significant for OSRs smaller than 10. As Fig. 3.4 shows, in theory the proposed ADC improves the NTF for low frequency values by more than 20 dB when compared with prior works.

The SQNR of the first stage and the overall output of the proposed ADC is presented in Fig. 3.5(a). This was evaluated with the system model discussed above, for different OSR values, when using 9-bit SAR ADCs. This figure shows the efficiency of the proposed structure to improve the SQNR of single loop NS-SAR ADCs. While the SQNR values of both stages increase with the OSR, the improvement achieved by the MASH configuration is even more significant with higher OSRs. However, it narrows the achieved bandwidth and also imposes using high-speed SAR ADCs.

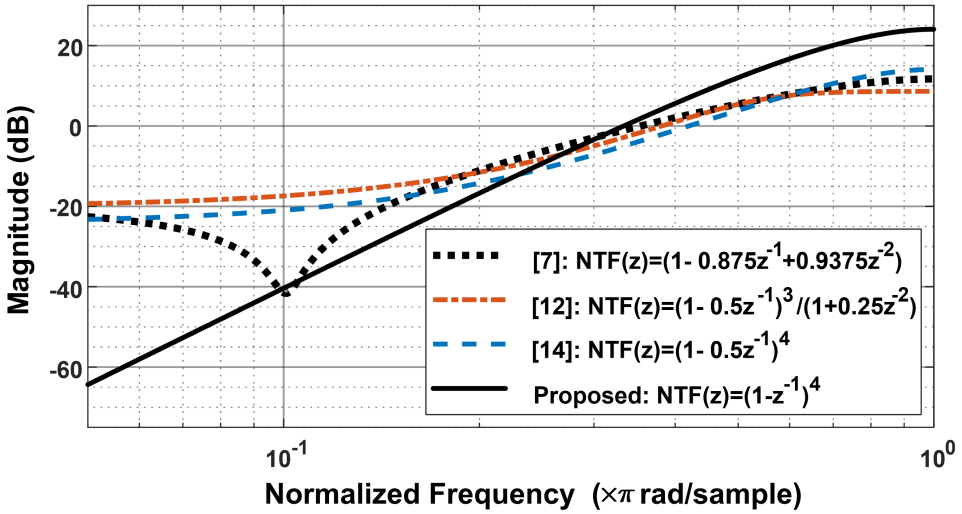
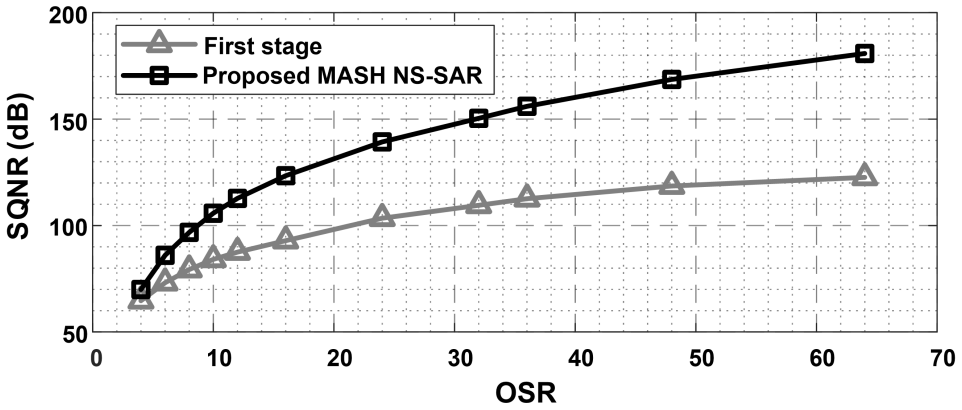
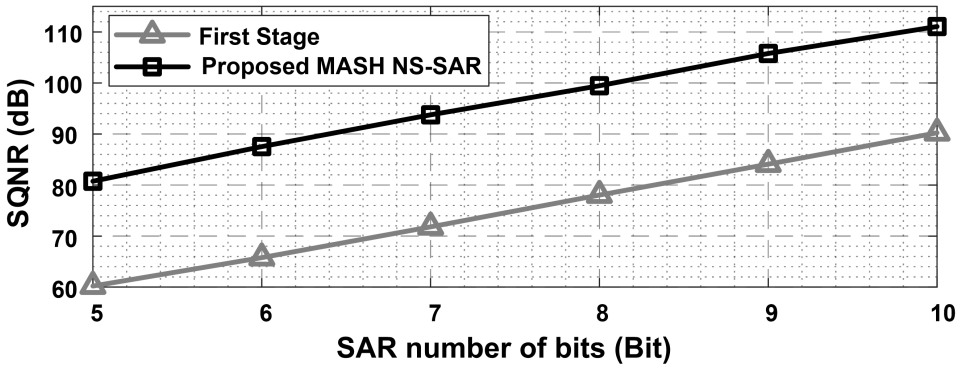



Figure 3.4 NTF system level comparison




(a)




(b)

Figure 3.5 Design parameters simulations: (a) SQNR versus OSR for normalized bandwidth and 9-bit SAR ADC, (b) SQNR versus SAR number of bits for OSR of 10

The linear relation between the SQNR and the SAR number-of-bits with an OSR of 10 is also depicted in Fig. 3.5(b). Therefore, in order to achieve a high resolution and a moderate bandwidth, using SAR ADCs with relaxed specifications, an OSR of 10 with 9-bit SAR ADC is utilized for the macro model simulations.

Figure 3.6 shows the effect of the FIR capacitors mismatch on the SQNR of the proposed ADC. Focusing on the expected mismatch for capacitors based on modern technologies (less than 0.2 percent [39]), our simulation results predict a 2 dB degradation in SQNR (dashed line). The FIR capacitors mismatch, itself, causes a mismatch between analog and digital (DCL) parts, which can be mitigated using calibration or sturdy MASH (SMASH) techniques. According to the solid line, these techniques can decrease the SQNR degradation to 0.5 dB.

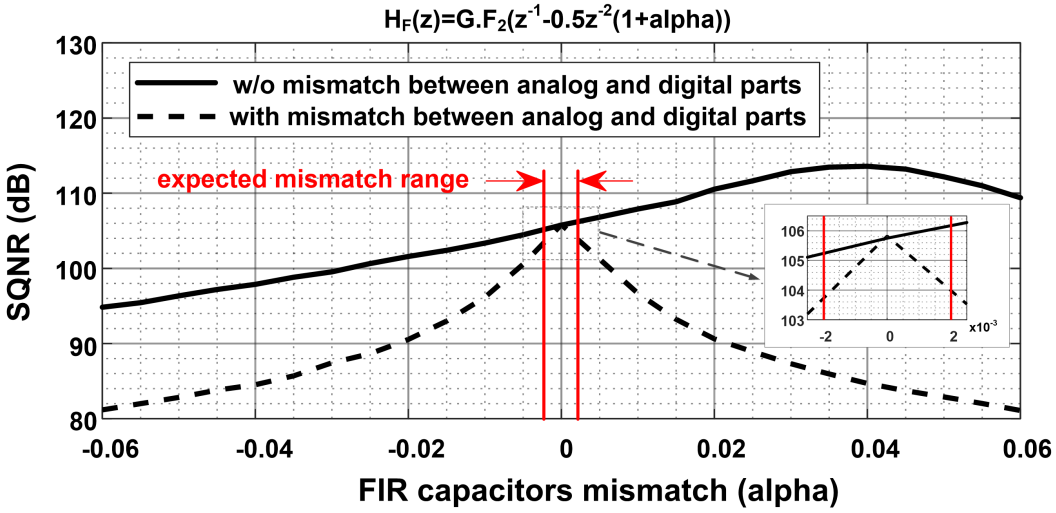
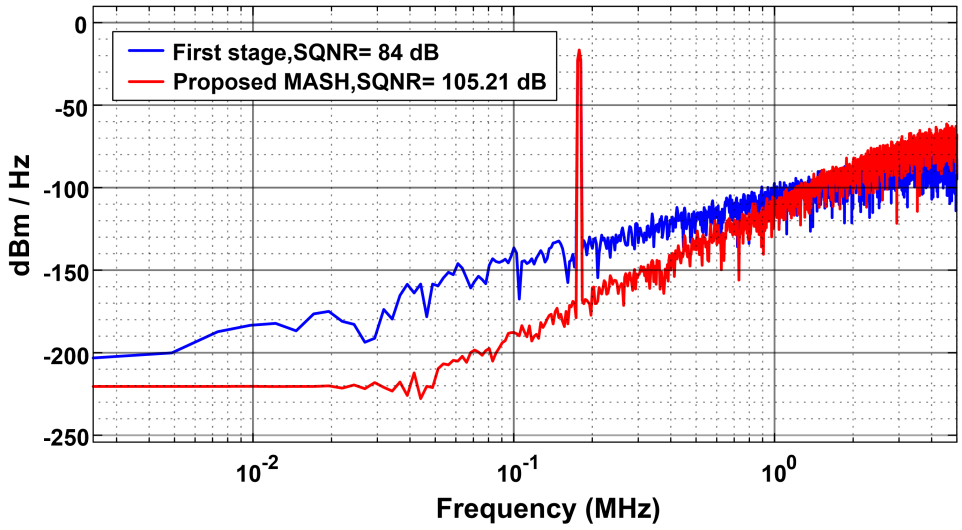


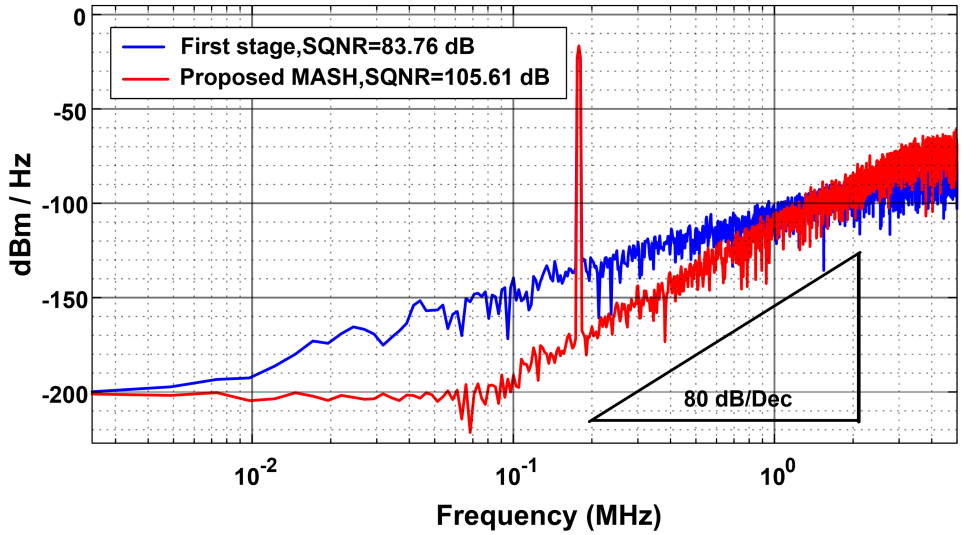

Figure 3.6 SQNR versus FIR capacitors mismatch

The proposed MASH NS-SAR ADC of Fig. 3.2 was implemented and simulated using Cadence SPECTRE. VerilogA blocks are employed to represent the switches, comparators, and clock generators. The SAR logic is realized using standard logic cells. The FIR filters are also implemented using switched capacitor circuits. The output of both stages is post-processed in MATLAB. Figure 3.7 shows the power spectral density of the ADC for both MATLAB/SIMULINK behavioral and macro-model simulations. The proposed ADC is simulated for an OSR of 10 over a 500 kHz signal bandwidth. The input signal magnitude applied to the ADC is -8 dBFS. As shown, there is an excellent agreement between the two simulations. The second-order and the fourth-order noise-shaping for the first and second stages are shown respectively.

The performance summary of the proposed ADC is listed in Table 3.1. The specifications of the proposed architecture compared to some prior works is also summarized in Table 3.2. It shows that the proposed architecture can provide the largest reported noise shaping order by using simpler comparator structure.




(a)




(b)

Figure 3.7 Output spectrum of the proposed MASH NS-SAR: (a) Behavioral simulation, (b) Macro-model simulation

Table 3.1 ADC Specifications

| Specification | Value |
|---|---|
| Resolution | 16 bit |
| Bandwidth | 500 kHz |
| SAR ADC Frequency | 200 MHz |
| Sampling frequency | 10 MHz |
| Signal-to-quantization noise ratio (SQNR) | 105 dB |

Table 3.2 Comparison table

| Specifition | JSSC 2018 [39] | Electron. Lett. 2017 [36] | JSSC 2019 [38] | JSSC 2019 [37] | Electron. Lett. 2018 [54] | This work |
|---|---|---|---|---|---|---|
| Architecture | Optimized NS-SAR | FPNS-SAR | TINS-SAR | FPNS-SAR | FPNS-SAR | MASH NS-SAR |
| D-Amp | Yes | No | No | No | No | Yes |
| NTF order | 2 | 3 | 4 | 2 | 3 | 4 |
| Comparator | 2-input | 3-input | 6-input | 4-input | 2-input | 2-input |
| Core DAC | 9-bit | 10-bit | 10-bit | 9-bit | 8-bit | 9-bit |

## 3.5 Conclusion

An OTA-free MASH ADC was proposed in this paper. It offers a fourth-order noise-shaping NTF better than the prior work exploiting a similar order. Furthermore, this MASH ADC does not suffer from the complexity caused by additional hardware in $\Delta\Sigma$-based MASH architectures. The capability of achieving high resolution and moderate bandwidth performance without increasing the OSR to high values have been verified by behavioral and macro-model simulation of the proposed ADC. However, the key design parameters, such as OSR and SAR bit resolution, can be optimized according to the targeted specifications.

# CHAPTER 4 ARTICLE 2 : OTA-FREE MASH TWO-STEP INCREMENTAL ADC BASED ON NOISE SHAPING SAR ADCS

The following sections are the reproduction of an accepted and presented article in 2020 18th IEEE International New Circuits and Systems Conference (NEWCAS).

- M. Akbari, M. Honarparvar, Y. Savaria and M. Sawan, "OTA-Free MASH Two-Step Incremental ADC based on Noise Shaping SAR ADCs," 2020 18th IEEE International New Circuits and Systems Conference (NEWCAS), 2020, pp. 138-141, doi: 10.1109/NEWCAS49341.2020.9159802 [55].

## 4.1 Abstract

An OTA-free two-step incremental ADC (IADC) based on the noise-shaping successive approximation register (NS-SAR) topology is presented in this paper. During the first step, the ADC is configured as a multi-stage noise-shaping (MASH) 2-2 NS-SAR incremental ADC. During the second step, the first stage of the ADC is re-used to enhance the resolution of the incremental ADC. Employing 4-bit SAR ADCs as core quantizers, along with re-using parts of the hardware, can make this structure area and power-efficient. Simulation results, performed with MATLAB/SIMULINK, demonstrate the efficiency of the proposed ADC featuring a signal to quantization noise ratio (SQNR) of 150 dB, with an oversampling rate (OSR) of 48 over a 250 kHz bandwidth.

## 4.2 Introduction

Incremental analog-to-digital converters (IADCs) offer a sample by sample conversion, which enables them to be multiplexed between several channels. Compared to the delta-sigma modulators ($\Delta\Sigma$Ms), IADCs benefit from fewer idle tones, lower latency, and simpler decimation filters [28]. Higher-order single-loop and multi-stage noise-shaping (MASH) IADCs have been presented in the literature [4, 56]. To further improve their power efficiency, multi/two-step IADCs have also been proposed, where part of the ADC is re-used to boost the overall resolution of the ADC [28, 30]. However, all the above-mentioned topologies are suffering from the following drawbacks. First, higher-order single-stage IADCs suffer from instability, such that a single-stage IADC with an order of 3 or more is rarely used. Second, single-stage, MASH, and multi-step IADCs still need power-hungry operational transconductance amplifiers (OTAs) although multi-step IADCs are taking advantage of lowering the number of

OTAs. Third, a multi-bit quantizer, e.g., FLASH ADC, is needed to meet the dynamic range (DR) requirements for a given oversampling rate (OSR). Therefore, linearization techniques, e.g., dynamic element matching (DEM), are required [5].

Noise-shaping successive approximation register (NS-SAR) ADCs were shown to be a promising approach to take advantage of both $\Delta\Sigma$Ms and SAR ADCs [12]. In such topology, the SAR ADC is either used as a multi-bit quantizer inside the loop filter of a $\Delta\Sigma$M or it is used to form an error feedback (EF) topology [36, 38, 39]. This eases the implementation of the multi-bit quantizer and the latter no longer requires power-hungry OTAs to realize the loop-filter. However, the NS-SAR ADCs suffer from any loss in the passive filters that limits their noise-shaping order [50].

To address the aforementioned drawbacks, an OTA-free MASH two-step NS-SAR IADC is proposed in this paper. In the proposed topology, a MASH NS-SAR IADC is utilized during the first step. The first stage of the proposed architecture is then employed to further process the residue and improve the resolution of the overall ADC. The remainder of this paper is organized as follows. Section 4.3 is divided into two parts; the first part describes the system-level structure of the proposed MASH two-step IADC. It is based on a second-order NS-SAR IADC which is also briefly discussed in this part. The macro-model implementation of the proposed architecture is shown in the second part. MATLAB/SIMULINK simulation results for the behavioral model of proposed ADC are presented in Section 4.4. Section 4.5 draws the conclusions from this paper.

## 4.3 Proposed Architecture

### 4.3.1 System Level Implementation

Figure 4.1 shows the block diagram of the second-order NS-SAR IADC, which is the core of the proposed ADC. It is based on the error-feedback (EF) topology with a second-order passive FIR filter in the feedback path. Its operation begins with a global reset. In each cycle, the FIR filter processes the residue voltage of the previous cycle, $E[i-1]$ ($i$: time index). This provides $W_1[i] = -E[i-1]$ and $W_2[i] = -E[i-2]$ at the outputs of the FIR filter, then summed with the input voltage, $U[i]$. The SAR ADC digitizes this voltage and produces the residue voltage, $E[i]$, which involves quantization noise, comparator thermal noise, digital-to-analog converter (DAC) thermal noise and settling time error, on the capacitance DAC array (C-DAC) [39]. Therefore, a second-order noise transfer function (NTF) expressed as $(1-z^{-1})^2$ is realized. This operation continues for $M$ cycles, and then the reset signal ($RST$) erases the memory elements to prepare the ADC for the next conversion. The time-domain

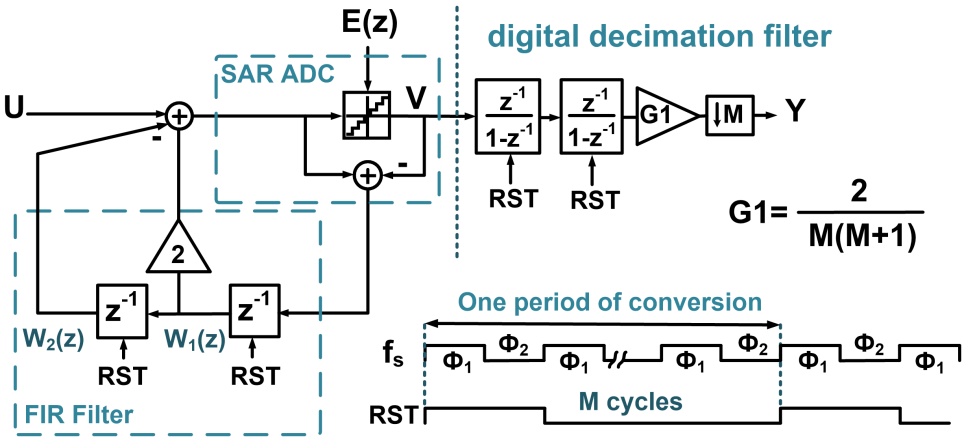



Figure 4.1 Block diagram of the second-order NS-SAR IADC

behavior of the architecture, shown in Fig. 4.1, is described by (4.1):

$$U[i] - W_2[i] + 2 \cdot \ W_1[i] + E[i] = V[i] \tag{4.1}$$

writing this equation for $M$ cycles confirms that the FIR output accumulates the error [1]. $W_2[M]$, which is a delayed version of the residue signal, is used in the proposed MASH two-step NS-SAR IADC.

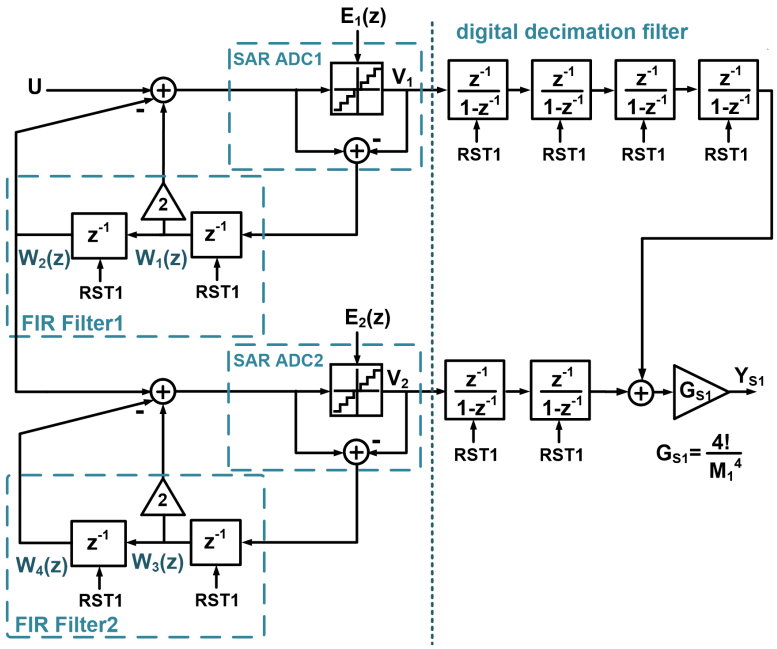
$$W_2[M] = \sum_{k=1}^{M-1} \sum_{i=1}^{k-1} U[i] - \sum_{k=1}^{M-1} \sum_{i=1}^{k-1} V[i] \tag{4.2}$$

The overall quantization error and SQNR expressions for the second-order NS-SAR IADC with an $L$-level quantizer is derived as in [1, 28].

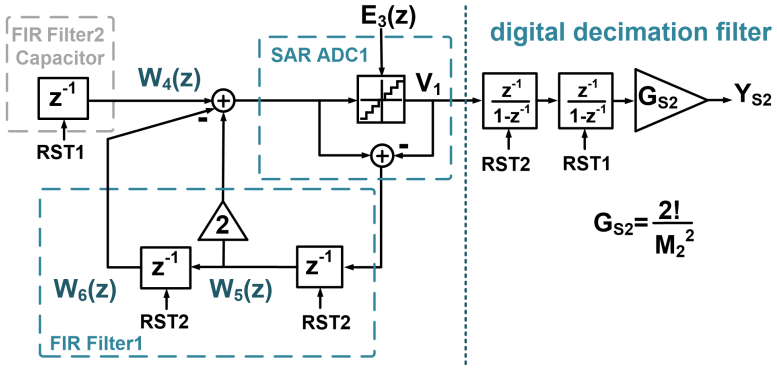
$$E = \frac{V_{FS}}{L-1} \cdot \frac{2!}{M \cdot (M+1)} \tag{4.3}$$

$$SQNR = 40 \cdot \log(M) + 20 \cdot \log(L-1) - 6 \tag{4.4}$$

Using advantages of the proposed architecture, depicted in Fig. 4.1, a MASH two-step NS-SAR IADC is proposed, as shown in Fig. 4.2. The MASH structure avoids increasing the quantization noise leakage, caused by the FIR filter capacitors in the higher-order single loop NS-SAR ADCs.




(a)

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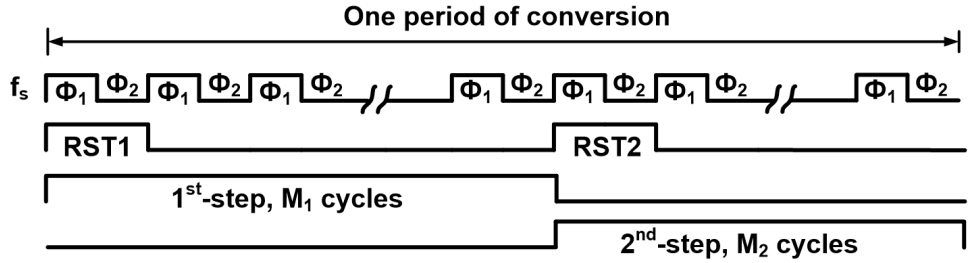



(c)

Figure 4.2 Proposed MASH two-step NS-SAR IADC: (a) Operation of the proposed ADC during the first step, (b) Operation of the proposed ADC during the second step, (c) Timing diagram

The presented NS-SAR IADC is utilized in each stage of the MASH for the first step operation of the ADC, and then the first stage is re-used in the second step. Therefore, the proposed structure achieves the sixth order noise-shaping using only two SAR ADCs, and without being limited by the OTA dependent non-idealities e.g. finite-gain, finite bandwidth, finite slew-rate, etc.

As shown in Fig. 4.2, each conversation period is split into two cycles i.e. $M_1$ and $M_2$. The overall operation of each stage is similar to what has been described for the NS-SAR IADC. In the first step, the $W_2[i]$ signal is used as the input of the second stage in each cycle. The overall error of the incremental MASH 2-2 (MASH NS-SAR IADC) structure ($W_4[M_1] = -E_2[M_1 - 2]$), after $M_1$ cycles, is expressed as follows:

$$W_4[M_1] = \sum_{k=1}^{M_1-1}\sum_{i=1}^{k-1} W_2[M_1] - \sum_{k=1}^{M_1-1}\sum_{i=1}^{k-1} V_2[i] \tag{4.5}$$

so the overall output of the first step is given by:

$$\begin{aligned} Y_{S_1}[M_1] &= \widetilde{U} + \frac{4!}{M_1^4}E[M_1] \\ &= \frac{4!}{M_1^4}\cdot\Big(\sum_{l=1}^{M_1-1}\sum_{j=1}^{l-1}\sum_{k=1}^{j-1}\sum_{i=1}^{k-1} V_1[i] + \sum_{k=1}^{M_1-1}\sum_{i=1}^{k-1} V_2[i]\Big) \end{aligned} \tag{4.6}$$

where $\widetilde{U}$ is the average of the input signal, $U$, when it does not change significantly during each conversion period.

At the end of $M_1$ cycles, the first stage is reset by $RST2$, but the second stage holds the $W_4[M_1]$. In the second step, the first stage of the MASH is re-used to further digitize the $W_4[M_1]$. Expressions (4.7) and (4.8) show the resulted error and output signal of the second step after $M_2$ cycles.

$$W_6[M_2] = \sum_{k=1}^{M_2-1}\sum_{i=1}^{k-1} W_4[M_1] - \sum_{k=1}^{M_2-1}\sum_{i=1}^{k-1} V_3[i] \tag{4.7}$$

$$Y_{S2}[M_2] = W_4[M_1] - \frac{4!}{M_1^4}\cdot\frac{2!}{M_2^2}W_6[M_2] = \frac{2!}{M_2^2}\sum_{i=1}^{k-1} V_3[i] \tag{4.8}$$

so the overall quantization error of the proposed circuit can be expressed as follows:

$$E_{two-step} \simeq \frac{V_{FS}}{L-1}\cdot\frac{4!}{M_1^4}\cdot\frac{2!}{M_2^2} \tag{4.9}$$

As described in [28], a similar procedure can be applied in order to optimize $M_1 : M_2$ to maximize the SQNR for $M = M_1 + M_2$ as expressed in (4.10)

$$SQNR_{opt} \simeq 6 \cdot 20 \cdot \log(M) + 20 \cdot \log(L-1) - 66.8 \tag{4.10}$$

where $M$ is the OSR of the IADC and $L = 2^B + 1$ is the number of quantization levels for a $B$-bit quantizer. As expressed in (4.10), increasing the number of quantizer bits by 1, results in a 6 dB SQNR improvement. This increase in the number of quantization bits can be achieved by doubling the number of comparators in flash-based quantizers; however, a SAR ADC offers multi-bit quantization using only one comparator, which can make the proposed topology power-efficient.

### 4.3.2 Macro-model Implementation

Figure 4.3 shows the macro-model implementation of the proposed ADC. Each stage includes a 4-bit SAR ADC with a second-order FIR filter. The gain $G = 32$ is used to amplify the error signal before being shaped by the FIR filter. This gain compensates the signal attenuation when the capacitors transfer the residue signal. Controlling this gain can also be used for calibrating the ADC against process, voltage, and temperature (PVT) variations [39]. The shaped error is then injected as an input signal by using the charge sharing between FIR capacitors and C-DAC with a coefficient of $F = \frac{1}{16}$ (as shown in Fig. 4.3). Consequently, the voltage on the $C_{F1.3}$ at the end of the SAR conversion is $W_2'[i] = 16E_1[i-2]$.

A replica path copies and holds the $W_2'[i]$ signal on $C_{R.3}$ in each SAR conversion cycle to be used in the second stage. In the sampling phase of the second stage, $\phi_{SMP2}$, the capacitance DAC array, C-DAC2, is discharged first and is then connected to the replica path for charge sharing operation ($\phi_{AD2}$). This operation generates the $E_1[i]$ signal on C-DAC2, which is processed by the second stage as similarly described for the first stage. The role of $C_{R.1}$ is to provide the required coefficient in this charge sharing phase. It should be noted that the overall error of the MASH 2-2 structure (first step) is $W_4'[M_1] = 16E_2[M_1 - 2]$ that is collected in $C_{F2.3}$ after $M_1$ cycles.

In the second step, the first stage is re-used similarly. At the end of $M_1$ cycles, FIR Filter1 capacitors should be discharged with $RST2$. However, the second stage is not reset and it holds $W_4'[M_1]$, so it is not required to have a replica path. The sampling phase is similar to that of the second stage in the first step. However, we also discharge $C_{F2.1}$ along with the C-DAC1 in order to provide the proper coefficient in the charge sharing phase ($\phi_{AD3}$). This process results in $E_2[M_1]$ on the C-DAC1 capacitor, which is digitized by the second step.

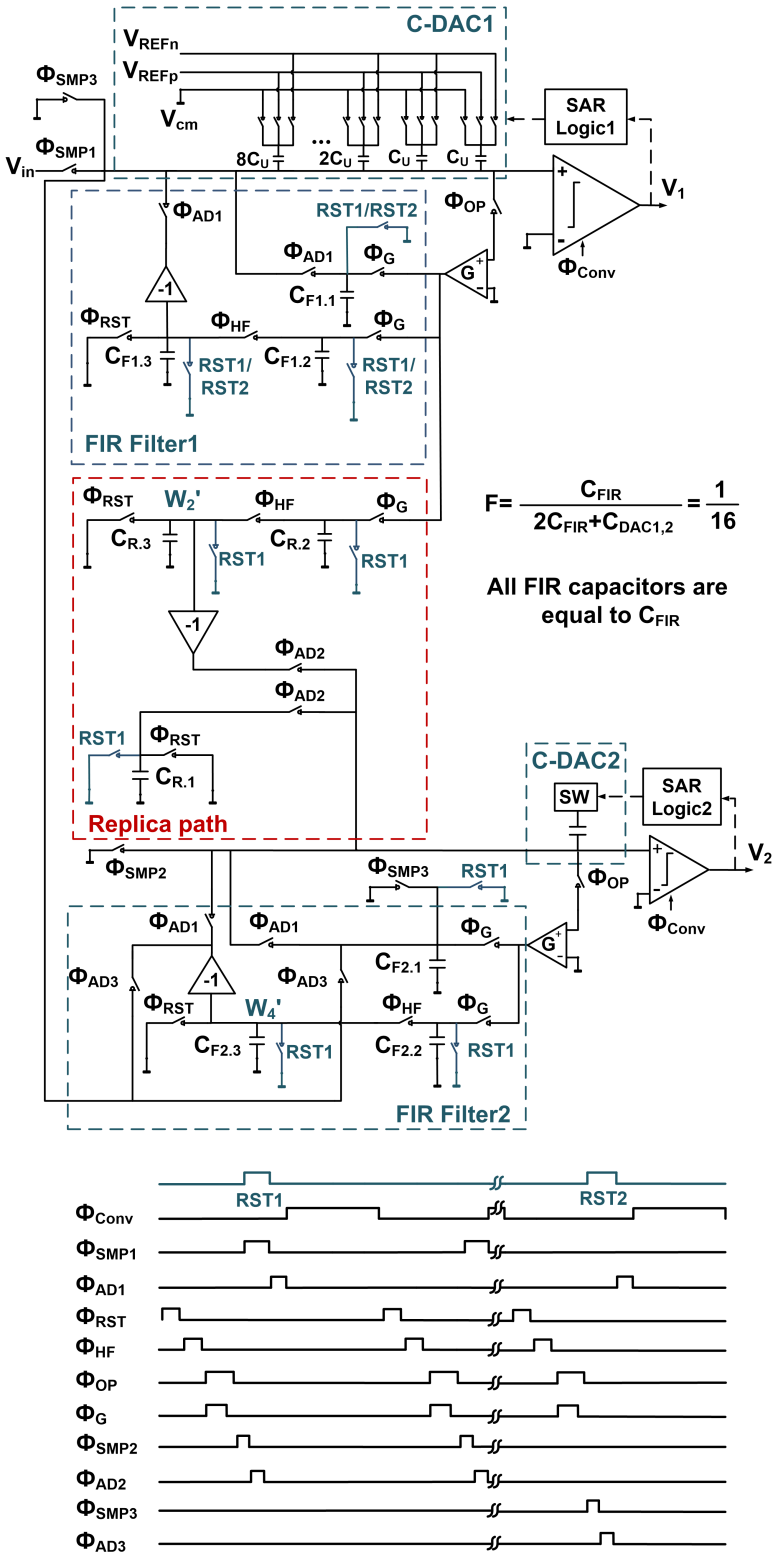



Figure 4.3 Macro-model of the MASH two-step NS-SAR IADC and its timing diagram

## 4.4 Simulation Results

### 4.4.1 Behavioral Model Simulation Results

Time-domain behavioral simulations were carried out in MATLAB/SIMULINK to verify the efficiency of the proposed MASH two-step NS-SAR IADC. A 4-bit SAR ADC along with an FIR filter was implemented behaviorally.

Figure 4.4 reports the SQNR obtained from simulations and calculations for the proposed ADC and its first step. This figure shows that at higher OSRs, the simulation and calculation results are more similar and the second step improves the SQNR more significantly.

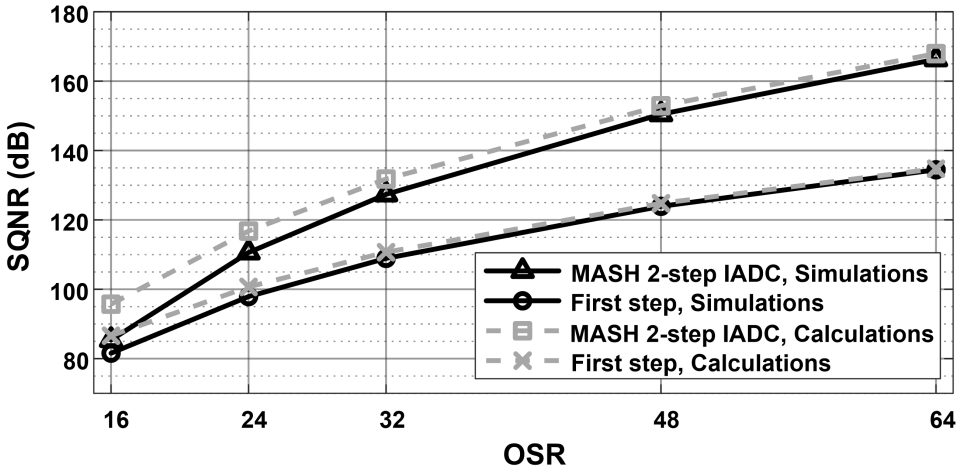



Figure 4.4 SQNR of the proposed IADC and its first step, for different OSRs, obtained by calculations and system-level simulations

For simulation purpose, $M_1 : M_2$ were set to $32 : 16$ for an overall OSR of 48. The proposed ADC was simulated over a bandwidth of 250 kHz. Figure 4.5, shows the power spectral density (PSD) of the proposed ADC for different case studies, i.e., 1) the second-order NS-SAR IADC, 2) the first step of the proposed architecture, 3) the proposed MASH two-step NS-SAR IADC. The simulated SQNRs for all the above-mentioned structures are 79.7/124/150 dB, respectively.

Table 4.1 compares the specification of the proposed architecture with [30], which is a two-step MASH IADC based on a $\Delta\Sigma$M structure. The first step of [30] comprises a MASH 2-1 IADC that is reconfigured to a second-order IADC in the second step. However, in [28], a second-order IADC is used for the first step and it is reconfigured to a first-order IADC in the second step. In order to have a fair comparison, the SQNR values have been calculated based on the expressions presented in each of prior works for an OSR of 48. This comparison

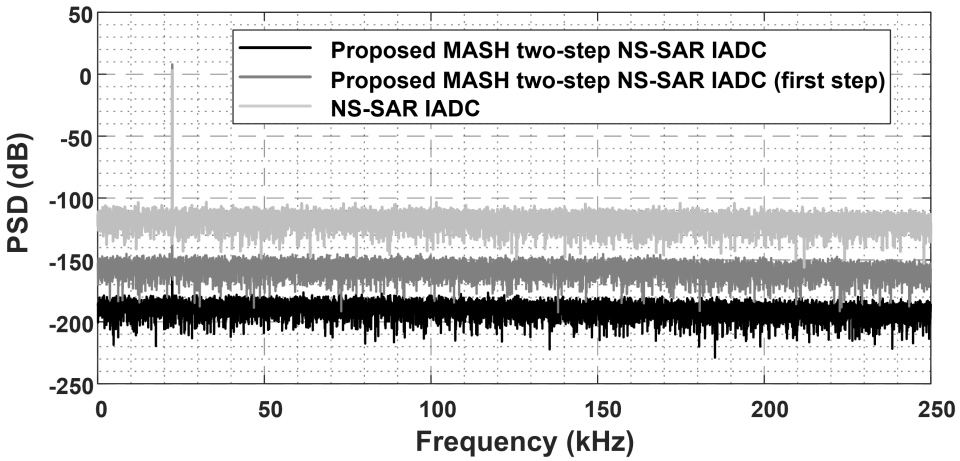



Figure 4.5 PSD of the proposed IADC for three different case studies

Table 4.1 Comparing various architectures and system level specifications

| Specifications | Electron. Lett. 2015 [30] | JSSC 2015 [28] | Conventional | Proposed |
|---|---|---|---|---|
| Architecture | ΔΣM-based | ΔΣM-based | ΔΣM-based | NS-SAR-based |
| Step1 /Step2 | MASH21 /2nd-order | 2nd-order /1st-order | MASH22 /2nd-order | MASH22 /2nd-order |
| No. of OTAs | 3 | 2 | 4 | 0 |
| No. of Comparators | 4 | 3 | 14 | 2 |
| SQNR (dB) | 106/128 | 126/90 | 150 | 150 |
| OSR | 32/48 | 192/48 | 48 | 48 |

illustrates that the proposed ADC can achieve a higher SQNR using fewer comparators and without utilizing OTAs. We also simulated the linear model of a conventional MASH two-step IADC (ΔΣM-based) and compared it with the proposed IADC. Table 4.1 reports that our design is OTA free while using a smaller number of comparators makes it efficient in terms of power dissipation and chip-area. It is important to consider the effects of non-idealities, such as thermal noise and capacitors mismatch in designing the proposed structure; however, it is not the focus of this paper.

## 4.5 Conclusion

A MASH two-step NS-SAR IADC is proposed. The MASH structure avoids the signal attenuation in the higher order NS-SAR ADCs. The proposed ADC takes advantage of an OTA-free structure. Therefore, OTA associated problems, such as finite gain, finite gain-bandwidth, linearity, etc, are no longer a concern. Using SAR-based quantizers provides

multi-bit quantizers without being concerned about linearization techniques, e.g. DEM. Not only does using a NS-SAR ADC in a two-step structure enhances resolution, but it also helps to have an area and power efficient ADC. Simulation results using SIMULINK show that an SQNR of 150 dB can be achieved by only using two 4-bit SAR ADCs. Therefore, the proposed topology is a potential candidate to implement an ultra-high resolution (20-24 bit) compact and energy efficient $\Delta\Sigma$-class ADCs.

## 4.6 Supplementary Materials

### 4.6.1 Time-domain Analysis

The time-domain analysis of the operation of the proposed IADC is presented in this section. According to Fig. 4.2(a), the behavior of the proposed architecture in the first stage is described as follows:

$$U[i] + 2 \cdot W_1[i] - W_2[i] + E_1[i] = V_1[i] \tag{4.11}$$

where $i$ is time-index, $W_1[i] = -E_1[i-1]$, and $W_2[i] = -E_1[i-2]$.

The quantization error samples during $M_1$ cycles are given by the following expressions:

$$E_1[1] = V_1[1] - U[1] \tag{4.12}$$

$$E_1[2] = V_1[2] + 2 \cdot V_1[1] - (U[2] + 2 \cdot U[1]) \tag{4.13}$$

$$\begin{aligned} E_1[3] = V_1[3] + 2 \cdot V_1[2] + 3 \cdot V_1[1] \\ - (U[3] + 2 \cdot U[2] + 3 \cdot U[1]+) \end{aligned} \tag{4.14}$$

$$\begin{aligned} E_1[M_1] = V_1[M_1] + 2 \cdot V_1[M_1 - 1] + ... + M_1 \cdot V_1[1] \\ - (U[M_1] + 2 \cdot U[M_1 - 1] + ... + M_1 \cdot U[1]) \end{aligned} \tag{4.15}$$

The compact form of (4.15) can be shown by the following expression:

$$E_1[M_1] = \sum_{k=1}^{M_1} \sum_{i=1}^{k} V_1[i] - \sum_{k=1}^{M_1} \sum_{i=1}^{k} U[i] \tag{4.16}$$

Modifying the last values of index of summations in (4.16), $W_2[M_1] = -E_1[M_1 - 2]$ is expressed as:

$$W_2[M_1] = \sum_{k=1}^{M_1-1}\sum_{i=1}^{k-1} U[i] - \sum_{k=1}^{M_1-1}\sum_{i=1}^{k-1} V_1[i] \tag{4.17}$$

According to Fig. 4.2(a), $W_2[i]$ is used as the input signal of the second stage. Using a similar process for the second-stage, $W_4[M_1] = -E_2[M_1 - 2]$ is expressed as follow:

$$W_4[M_1] = \sum_{k=1}^{M_1-1}\sum_{i=1}^{k-1} W_2[i] - \sum_{k=1}^{M_1-1}\sum_{i=1}^{k-1} V_2[i] \tag{4.18}$$

Since $W_2[i]$ does not change significantly during each conversion period, it can be replaced by $W_2[M_1]$ in (4.18), which results in the following expression:

$$\begin{aligned} W_4[M_1] = \frac{M_1^4}{4!}\cdot\widetilde{U} - \sum_{l=1}^{M_1-1}\sum_{j=1}^{l-1}\sum_{k=1}^{j-1}\sum_{i=1}^{k-1} V_1[i] \\ - \sum_{k=1}^{M_1-1}\sum_{i=1}^{k-1} V_2[i] \end{aligned} \tag{4.19}$$

where $\widetilde{U}$ is the average of the input signal, $U$, when it does not change significantly during each conversion period, as expressed in (4.20).

$$\begin{aligned} \widetilde{U} = \frac{4!}{(M_1-1)\cdot(M_1-2)\cdot(M_1-3)\cdot(M_1-4)} \\ \cdot \sum_{l=1}^{M_1-1}\sum_{j=1}^{l-1}\sum_{k=1}^{j-1}\sum_{i=1}^{k-1} U[i] \simeq \frac{4!}{M_1^4}\cdot \sum_{l=1}^{M_1-1}\sum_{j=1}^{l-1}\sum_{k=1}^{j-1}\sum_{i=1}^{k-1} U[i] \end{aligned} \tag{4.20}$$

As illustrated in Fig. 4.2(b), $W_4[M_1]$ is used as the input signal in the second step. Performing a similar process, $W_6[M_2]$ is obtained by:

$$\begin{aligned} W_6[M_2] = \frac{M_1^4\cdot M_2^2}{4!\cdot 2!}\cdot\widetilde{U} - \frac{M_2^2}{2!}\cdot \sum_{l=1}^{M_1-1}\sum_{j=1}^{l-1}\sum_{k=1}^{j-1}\sum_{i=1}^{k-1} V_1[i] \\ - \frac{M_2^2}{2!}\cdot \sum_{k=1}^{M_1-1}\sum_{i=1}^{k-1} V_2[i] - \sum_{k=1}^{M_1-1}\sum_{i=1}^{k-1} V_3[i] \end{aligned} \tag{4.21}$$

### 4.6.2 Macro Model Simulation Results

Figure 4.6 shows the macro-model simulation results for power spectral density (PSD) of the proposed IADC at $M = 18$. Comparing Fig. 4.6 with Fig. 4.4 confirms the similarity of the calculation, behavioral model and macro-model simulation results.

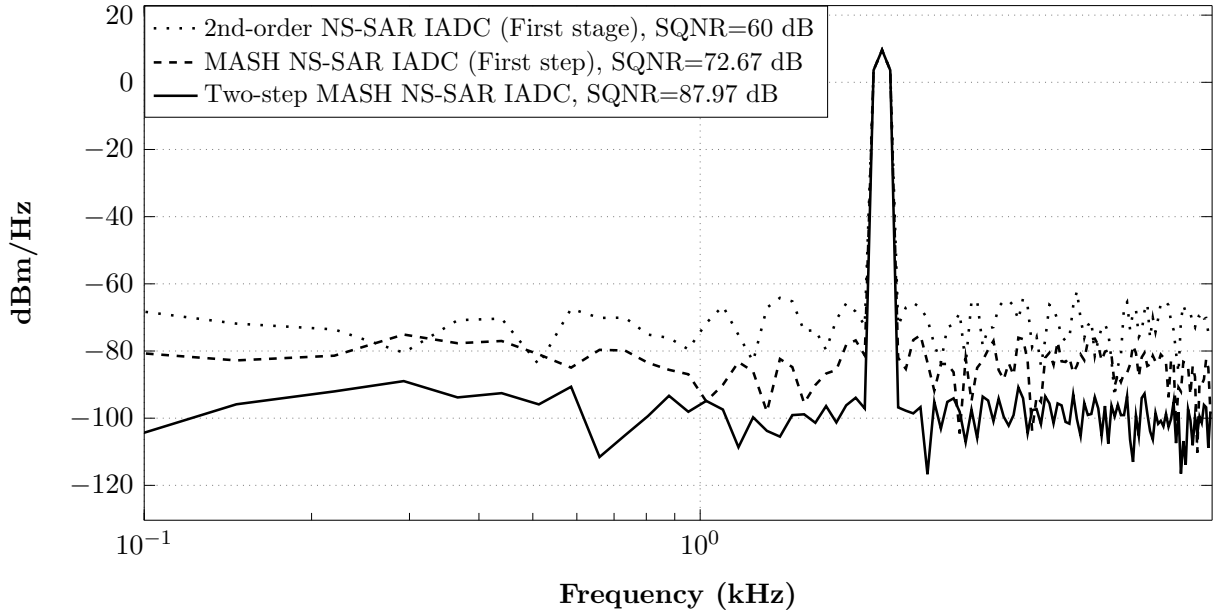



Figure 4.6 Macro-model simulation in Cadence: 4096-point PSD of the proposed IADC's first stage, first step, two-step output for $f_s = 300\ kHz$, $f_{in} = 2.125\ kHz$, $M = 18$ ($M_1 = 12$, $M_2 = 6$)

# CHAPTER 5 ARTICLE 3 : POWER BOUND ANALYSIS OF A TWO-STEP MASH INCREMENTAL ADC BASED ON NOISE-SHAPING SAR ADCS

The following sections are the reproduction of a published article in IEEE Transactions on Circuits and Systems I: Regular Papers.

- M. Akbari, M. Honarparvar, Y. Savaria and M. Sawan, "Power Bound Analysis of a Two-Step MASH Incremental ADC Based on Noise-Shaping SAR ADCs," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 68, no. 8, pp. 3133-3146, Aug. 2021, doi: 10.1109/TCSI.2021.3077366 [57].

## 5.1 Abstract

Power consumption is an important limitation in designing analog-to-digital converters (ADCs) used in low-power sensing applications. This paper estimates analytically the power bound of a two-step multi-stage noise-shaping successive-approximation-register incremental ADC (two-step MASH NS-SAR IADC) proposed in our previous work. Our model considers the impacts of thermal noise, mismatch, and CMOS process (minimum feature size in CMOS technologies) on the power bounds of the proposed IADC. The analytic results show that thermal noise and CMOS process requirements determine the power consumption lower bounds in high and low resolutions, respectively. A comparison with the most competitive single-loop delta-sigma ($\Delta\Sigma$) IADC shows a 3-dB higher theoretical figure-of-merit (FoM) for our proposed IADC when the resolutions are higher than 12-bit. Our proposed systematic analysis can be used to estimate the power bounds of amplifier-based NS-SAR ADCs used in either $\Delta\Sigma$ or incremental mode with multi-stage and multi-step topologies designed in various CMOS technologies. The reported analytic results are confirmed by experimental results of previously reported implementations.

Key Words: Two-step incremental analog-to-digital converters, noise-shaping SAR ADCs, multi-stage-noise-shaping, power bound.

## 5.2 Introduction

Power consumption is an important parameter of most integrated circuits used in portable applications such as sensor interfaces and internet of things (IoTs). Incremental analog-to-digital converters (IADCs) offer an appealing option in such applications [1,29]. They benefit

from oversampling and noise-shaping techniques to achieve a high-resolution ADC, while providing a sample-by-sample data conversion similar to that of a Nyquist rate ADC. IADCs offer several advantages over delta-sigma modulators ($\Delta\Sigma$Ms), e.g., simpler decimation filters, low latency, better immunity to idle tones, and better stability [18, 28].

Recently, a great deal of attention was dedicated towards designing power-efficient IADCs. Higher-order single-loop and multi-stage noise-shaping (MASH) IADCs have been presented in the literature [4, 19]. To further improve the power-efficiency of IADCs, multi-step IADCs have been proposed, where part of the ADC is re-used to boost the overall resolution [28, 30]. It is worth noting that operational transconductance amplifiers (OTAs) are integral parts of the IADC structures that need a lot of design effort. Multi-step structures are more power and area efficient because they increase the ADC resolution by re-using the number of OTAs. However, they still suffer from the following issues; 1) Higher-order modulators limit the output swing of the OTAs, 2) Multi-bit quantizers, e.g., FLASH ADCs, are needed to meet the required dynamic range (DR) when the oversampling ratio (OSR) is low. Therefore, not only does the power consumption matter, but linearization techniques are also required to mitigate the non-linearity of the digital-to-analog converter (DAC) used in the feedback [5].

As emphasized, when it comes to power consumption, implementing these architectures is challenging due to the OTAs and quantizers. To alleviate the above challenges, we proposed a two-step MASH IADC structure based on noise-shaping successive-approximation-register (NS-SAR) ADCs in [55]. NS-SAR ADCs are power-efficient topologies, which embed SAR ADCs in $\Delta\Sigma$Ms structures [38, 45, 50]. An error feedback (EF) structure was utilized in [32] to implement a fully passive NS-SAR (FPNS-SAR) ADC for the first time. However, as discussed in [42], the comparator suffers from substantial noise due to the limited gain of the filter. Also, it suffers from signal attenuation caused by charge-sharing, which results in an imperfect noise-transfer function (NTF). A buffer would mitigate this issue, but the structure would no longer be fully passive. Recently, an amplifier has been employed in front of the passive filter to alleviate the signal attenuation [39]. We adopted this idea for implementing the NS-SAR ADC sub-block in the proposed IADC. Figure 5.1 compares NS-SAR ADCs with the best performances, previously published in the International Solid-State Circuits Conference (ISSCC) and the Journal of Solid-State Circuits (JSCC) during the past six years. It demonstrates that the majority of amplifier-based NS-SAR ADCs have achieved the highest FoMs.

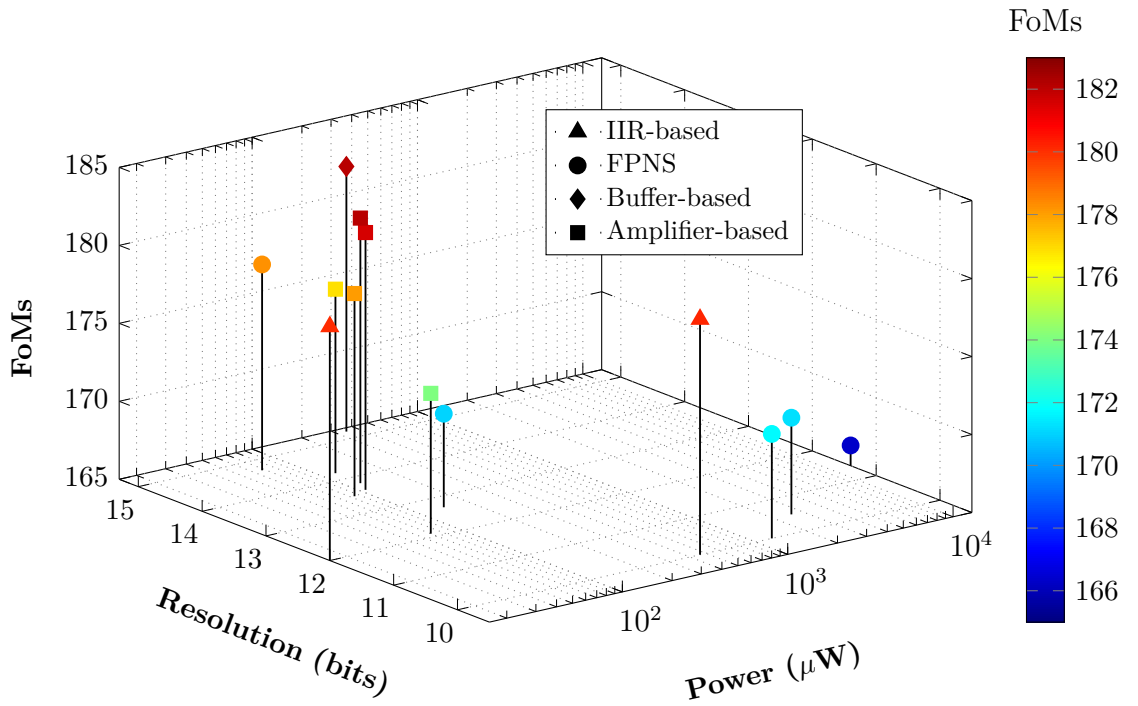



Figure 5.1 Comparison of NS-SAR ADCs, offering the best performance, published in ISSCC and JSSC from 2016 to 2021

Our proposed IADC obtains higher noise-shaping order by cascading lower noise-shaping order single-loop NS-SAR ADCs in an incremental mode. In the proposed topology, a MASH 2-2 NS-SAR IADC is utilized during the first step. The first stage is then employed to process the residue voltage and improve the overall resolution of the IADC.

It is worth noting that analyzing the power bound is required for further optimizing the power-efficiency of the proposed IADC. Power bound analyses have been published for Nyquist rate ADCs and $\Delta\Sigma$ IADCs [7–9]. However, to the best of the authors knowledge, a comprehensive analytic study has not been performed for the NS-SAR ADCs, multi-stage, and multi-step IADCs. The present paper introduces the analysis of power bounds for the proposed IADC structure, considering three factors, i.e., thermal noise, mismatch, and complementary metal-oxide-semiconductor (CMOS) process impact due to the minimum feature size in CMOS technologies. It is worth to note that since IADCs are mostly used in low-frequency applications, the flicker noise affects their performance significantly. However, most flicker noise can be effectively canceled using chopping, auto-zeroing and correlative-double sampling (CDS) techniques [40, 58]. Therefore, the impact of the flicker noise is ignored in this paper. The presented analysis investigates the most power-consuming components, which need more effort to be designed efficiently. The achieved analytic results also predict the

dominant factor that determines the IADC power bound according to the IADC specifications and desired resolution. Also, the necessity of using DAC calibration and sampling capacitor scaling techniques are determined based on the results of our analysis. A comparison of the analytic thermal noise-limited Schrier figure-of-merit ($FoM_s$)[1] of the proposed IADC with its counterpart single-loop $\Delta\Sigma$ IADC shows a 3-dB improvement.

The remainder of this paper is organized as follows. Section 5.3 briefly discusses the system-level and macro-model structure of our proposed two-step MASH NS-SAR IADC and generalize the equations derived in [55]. This information is then employed in Section 5.4 to present a set of equations that allow estimating the proposed IADC power bounds limited by thermal noise, mismatch, and CMOS process. Section 5.5 draws conclusions from this paper. It is worth noting that Table 5.1 lists and defines parameters utilized in this paper.

## 5.3 Proposed Architecture

The following sections summarize the information and results presented in [55], which are required later to analyze the power bounds of the proposed IADC architecture. It should be noted that a more detailed description along with a system-level comparison with other known structures is provided in [55].

### 5.3.1 System-level Implementation

Figure 5.2 shows the block diagram and timing diagram of the first and second steps of the proposed IADC. As depicted in Fig. 5.2(a), a MASH structure, with two similar stages, is employed in the first step of the IADC, and then the first stage is re-used in the second step, as shown in Fig. 5.2(b). In the proposed structure, each stage is based on an EF-NS-SAR topology with a second-order finite impulse response (FIR) filter in the feedback path. Each stage realizes a second-order NTF, $NTF(z)=(1-z^{-1})^2$. Therefore, the proposed structure achieves a sixth-order noise-shaping performance using only two SAR ADCs.

As shown in Fig. 5.2(c), each conversion period that lasts a total $M$ cycles is split into two phases lasting $M_1$ and $M_2$ cycles each.

[1] $FoM_s = SNDR + 10log(\frac{Bandwidth}{Power})$

Table 5.1 Parameters list

| Parameter | Description |
|---|---|
| OAi (i=1,2,3) | Operational amplifier of i-th stage |
| SARi (i=1,2,3) | SAR ADC of i-th stage |
| $b$ | IADC resolution |
| $b_s$ | SAR ADCs resolution |
| $P_{OA_{ref}}$ | Power consumption of the operational amplifier with unity-gain frequency: $f_u$ operation time: one conversion period |
| $P_{SAR_{ref}}$ | Power consumption of the SAR ADC with operation time: one conversion period |
| $t_s$ | Settling time of the OA with unity gain frequency of $f_u$ |
| $NNR$ | Noise reduction ratio achieved by noise-shaping and oversampling techniques in IADCs |
| $P_{OA_t,th}$ | OAs total thermal noise-limited power consumption |
| $P_{t,SAR,th}$ | SAR ADCs total thermal noise-limited power consumption |
| $P_{t,th}$ | IADC total thermal noise-limited power consumption |
| $P_{OA_t,mis1}$ | OAs total power consumption limited by DAC unit capacitor mismatch |
| $P_{t,SAR,th}$ | SAR ADCs total power consumption limited by DAC unit capacitor mismatch |
| $P_{t,mis1}$ | IADC total power consumption limited by DAC unit capacitor mismatch |
| $P_{t,mis2}$ | IADC total power consumption limited by FIR capacitors mismatch |
| $P_{OA_t,process}$ | OAs total power consumption limited by CMOS process |
| $P_{t,SAR,process}$ | SAR ADCs total power consumption limited by CMOS process |
| $P_{t,mis1}$ | IADC total power consumption limited by CMOS process |
| $P_{t,th}$ | IADC total thermal noise-limited power consumption |
| $P_{OA_t,mis1}$ | OAs total power consumption limited by DAC unit capacitor mismatch |
| $C_{DAC,th}$ | DAC capacitor size determined by thermal noise |
| $C_{DAC,mis1}$ | DAC capacitor size determined by DAC unit capacitor mismatch |
| $C_{DAC,mis2}$ | DAC capacitor size determined by FIR capacitors mismatch |
| $C_{DAC,process}$ | DAC capacitor size determined by CMOS process |

According to the time-domain analysis presented in our previous paper, [55], the overall output of the proposed IADC, $Y[M]$, is given by:

$$\begin{aligned} Y[M] = Y_{s1}[M_1] + \frac{4!}{M_1^4} \cdot Y_{s2}[M_2] = \frac{4!}{M_1^4} \cdot \Big( \sum_{l=1}^{M_1-1} \sum_{q=1}^{l-1} \sum_{j=1}^{q-1} \sum_{i=1}^{j-1} V_1[i] + \sum_{j=1}^{M_1-1} \sum_{i=1}^{j-1} V_2[i] \Big) \\ + \frac{4!}{M_1^4} \cdot \frac{2!}{M_2^2} \cdot \sum_{j=1}^{M_2-1} \sum_{i=1}^{j-1} V_3[i] = \widetilde{U} - \frac{4!}{M_1^4} \cdot \frac{2!}{M_2^2} \cdot W_6[M_2] \end{aligned} \tag{5.1}$$

where $Y_{s1}[M_1]$ and $Y_{s2}[M_2]$ are the overall output signal of the first and second steps, respectively.

According to Fig. 5.2(b), $W_6[M_2]$ equals to $-E_3[M_2-2]$, i.e., SAR ADC quantization error, which is defined by:

$$E_3[M_2-2] = \frac{V_{FS}}{L-1} \tag{5.2}$$

where $V_{FS}$ is the full-scale voltage of the IADC, and $L{=}2^Q-1$ is the number of quantization levels for a $Q$-bit quantizer.

It is worth noting that in NS-SAR ADC topologies, an extra SAR ADC conversion clock cycle is required to extract the residue voltage of the SAR ADC. Therefore, a $b_s$-bit SAR ADC, which is used as a quantizer, produces $Q = b_s - 1$.

The overall quantization error of the IADC, $E_{Q,t}$, is then obtained using (5.1) and (5.2), as established by the following expression:

$$E_{Q,t} \simeq \frac{4!}{M_1^4} \cdot \frac{2!}{M_2^2} \cdot \frac{V_{FS}}{L-1} \tag{5.3}$$

Signal-to-quantization-noise-ratio (SQNR) is defined as follow:

$$SQNR = 10 \cdot \log(\frac{P_{sig,FS}}{P_Q}) = 10 \cdot \log(\frac{\frac{V_{FS}}{2\sqrt{2}}}{\frac{E_{Q,t}}{\sqrt{12}}})^2 \simeq 20 \cdot \log(\frac{V_{FS}}{E_{Q,t}}) \tag{5.4}$$

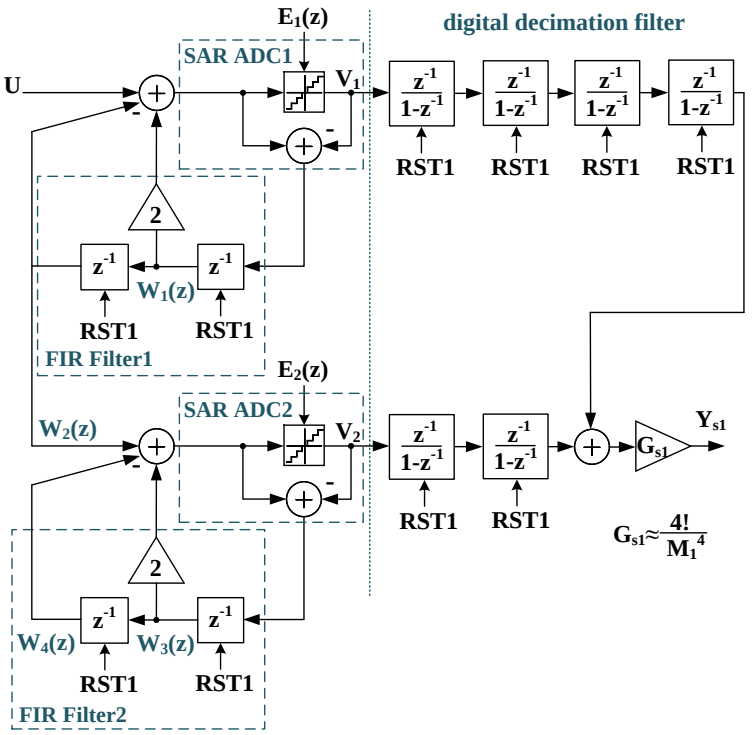
where $P_{sig,FS}$ and $P_Q$ are IADC full-scale input signal power and quantization noise power, respectively.

Replacing $E_{Q,t}$ from (5.3) in (5.4) results in the SQNR equation of the proposed structure shown by the following expression:

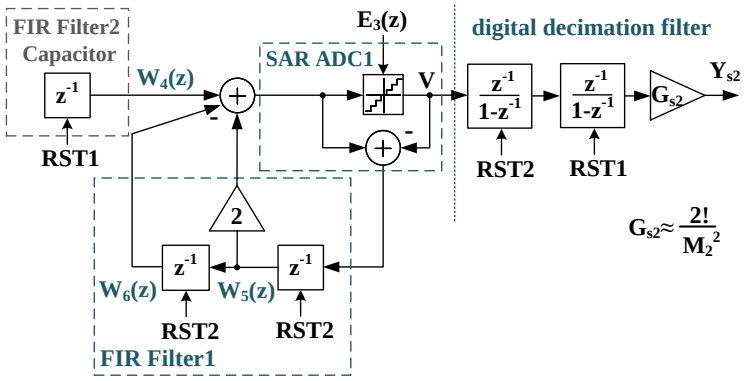
$$SQNR = 4 \cdot 20 \cdot \log(M_1) + 2 \cdot 20 \cdot \log(M_2) + 20 \cdot \log(L-1) - 20 \cdot \log(4! \cdot 2!) \tag{5.5}$$

The derived SQNR equation can be generalized, as denoted by $SQNR_g$ in (5.6), for an $N_1^{th}+N_2^{th}$ order NTF, where $N_1$ and $N_2$ are the NTF orders of the proposed IADC in the first and the second steps, respectively.

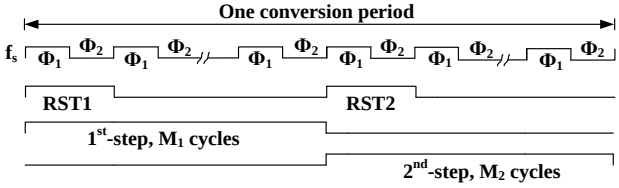
$$SQNR_g \simeq N_1 \cdot 20\log(M_1) + N_2 \cdot 20\log(M_2) + 20\log(L-1) - 20\log(N_1! \cdot N_2!) \tag{5.6}$$




(a)




(b)




(c)

Figure 5.2 Proposed two-step MASH NS-SAR IADC: (a) Operation of the proposed LADC during the first step, (b) Operation of the proposed IADC during the second step, (c) Timing diagram

The IADC overall quantization error, $E_{Q,g}$, expression can also be generalized as:

$$E_{Q,g} \simeq \frac{N_1!}{M_1^{N_1}} \cdot \frac{N_2!}{M_2^{N_2}} \cdot \frac{V_{FS}}{L-1} \tag{5.7}$$

The proper $\gamma{=}\frac{M_1}{M_2}$ ratio to optimize SQNR value is achieved by replacing $M_1{=}\frac{\gamma}{\gamma+1} \cdot M$ and $M_2 = \frac{1}{\gamma+1} \cdot M$ in (5.7) and solving $\frac{\partial E_{Q,g}}{\partial \gamma} = 0$, as follows:

$$\gamma_{opt} = \frac{N_1}{N_2} \tag{5.8}$$

The proposed behavioral two-step MASH NS-SAR IADC model was implemented using 4-bit SAR ADCs, along with the FIR filters. Then, behavioral simulations were carried out in MATLAB/SIMULINK to verify the validity of derived equations. Employing (5.8), $\frac{M_1}{M_2}{=}2$ is used in these simulations.

Figure 5.3 shows the SQNR as a function of the oversampling ratio obtained from behavioral simulations and calculations for the proposed IADC for two following different NTF order combinations. Case1: $N_1 = 2$ and $N_2 = 1$, Case2: $N_1 = 4$ and $N_2 = 2$. Simulation results have the same trend as the calculation results. In Case2, the difference between simulation and calculation results in low oversampling ratio values is due to the approximations that we used in [55] for simplifying the equations, as follows:

$$(M_1 - 1) \cdot (M_1 - 2) \cdot (M_1 - 3) \cdot (M_1 - 4) \simeq M_1^4 \tag{5.9}$$

$$(M_2 - 1) \cdot (M_2 - 2) \simeq M_2^2 \tag{5.10}$$

Similarly, the following approximations are used for Case1.

$$(M_1 - 1) \cdot (M_1 - 2) \simeq M_1^2 \tag{5.11}$$

$$(M_2 - 1) \simeq M_2 \tag{5.12}$$

Precise calculation results without using the above estimations are illustrated in Fig. 5.3 for Case1 and Case2. Good agreement between simulation and precise calculation results validates the reliability of the presented analysis.

Unlike Case2, estimated and precise SQNR values for Case1 are more similar because of

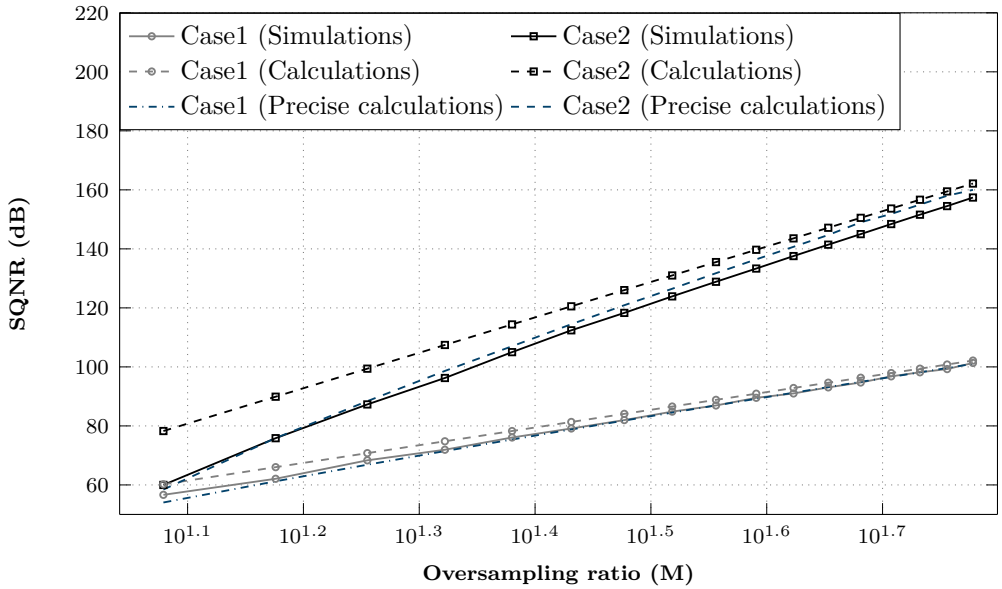



Figure 5.3 Calculation (estimated and precise) and behavioral simulation results for SQNR versus oversampling ratio; Case1: $N_1 = 2$, $N_2 = 1$, Case2: $N_1 = 4$, $N_2 = 2$

its lower noise-shaping order in each step as compared with Case2. The general expression (5.13) explains the observed difference between Case1 and Case2.

$$(n-1)\cdot(n-2)\cdots(n-i) \simeq n^i \tag{5.13}$$

This approximation is more precise for large values of $n$ or small values of $i$, where $n$ is used instead of $M_1$ or $M_2$ and $i$ is the noise-shaping order in the first or second step of the IADC, which are expressed by $N_1$ and $N_2$.

### 5.3.2 Macro-model Implementation

Figure 5.4 shows the macro-model implementation of the proposed IADC. Each stage includes a 4-bit SAR ADC as a multi-bit quantizer. The loop filter consists of a second-order switched-capacitor (SC) FIR filter and an operational amplifier (OA) with the gain of $G = 16$.

As discussed in [55], processing the residue signal by FIR filter and injecting it to the input is based on charge sharing between FIR capacitors and also between FIR capacitors and DAC capacitors, $C_{DAC}$, respectively. The charge sharing operation in the first stage is formulated using three coefficients, i.e., $k_f$, $k_d$, and $k_s$, as follows:

$$k_f = \frac{C_{F1.1/F1.3}}{C_{F1.1} + C_{F1.3} + C_{DAC1}} = \frac{C_{FIR}}{C_{DAC} + 2C_{FIR}} = \frac{1}{8} \tag{5.14}$$

$$k_d = \frac{C_{F1.2}}{C_{F1.2} + C_{F1.1}} = \frac{1}{2} \tag{5.15}$$

$$k_s = \frac{C_{DAC1}}{C_{DAC1} + C_{F1.1} + C_{F1.3}} = \frac{C_{DAC}}{C_{DAC} + 2 \cdot C_{FIR}} = \frac{3}{4} \tag{5.16}$$

Since FIR capacitors and DAC capacitors size equal to $C_{FIR}$ and $C_{DAC}$, respectively, the achieved coefficients are valid for both stages. The capacitors size ratio, i.e., $\frac{C_{DAC}}{C_{FIR}} = 6$, and hence the charge sharing coefficient values mentioned in (5.14)-(5.16) are required to realize a second-order NTF in each stage. The derived equations in this section are the foundation of our analysis in the following section to estimate thermal noise and mismatch limited power consumption.

It is worth noting that increasing the size of OAs input transistors suppresses the flicker noise. However, OAs non-linear input capacitors cause distortion when their size is large enough to change DAC capacitor voltage. Increasing the DAC capacitor size can alleviate this distortion. Also, a linearity enhancement technique presented in [38] could be adopted when using small DAC capacitor values. On the other hand, the mismatch between analog and digital parts caused by the large OA input capacitor is mitigated by tuning the decimation filters, as discussed in Section III-D. Chopping is also a widely used technique for canceling the flicker noise. According to the low bandwidth operation of the IADCs, chopping is possible even in high OSR values, as performed in [5] with OSR of 1000 and bandwidth of 2 $MHz$. The majority of published NS-SAR ADCs employed either linearity enhancement or chopping techniques. Besides, both methods have been used in [40] without any destructive interaction and power consumption costs.

## 5.4 Power Consumption Estimation

Noise, mismatch, and CMOS process contribute to determining the ADCs minimum power consumption [7–9]. This section analyzes the proposed IADC power consumption that is determined by the power dissipation in its components, i.e., OAs and SAR ADCs.

As mentioned earlier, the proposed two-step structure consists of two stages with two OAs and two SAR ADCs, and the first stage is re-used in the second step. Two assumptions are considered for the rest of our analysis.

First, it is assumed that there are three OAs and three SAR ADCs in the proposed IADC. The OA1 and SAR1 are considered as the first-stage OA and SAR ADC, which are used in

the first step. The OA2 and SAR2 are the second-stage OA and SAR ADC, which operate in the first step. Finally, OA3 and SAR3 are the first-stage OA and SAR ADC that are re-used in the second step.

Second, the operation time for the OAs and SAR ADCs mentioned in the first assumption is not identical. Each conversion period consists of $M = M_1 + M_2$ cycles. The OA1, SAR1, OA2 and SAR2 operate for $\frac{2}{3}$ of the conversion period, i.e., $M_1$ cycles, while OA3 and SAR3 operate for $\frac{1}{3}$ of the conversion period, i.e., $M_2$ cycles.

### 5.4.1 Operational Amplifier Power Consumption

The OA power consumption is related to the required OA unity-gain frequency to meet the target dynamic range (DR) [7]. For that reason, the OA settling error must be less than half of the IADC least-significant-bit (LSB). The step response of the OA is formulated by the OA load capacitor charge equation as follow:

$$V_{out} = V_{out+} - V_{out-} = V_{ref} \cdot (1 - e^{-t/\tau}) \tag{5.17}$$

where $V_{out+}$, $V_{out-}$ are single-ended, and $V_{out}$ is the differential output voltages of a fully-differential OA, $V_{ref}$ is the reference voltage of the IADC, and $\tau$ is the OA time constant.

The required OA settling error, $e_s$, is determined by:

$$e_s = V_{out}(t = \infty) - V_{out}(t_s) = \frac{LSB}{2} = \frac{V_{ref}}{2 \cdot 2^b} \tag{5.18}$$

where $t_s$ is the OA settling time and $b$ is the IADC overall resolution. Combining (5.17) and (5.18), the OA time constant, $\tau$, is expressed as:

$$\tau = \frac{t_s}{(b+1) \cdot \ln 2} \tag{5.19}$$

According to the timing diagram of the proposed IADC shown in Fig. 5.4, the OA settling time is the same as or less than half of the IADC sampling time, $T_s$. Assuming $t_s = \frac{T_s}{2}$ in (5.19), the required OA unity-gain frequency, $f_u$, and transconductance, $G_m$, are given by:

$$f_u = \frac{1}{\tau} = 2 \cdot \ln 2 \cdot (b+1) \cdot f_s \tag{5.20}$$

$$G_m = \frac{C_L}{\tau} = 4 \cdot (b+1) \cdot \ln 2 \cdot C_L \cdot f_s \tag{5.21}$$

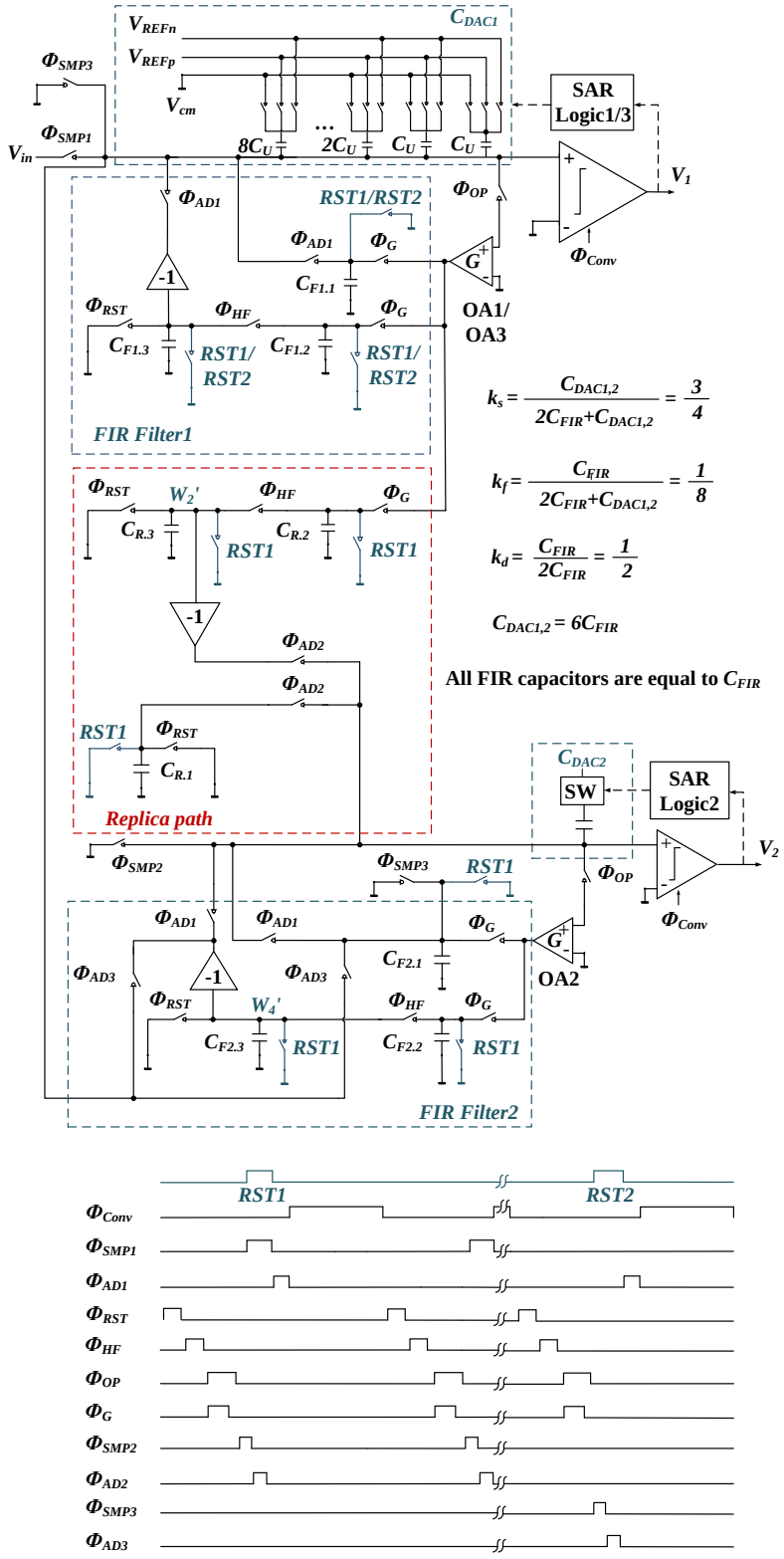



Figure 5.4 Macro-model of the proposed two-step MASH NS-SAR IADC and its timing diagram

where $f_s = \frac{1}{T_s}$ is IADC sampling frequency, and OA load capacitor in the proposed structure is $C_L = C_{FIR} = \frac{1}{6} \cdot C_{DAC}$.

Thus, the power consumption of a single-stage fully-differential OA structure that operates for $M$ cycles in each IADC conversion cycle with a unity-gain frequency of $f_u$, i.e., $P_{OA_{ref}}$, is expressed as follows:

$$P_{OA_{ref}} = 2 \cdot I_d \cdot V_{DD} = G_m \cdot V_{ov} \cdot V_{DD} = \frac{1}{3} \cdot (b+1) \cdot \ln 2 \cdot C_{DAC} \cdot f_s \cdot V_{ov} \cdot V_{DD} \tag{5.22}$$

where $I_d$ and $V_{ov}$ are the current and the overdrive-voltage of the OA input differential pair, respectively, and $V_{DD}$ is the supply voltage. Comparing (5.20) and (5.22) demonstrates that the OA power is linearly related to the OA unity-gain frequency.

$$P_{OA_{ref}} = \frac{1}{6} \cdot C_{DAC} \cdot V_{ov} \cdot V_{DD} \cdot f_u \tag{5.23}$$

Behavioral simulations are then used to investigate the unity-gain frequency of three OAs mentioned in the first assumption to estimate their contribution to the total power consumption. Figure 5.5 depicts $f_u$ of OA1, OA2, and OA3, which is required to achieve the resolution of $b$=20-bit, versus the sampling frequency. This figure illustrates the linear relationship between $f_u$ and $f_s$ as predicted by (5.20). Also, comparing the slope of the lines, the relationship between OAs unity-gain frequency is established as follows:

$$f_{u_1} = 1.45 \cdot f_{u_2} = 2.8 \cdot f_{u_3} \tag{5.24}$$

where $f_{u_1}$, $f_{u_2}$, and $f_{u_3}$ are the minimum unity-gain frequency requirement of OA1, OA2, and OA3, respectively, to achieve the target resolution. Since $f_{u3}$ is smaller than $f_{u1}$, OA1 can be reconfigured in the second step as OA3 with a relatively relaxed unity-gain frequency.

According to (5.23), expression (5.24) could determine a relationship between OAs power consumption if they had the same operation time. It is worth noting that (5.22) gives the power consumption of an OA with a unity-gain frequency of $f_u$, and an operation time equals the conversion period. However, OAs operation time is not identical according to the second assumption, i.e., $M_1 = 2 \cdot M_2 = \frac{2}{3} \cdot M$. Considering (5.24) with the OAs operation time, and $f_{u_1} = f_u$, results in OAs power consumption as follows:

$$P_{OA_1} = 0.67 \cdot P_{OA_{ref}} \tag{5.25}$$

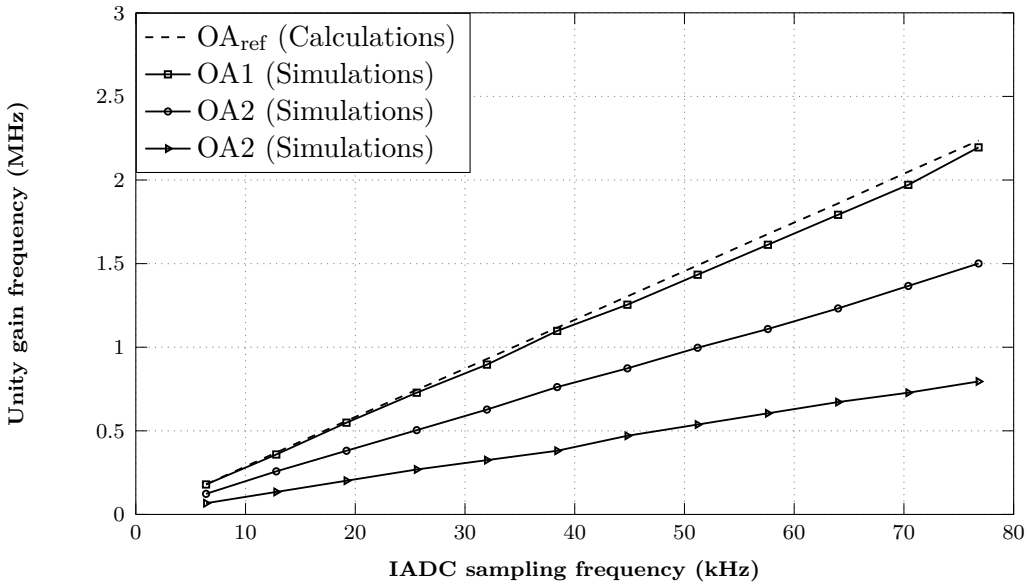



Figure 5.5 OAs minimum required unity-gain frequency predicted by behavioral simulations to achieve a 20-bit resolution at different IADC sampling frequencies, and $f_u$ values calculated by (5.20)

$$P_{OA_2} = 0.46 \cdot P_{OA_{ref}} \tag{5.26}$$

$$P_{OA_3} = 0.12 \cdot P_{OA_{ref}} \tag{5.27}$$

where $P_{OA_1}$, $P_{OA_2}$, and $P_{OA_3}$ are the power consumption of OA1, OA2, and OA3, respectively. Therefore, the total power dissipation by OAs, $P_{OA_t}$, is derived as follows:

$$P_{OA_t} = 1.25 \cdot P_{OA_{ref}} = 1.86 \cdot P_{OA_1} \tag{5.28}$$

which predicts that the OA1 consumes approximately 54% of the total OAs power dissipation. Applying (5.22) to (5.25) results in:

$$P_{OA_t} \simeq 0.42 \cdot \ln 2 \cdot (b+1) \cdot V_{ov} \cdot V_{DD} \cdot C_{DAC} \cdot f_s \tag{5.29}$$

This result is employed later in combination with information on noise, mismatch, and CMOS process requirements for estimating the IADC total power consumption.

### 5.4.2 SAR ADC Power Consumption

The SAR ADC power consumption is determined by summing the DAC array switching power, $P_{SW}$, comparator power, $P_C$, and SAR logic power, $P_L$.

Figure 5.6 depicts the $V_{cm}$-based switching method procedure of a 3-bit SAR ADC. Summing the average switching energy in each switching phase, the total switching energy, $E_{SW}$, for a $b_s$-bit SAR ADC is established by:

$$E_{SW} = \sum_{i=2}^{b_s} 2^{b_s-2\cdot i} \cdot (2^{i-1} - 1) \cdot C_U \cdot V_{ref}^2 \tag{5.30}$$

where $C_U$ is the DAC unit capacitor, which is defined as:

$$C_U = \frac{C_{DAC}}{2^{b_s}} \tag{5.31}$$

Therefore, the SAR switching power consumption is achieved by:

$$P_{SW} = \sum_{i=2}^{b_s} 2^{-2\cdot i} \cdot (2^{i-1} - 1) \cdot C_{DAC} \cdot V_{ref}^2 \cdot f_s \tag{5.32}$$

The power consumption of a dynamic latch comparator is expressed in [8] as follows:

$$P_C = f_c \cdot C_C \cdot V_{DD}^2 + (2 \cdot f_s \cdot V_{DD} \cdot V_{ov} \cdot C_C \cdot b_s \cdot (\ln \frac{V_{DD}}{V_{ref}} + \frac{(b_s+1)}{2} \cdot \ln 2 + 1)) \tag{5.33}$$

where $C_C$ is the minimum load capacitor of the comparator, and the SAR clock frequency is $f_c > (b_s + 1) \cdot f_s$.

The SAR logic power dissipation is estimated by its dynamic power based on assuming a conventional SAR logic structure consists of $2 \cdot b_s$ D-type Flip-Flops (DFFs) for a $b_s$-bit SAR ADC resolution.

$$P_L = 0.5 \cdot C_{Logic} \cdot f_s \cdot V_{DD}^2 \tag{5.34}$$

where $C_{Logic}$ is the SAR logic load capacitor, which is considered approximately $16{\cdot}b_s$ inverters since the capacitive load of one DFF equals that of 8 inverters.

$$P_L = 16 \cdot \beta \cdot b_s \cdot f_c \cdot C_{inv} \cdot V_{DD}^2 \tag{5.35}$$

where $C_{inv}$ is the input capacitance of a minimum-sized inverter for the adopted CMOS

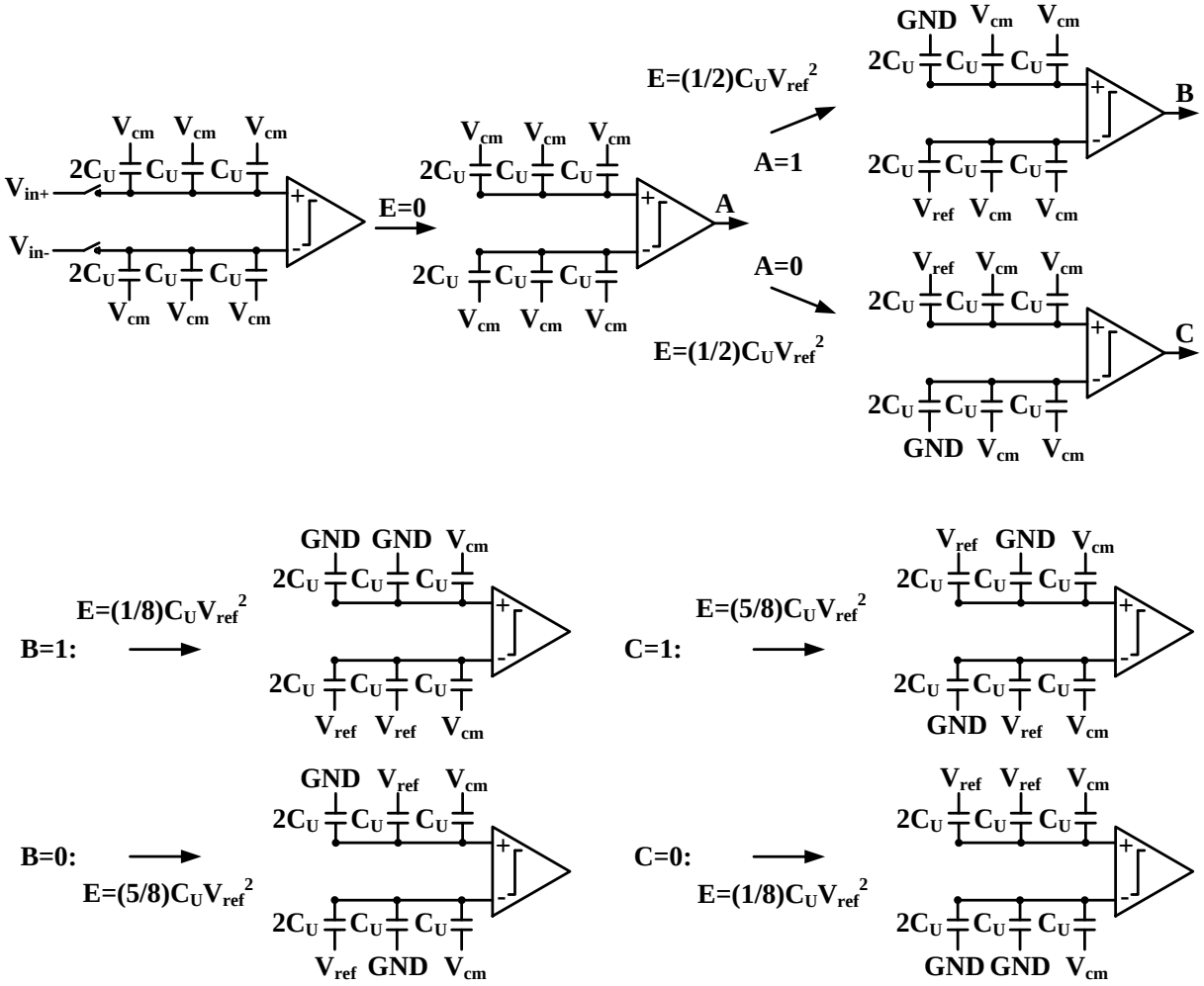



Figure 5.6 $V_{cm}$-based DAC switching process for a 3-bit SAR ADC

process. The total activity of the SAR logic is expressed by $\beta$, which is assumed to be 0.4 for clocking one-fourth of the transistors in the SAR logic [8].

We select $V_{DD}$=$V_{ref}$, $b_s$=4 and hence $f_c$=5 $\cdot$ $f_s$ in all presented analyses in this paper. Therefore, if SAR ADC operates for $M$ cycles in all conversion periods, its power consumption, $P_{SAR_{ref}}$, is derived as:

$$P_{SAR_{ref}} \simeq f_s \cdot C_{DAC} \cdot V_{DD}^2 \cdot (0.137 + \frac{C_C}{C_{DAC}}(\frac{22 \cdot V_{ov}}{V_{DD}} + 5) + 128 \cdot \frac{C_{inv}}{C_{DAC}}) \tag{5.36}$$

However, as mentioned in the first and second assumptions, SAR1, SAR2, and SAR3 operate in a fraction of the IADC conversion period lasting $M_1$, $M_1$, and $M_2$ cycles, respectively.

Accordingly, the power consumption of SARs are related to $P_{SAR_{ref}}$ as follows:

$$P_{SAR1} = P_{SAR2} = \frac{2}{3} \cdot P_{SAR_{ref}} \tag{5.37}$$

$$P_{SAR3} = \frac{1}{3} \cdot P_{SAR_{ref}} \tag{5.38}$$

$$P_{t,SAR} = \frac{5}{3} \cdot P_{SAR_{ref}} \tag{5.39}$$

where $P_{t,SAR}$ is total power consumption by SAR ADCs. Comparing (5.37) with (5.39) predicts that SAR1 accounts for approximately 40% of the total SAR ADCs power consumption. Injecting (5.36) into (5.39), the total power dissipation by SAR ADCs is expressed as follow:

$$P_{t,SAR} = \frac{5}{3} \cdot f_s \cdot C_{DAC} \cdot V_{DD}^2 \cdot (0.137 + \frac{C_C}{C_{DAC}}(\frac{22 \cdot V_{ov}}{V_{DD}} + 5) + 128 \cdot \frac{C_{inv}}{C_{DAC}}) \tag{5.40}$$

The following sections use the obtained expressions to estimate the IADC power consumption for given levels of noise, mismatch and CMOS process requirements.

### 5.4.3 ADC Thermal Noise-limited Power Bound

Thermal noise-limited power consumption is estimated by considering the target signal-to-noise-ratio (SNR). This value is mainly constrained by ADC total input-referred noise power, which is assumed to be split equally between quantization and thermal noise power [7–9]. It is noteworthy that noise reduction caused by oversampling and noise-shaping techniques should be considered in calculating the noise power of the IADCs. In the following, we present a process to estimate the proposed IADC quantization and thermal noise. The achieved results are then used to formulate the ADC thermal noise-limited power bound.

The quantization noise power, $\overline{v_{nq,in}^2}$, for the proposed IADC is obtained by:

$$\overline{v_{nq,in}^2} = \frac{V_{ref}^2}{12 \cdot 2^{2 \cdot b}} \tag{5.41}$$

Figure 5.7 depicts the block diagram of the first stage of the proposed structure with the charge sharing effects and thermal noise of the components. The coefficients used to model the charge sharing effect, i.e., $k_f$, $k_d$, and $k_s$, are defined by (5.14)-(5.16). Also, the FIR filter noise power stored in the FIR capacitors after each switching phase is derived (Fig. 5.8).

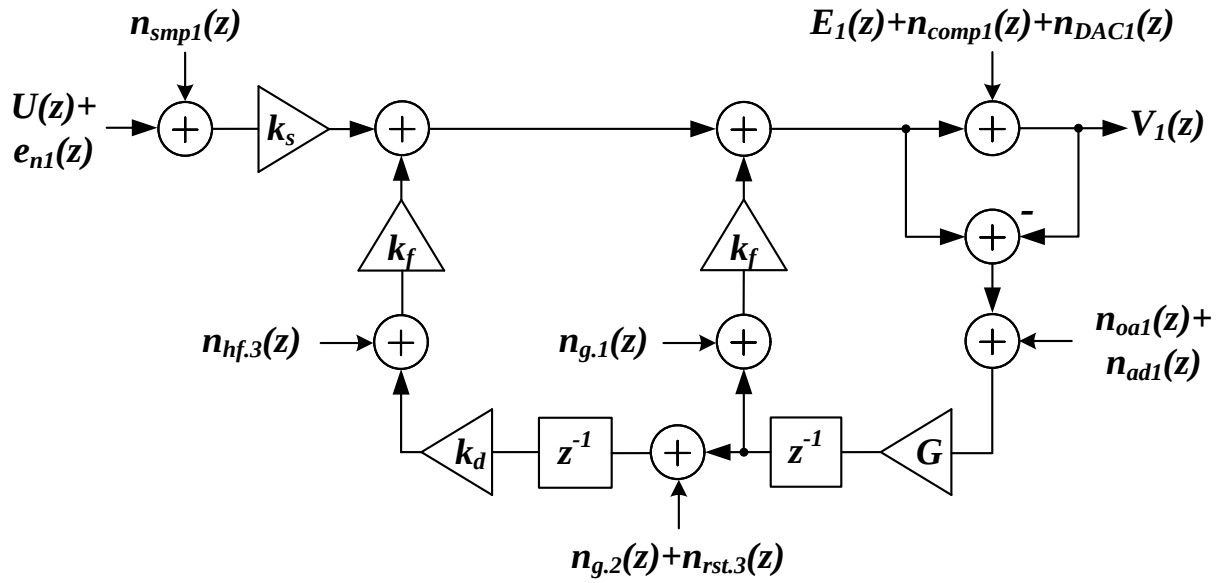



Figure 5.7 Block diagram of the first stage of the proposed IADC with the noise and charge sharing models

To investigate the impact of each IADC stage on the overall noise power, $e_{n1}[i]$ and $e_{n2}[i]$ are assumed to be the input-referred thermal noise for the first stage and the second stage, respectively. Since the first stage is re-used in the second step, a third stage with the input-referred thermal noise of $e_{n3}[i]$ is assumed to simplify the analysis. Considering Fig. 5.7 and the similar procedure presented in [55], the following expression is obtained:

$$\begin{aligned} -W_6[M_2] = {} & k_s^3 \cdot \frac{M_1^4 M_2^2}{4! \times 2!} \cdot \widetilde{U} + k_s^3 \cdot \frac{M_2^2}{2!} \cdot \sum_{l=1}^{M_1-1} \sum_{q=1}^{l-1} \sum_{j=1}^{q-1} \sum_{i=1}^{j-1} e_{n1}[i] \\ & + k_s^2 \cdot \frac{M_2^2}{2!} \cdot \sum_{j=1}^{M_1-1} \sum_{i=1}^{j-1} e_{n2}[i] + k_s \cdot \sum_{j=1}^{M_2-1} \sum_{i=1}^{j-1} e_{n3}[i] \\ & - k_s^2 \cdot \frac{M_2^2}{2!} \cdot \sum_{l=1}^{M_1-1} \sum_{q=1}^{l-1} \sum_{j=1}^{q-1} \sum_{i=1}^{j-1} V_1[i] - k_s \cdot \frac{M_2^2}{2!} \cdot \sum_{j=1}^{M_1-1} \sum_{i=1}^{j-1} V_2[i] - \sum_{j=1}^{M_2-1} \sum_{i=1}^{j-1} V_3[i] \end{aligned} \tag{5.42}$$

Therefore, the output signal power is given by:

$$P_{sig} = (k_s^3 \cdot \frac{M_1^4 \cdot M_2^2}{4! \cdot 2!})^2 \cdot \widetilde{U}^2 = k_s^6 \cdot A_{sig}^2 \cdot \widetilde{U}^2 \tag{5.43}$$

where $A_{sig}$ is defined as the signal gain from the input to the output of IADC.

$$A_{sig} = \frac{M_1^4 \cdot M_2^2}{4! \cdot 2!} \tag{5.44}$$

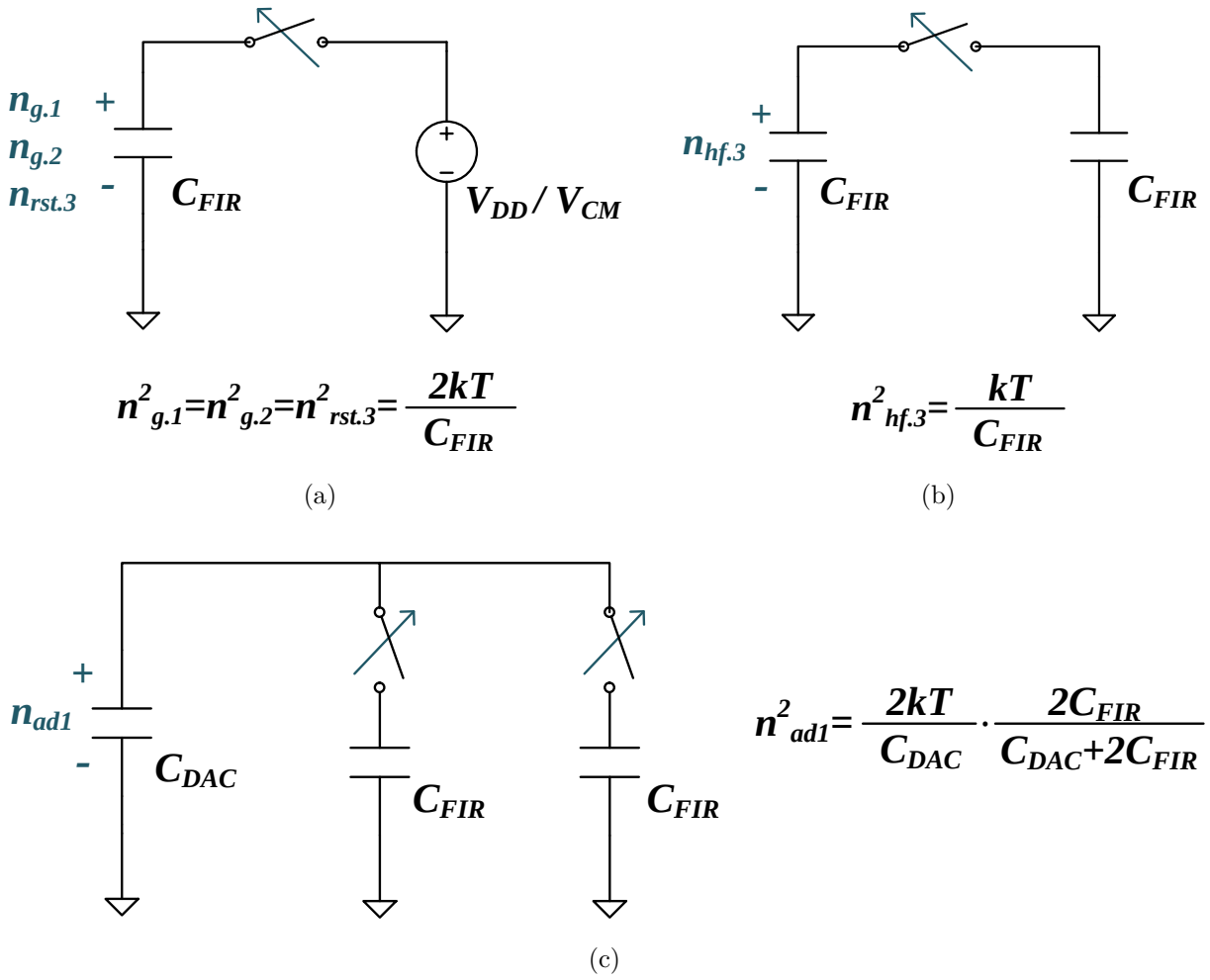



Figure 5.8 Derivation of the FIR filter noise power, which is stored in capacitors followed by (a) phase $\Phi_{RST}$ and $\Phi_G$, (b) phase $\Phi_{HF}$, (c) phase $\Phi_{AD}$ [39]

Since the noise signal variance is time-invariant, i.e., $Var(e_{n1}[i]) = Var(e_{n2}[i]) = Var(e_{n3}[i]) = \sigma_{thi}^2$, the output noise power caused by the input-referred thermal noise of the third stage, $\sigma_{tho3}^2$, is estimated form (5.42) as given by the following expression:

$$\sigma_{tho3}^2 \simeq k_s^2 \cdot ((M_2 - 1)^2 + (M_2 - 2)^2 + \cdots + 1^2) \cdot \sigma_{thi}^2 \simeq \frac{M_2^3 \cdot k_s^2}{3} \cdot \sigma_{thi}^2 \tag{5.45}$$

Employing a similar process used in (5.45), the output noise power resulted from the input-referred thermal noise of the first and second stages are achieved as follows:

$$\sigma_{tho1}^2 \simeq \frac{M_1^7 \cdot M_2^4 \cdot k_s^6}{7 \cdot 3!^2 \cdot 2!^2} \cdot \sigma_{thi}^2 \tag{5.46}$$

$$\sigma_{tho2}^2 \simeq \frac{M_1^3 \cdot M_2^4 \cdot k_s^4}{3 \cdot 2!^2} \cdot \sigma_{thi}^2 \tag{5.47}$$

As expressed in (5.48), for $M_1 > 5$, the noise power of the second and third stages are negligible compared to the first stage.

$$\sigma_{tho1}^2 = \frac{M_1^4 \cdot k_s^2}{7 \cdot 3! \cdot 2!} \cdot \sigma_{tho2}^2 = \frac{M_1^7 \cdot M_2 \cdot k_s^4}{7 \cdot 3! \cdot 2!^2} \cdot \sigma_{tho3}^2 \tag{5.48}$$

Therefore, the output thermal noise-limited SNR, i.e., $SNR_{th,out}$, is given by:

$$SNR_{th,out} = \frac{P_{sig}}{\sigma_{tho1}^2} = \frac{7 \cdot M_1}{16} SNR_{th,in} \tag{5.49}$$

It is concluded from (5.49) that the proposed IADC structure improves the $SNR_{th,in}$ by a ratio of $\frac{7}{16} \cdot M_1$. Such improvement, which is achieved using noise shaping and oversampling techniques, is defined as the noise-reduction-ratio (NRR) [7]. The NRR also expresses the ratio of the input-referred thermal noise power, $\overline{v_{n,in}^2}$, to the actual input thermal noise power, $\overline{v_{an,in}^2}$, as follows:

$$NRR = \frac{\overline{v_{n,in}^2}}{\overline{v_{an,in}^2}} = \frac{\sigma_{tho1}^2}{\sigma_{thi1}^2} \frac{1}{A_{sig}^2} \tag{5.50}$$

According to Fig. 5.7 and Fig. 5.8, the actual input-referred noise power is calculated as follows:

$$\begin{aligned} \overline{v_{an,in}^2} = n_{smp1}^2 + 0.25 \cdot \frac{k_f^2}{k_s^2} \cdot (n_{rst.3}^2 + n_{hf.3}^2) + \frac{k_f^2}{k_s^2} \cdot n_{g.2}^2 + \frac{k_f^2}{k_s^2} \cdot n_{g.1}^2 \\ + \frac{(G \cdot k_f - 0.5 \cdot G \cdot k_f)^2}{k_s^2} \cdot (n_{oa1}^2 + n_{ad1}^2) = 1.78 \cdot n_{oa1}^2 + 3.5 \cdot \frac{k \cdot T}{C_{DAC1}} \end{aligned} \tag{5.51}$$

where $k = 1.38 \cdot 10^{-23}$ J/K is the Boltzmann constant and $T \simeq 300$ K is the room temperature. The OA noise power can be estimated as a fraction of the $\frac{k \cdot T}{C_L}$ according to its architecture, where the $C_L$ denotes the OA load capacitor. However, the OA noise power is kept in its

general form in this analysis. It is worth noting that actual input thermal noise power does not consider the effect of the noise-shaping and oversampling techniques. Therefore, we estimate the input-referred thermal noise by plugging (5.51) into (5.50).

$$\overline{v_{n,in}^2} = \frac{16}{7 \cdot M_1} \cdot (1.78 \cdot n_{oa1}^2 + 3.5 \cdot \frac{k \cdot T}{C_{DAC1}}) \tag{5.52}$$

Combining (5.52) and (5.41) yields:

$$\frac{16}{7 \cdot M_1} \cdot (1.78 \cdot n_{oa1}^2 + 3.5 \cdot \frac{k \cdot T}{C_{DAC1}}) = \frac{V_{ref}^2}{12 \cdot 2^{2 \cdot b}} \tag{5.53}$$

Studying the EF-NS-SAR ADCs shows that approximately 50% of the ADC total thermal noise power is produced by the OA [39, 59]. Using this approximation that is assumed to hold regardless of the OA topology, expression (5.53) can be rewritten as follows:

$$\frac{16}{7 \cdot M_1} \cdot (0.87 \cdot \frac{V_{ref}^2}{12 \cdot 2^{2 \cdot b}} + 3.5 \cdot \frac{k \cdot T}{C_{DAC1}}) = \frac{V_{ref}^2}{12 \cdot 2^{2 \cdot b}} \tag{5.54}$$

It must be noted that the DAC capacitor array of SAR1 is also used as the sampling capacitor in the proposed architecture. Therefore, employing (5.54), the minimum required sampling capacitor size to meet the target SNR is given by:

$$C_{DAC1,th} = \frac{42 \cdot k \cdot T \cdot 2^{2 \cdot b}}{(\frac{7 \cdot M_1}{16} - 0.87) \cdot V_{ref}^2} \tag{5.55}$$

Substituting $C_{DAC}$ in (5.29) with (5.55), the total OAs thermal noise-limited power consumption, $P_{OA_t,th}$, can be expressed as follows:

$$P_{OA_t,th} = \frac{17.5 \cdot \ln 2 \cdot (b+1) \cdot 2^{2 \cdot b} \cdot V_{ov} \cdot V_{DD} \cdot k \cdot T \cdot f_s}{(\frac{7 \cdot M_1}{16} - 0.87) \cdot V_{ref}^2} \tag{5.56}$$

On the other hand, to estimate the SAR thermal noise-limited power dissipation, the proper value of $C_{inv}$ and $C_C$ parameters in (5.40) should be investigated.

In SAR ADCs, the comparator capacitor load is generally approximated by the minimum inverter capacitor size, $C_{inv}$; however, this value must also satisfy the comparator thermal noise requirements. So, the comparator capacitor load is:

$$C_C \geq Max(C_{C,th}, C_{inv}) \tag{5.57}$$

The minimum inverter capacitor size, $C_{inv}$, is less than 3 fF for CMOS technologies that are more advanced than 350-nm [9]. However, since this part considers only the thermal noise, the $C_{inv}$ is neglected.

The $C_{C,th}$ is sized by performing a similar process employed to calculate the $C_{DAC1,th}$ size, i.e., taking the comparator input-referred noise power, $\overline{v_{nc,in}^2}$, as equal to the comparator quantization noise. Since the comparator noise is shaped by the NS-SAR loop-filter, its quantization noise is determined by the SAR ADC resolution, $b_s$. Accordingly, the value of $C_{C,th}$ is obtained by the following expression:

$$C_{C,th} = \frac{16}{7 \cdot M_1}\left(\frac{24 \cdot k \cdot T \cdot 2^{2 \cdot b_s}}{V_{ref}^2}\right) \tag{5.58}$$

From (5.55) and (5.58), the ratio of $C_{C,th}$ to $C_{DAC1,th}$ is expressed by (5.59).

$$\frac{C_{C,th}}{C_{DAC1,th}} \simeq \frac{1}{2^{2 \cdot (b - b_s)}} \tag{5.59}$$

The SAR ADCs total thermal noise-limited power dissipation, $P_{t,SAR,th}$, is formulated by injecting (5.55) and (5.59) into (5.40). Assuming $b_s = 4$ and $b > 12$-bit, the ratio of $\frac{C_{C,th}}{C_{DAC1,th}}$ is very small and can be replaced by zero in (5.40). Therefore, the $P_{t,SAR,th}$ is estimated as follows:

$$P_{t,SAR,th} \simeq 0.23 \cdot f_s \cdot C_{DAC1,th} \cdot V_{DD}^2 = \frac{9.66 \cdot k \cdot T \cdot 2^{2 \cdot b} \cdot V_{DD}^2 \cdot f_s}{(\frac{7 \cdot M_1}{16} - 0.87) \cdot V_{ref}^2} \tag{5.60}$$

Summing (5.56) and (5.60), the proposed IADC total thermal noise-limited power consumption, $P_{t,th}$, is given by:

$$P_{t,th} \simeq \frac{9.66 \cdot k \cdot T \cdot 2^{2 \cdot b} . V_{DD} . f_s}{(\frac{7 \cdot M_1}{16} - 0.87) \cdot V_{ref}^2} \cdot (1.82 \cdot \ln 2 \cdot V_{ov} \cdot (b + 1) + V_{DD}) \tag{5.61}$$

An analysis of thermal noise-limited power consumption that applies to the single-loop first, second, and third-order $\Delta\Sigma$ IADCs is presented in [7]. Considering that the first OTA consumes more than 50% of the $\Delta\Sigma$ IADCs power consumption, the results presented in [7] are extended to a six-order $\Delta\Sigma$ IADC, as follows:

$$SNR_{th,out,IADC} = \frac{11 \cdot M_{IADC}}{36} \cdot SNR_{th,in,IADC} \tag{5.62}$$

$$P_{t,th-IADC} \simeq \frac{35 \cdot \ln 2 \cdot (b+1) \cdot 2^{2 \cdot b} \cdot V_{DD} \cdot k \cdot T \cdot f_s}{M_{IADC} \cdot V_{ref}^2} \tag{5.63}$$

where $M_{IADC}$ is the oversampling ratio, $SNR_{th,out,IADC}$ is the thermal noise-limited SNR, and $P_{t,th-IADC}$ denotes the total power consumption of the six-order $\Delta\Sigma$ IADC. Comparing (5.62) with (5.49) illustrates that the proposed IADC provides the thermal noise-limited SNR and resolution, $b$, that are similar to those of the six-order $\Delta\Sigma$ IADC with the same oversampling ratio, $M_{IADC} = M = 1.5 \cdot M_1$.

Considering $V_{DD} = 1.8\ V$, $V_{ov} = 200\ mV$, and $b \geq 12$-bit, the power bound of the proposed IADC is estimated, $P_{t,th,max}$, by:

$$\begin{aligned} P_{t,th,max} &\simeq \frac{16.2 \cdot \ln 2 \cdot (b+1) \cdot 2^{2 \cdot b} \cdot V_{DD} \cdot k \cdot T \cdot f_s}{M \cdot V_{ref}^2} \cdot (1 + \frac{0.27 \cdot 1.8}{12+1}) \\ &\simeq \frac{17 \cdot \ln 2 \cdot (b+1) \cdot 2^{2 \cdot b} \cdot V_{DD} \cdot k \cdot T \cdot f_s}{M \cdot V_{ref}^2} \end{aligned} \tag{5.64}$$

A thermal noise-limited FoM, $FoM_{s,th}$, is utilized to compare the efficiency of two above-mentioned IADC architectures. Utilizing the Schrier FoM expression, the FoM difference between the proposed IADC and the six-order single-loop $\Delta\Sigma$ IADC at the same bandwidth is obtained by:

$$\Delta FoM_{s,th} = FoM_{s,th} - FoM_{s,th-IADC} = 10 \log(\frac{P_{t,th-IADC}}{P_{t,th}}) \simeq 3\ dB \tag{5.65}$$

According to (5.65), the proposed IADC improves the $FoM_{th}$ by 3-dB while it is expected to be an area-efficient solution because of its two-step hardware-sharing structure and replacing FLASH-based multi-bit quantizers with the SAR ADCs.

### 5.4.4 ADC Mismatch-limited Power Bound

The proposed IADC exploits two main capacitor networks found in the DAC array and in the SC FIR filter, which are assumed to be network $n1$ and $n2$, respectively, in this paper. The proposed IADC power consumption is estimated by determining the maximum acceptable mismatch for each network according to the desired resolution.

DAC unit capacitor mismatch limits the ADC linearity, which is defined by the peak-differential-nonlinearity (DNL) and peak-integral-nonlinearity (INL). By modeling the DAC unit capacitor, $C_U$, as an independent identically-distributed Gaussian random variable, the

worst-case variance of DNL, which is larger than that of the INL, is achieved [60].

$$\sigma_{max} = \sqrt{2^b - 1} \cdot \sigma(\frac{\Delta C_U}{C_U}) \cdot LSB \tag{5.66}$$

where $\sigma(\frac{\Delta C_U}{C_U})$ is the standard deviation of the DAC unit capacitor mismatch. For a $b$-bit resolution ADC, it is required to meet $3 \cdot \sigma_{max} \leq 0.5 \cdot LSB$. Therefore, the standard deviation of the DAC unit capacitor is obtained by:

$$\sigma(\frac{\Delta C_U}{C_U}) \leq \frac{1}{6 \cdot \sqrt{2^b - 1}} \tag{5.67}$$

The metal-insulator-metal (MIM) capacitor parameters are usually considered to estimate the DAC unit capacitor size according to its standard deviation [8]:

$$\sigma(\frac{\Delta C_U}{C_U}) = \frac{K_\sigma}{\sqrt{A}} \tag{5.68}$$

$$C_U = K_c \cdot A \tag{5.69}$$

where $K_c$ is the capacitor density, $A$ is the capacitor area, and $K_\sigma$ is the mismatch parameter. By plugging $A$ derived from (5.68) into (5.69), the DAC unit capacitor value is estimated by:

$$C_U \geq 36 \cdot (2^b - 1) \cdot K_\sigma^2 \cdot K_c \tag{5.70}$$

The $K_\sigma = 1\%$ $\mu$m and $K_c = 1$ fF/$\mu$m$^2$ are considered for CMOS technologies more advanced than 350-nm [9]. Assuming a 4-bit SAR ADC, the DAC capacitor size constrained by the DAC unit capacitor mismatch, i.e., $C_{DAC-n1} = 2^4 \cdot C_U$, is determined by:

$$C_{DAC-n1} \geq 576 \cdot (2^b - 1) \cdot K_\sigma^2 \cdot K_c \simeq 5.76 \cdot 10^{-17} \cdot (2^b - 1) \tag{5.71}$$

Replacing $C_{DAC}$ in (5.29) with (5.71) results in the OAs total power consumption constrained by the DAC unit capacitor mismatch, $P_{OA_t,mis1}$, to be expressed as follows:

$$\begin{aligned} P_{OA_t,mis1} &\simeq 0.42 \cdot \ln 2 \cdot (b+1) \cdot V_{ov} \cdot V_{DD} \cdot C_{DAC-n1} \cdot f_s \\ &\simeq 2.42 \cdot 10^{-17} \cdot (2^b - 1) \cdot (b+1) \cdot \ln 2 \cdot f_s \cdot V_{ov} \cdot V_{DD} \end{aligned} \tag{5.72}$$

The expression (5.40) is employed to estimate the SAR ADC mismatch-limited power dissipa-

tion. The comparator capacitor load depends on the CMOS process and it is not mismatch-limited. Therefore, $C_C$ size is assumed negligible compared to $C_{DAC-n1}$. Consequently, the total SAR ADCs power consumption, which is limited by the DAC unit capacitor mismatch, is estimated by substituting $C_{DAC}$ with (5.71) in (5.40) as follows:

$$P_{t,SAR,mis1} \simeq 0.23 \cdot C_{DAC-n1} \cdot f_s \cdot V_{DD}^2 = 1.3 \cdot 10^{-17} \cdot (2^b - 1) \cdot f_s \cdot V_{DD}^2 \tag{5.73}$$

Summing (5.72) and (5.73), the proposed IADC total DAC unit capacitor mismatch-limited power dissipation is expressed as:

$$P_{t,mis1} \simeq 1.3 \cdot 10^{-17} \cdot (1 + 1.87 \cdot (b+1) \cdot \frac{V_{ov}}{V_{DD}}) \cdot f_s \cdot V_{DD}^2 \tag{5.74}$$

It is worth noting that if a DAC mismatch calibration is utilized, the IADC mismatch-limited power is determined only by the FIR capacitors mismatch.

To estimate the IADC power bound limited by the FIR capacitors mismatch, we formulate the effect of the mismatch on SNDR of the IADC. In this paper, the mismatch caused by the network $n2$, i.e., the FIR capacitors, is defined by:

$$\alpha = \frac{\Delta C_{FIR}}{C_{FIR}} \tag{5.75}$$

As depicted in Fig. 5.7, in the proposed IADC, the NTF in each stage, $NTF_{stage}(z)$, is given by:

$$NTF_{stage}(z) = (1 - G \cdot k_f \cdot z^{-1} + G \cdot k_f \cdot k_d \cdot z^{-2}) \tag{5.76}$$

The zero locations of an ideal NTF expression are on the unit-circle in z-domain. According to (5.14) and (5.15), the FIR capacitors mismatch changes the charge sharing coefficients, i.e., $k_f$, and $k_d$. From (5.76), any variation in $k_f$ and $k_d$ values changes the NTF coefficients and hence the NTF zero locations. In the following expressions, parameters $k'_f$ and $k'_d$ represent the values of $k_f$ and $k_d$ considering their variation caused by the FIR capacitors mismatch.

$$k'_d = k_d \cdot (1 + \frac{\Delta k_d}{k_d}) = \frac{C_{F1.2} + \Delta C_{F1.2}}{C_{F1.2} + \Delta C_{F1.2} + C_{F1.3}} = \frac{k_d + k_d \cdot \alpha}{2 + k_d \cdot \alpha} \simeq k_d \cdot (1 + \alpha) \tag{5.77}$$

$$k'_f = k_f \cdot (1 + \frac{\Delta k_f}{k_f}) = \frac{C_{F1.1} + \Delta C_{F1.1}}{C_{F1.1} + \Delta C_{F1.1} + C_{F1.3} + C_{DAC}} = \frac{k_f + k_f \cdot \alpha}{1 + k_f \cdot \alpha} \simeq k_f \cdot (1 + \alpha) \tag{5.78}$$

where $C_{F1.i} = C_{FIR}$ $(i = 1, 2, 3)$ and $C_{DAC} = 6 \cdot C_{FIR}$. It is also concluded from (5.77) and

(5.78) that the FIR capacitors mismatch results in the same coefficient variation values as shown by:

$$\alpha = \frac{\Delta C_{FIR}}{C_{FIR}} = \frac{\Delta k_d}{k_d} = \frac{\Delta k_f}{k_f} \tag{5.79}$$

Figure 5.9 shows the SNDR of the proposed IADC predicted by behavioral simulations that consider variations of the $k_d$ and $k_f$ coefficients.

Figure 5.9 illustrates that increasing $\alpha$ degrades the SNDR significantly. It is worth noting that the coefficient variations also cause a mismatch between the analog and digital parts of the proposed IADC. Therefore, the decimation filter should be modified to compensate for such mismatch. The decimation filter shown in Fig. 5.2 consists of the counter blocks with z-domain transfer function of $\frac{z^{-1}}{1-z^{-1}}$. For tuning the decimation filter, we assumed the transfer function of the counters to be $\frac{z^{-1}}{1-(1+\rho)\cdot z^{-1}}$. The maximum SNDR value for each $\alpha$ value is then achieved by varying the $\rho$. This tuning is performed along with the post-processing of the IADC outputs in MATLAB. Solid curves in Fig. 5.9 show the achieved SNDR versus the $\alpha$ employing the tuned decimation filter.

The following procedure estimates the acceptable FIR capacitors mismatch to achieve the target resolution. The fourth-order NTF assuming different mismatch values along with the ideal fourth and third-order NTFs are depicted in Fig. 5.10 to examine the impact of the capacitor mismatch on the NTF order. It is observed that although the NTF formulation maintains a fourth-order polynomial by increasing $\alpha$, the NTF curve slope becomes comparable to that of an ideal third-order NTF for $\alpha \simeq 0.07$ in lower frequencies, which are desired frequency values for IADCs. Accordingly, this paper assumes that the FIR capacitors mismatch can be translated to a decrease in NTF order by a non-integer value. Therefore, parameter $\eta$ is defined to represent the NTF order degradation caused by the mismatch.

Based on this observation, it is predicted that the SNDR of the proposed IADC can be estimated by considering $\eta$ in (5.6), as illustrated by the following expression:

$$\begin{aligned} SNDR_{mis} \simeq\ & (N_1-\eta)\cdot 20\cdot\log(M_1) + 20\cdot\log(L-1) + (\frac{N_1-\eta}{2})\cdot 20\cdot\log(M_1) \\ & - 20\cdot\log((N_1-\eta)!\cdot(\frac{N_1-\eta}{2})!) \end{aligned} \tag{5.80}$$

where $SNDR_{mis}$ is the SNDR of the proposed structure predicted by considering the FIR capacitors mismatch effect.

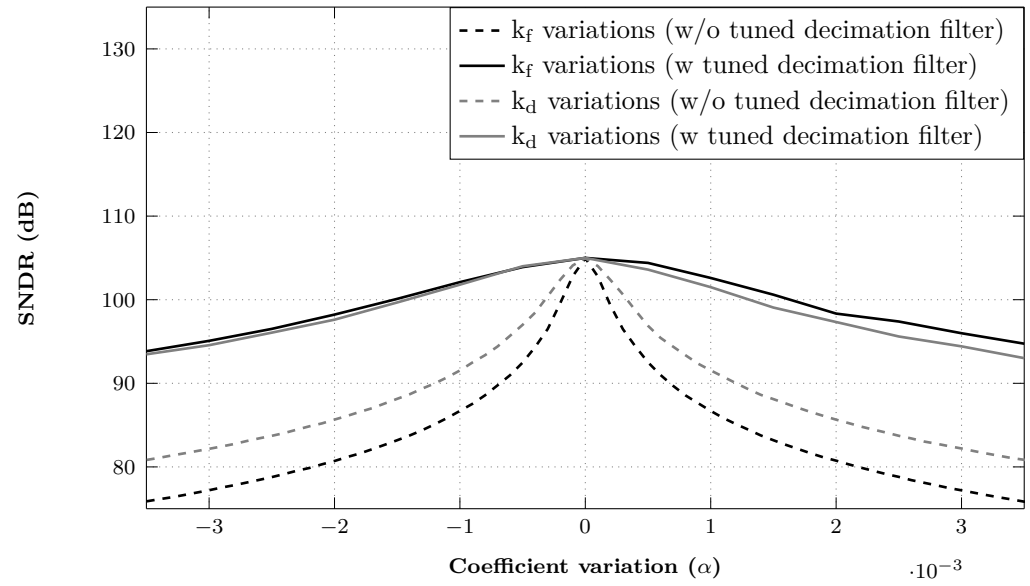



Figure 5.9 SNDR variations versus coefficient mismatch values with and without tuning the decimation filter to achieve the maximum SNDR values

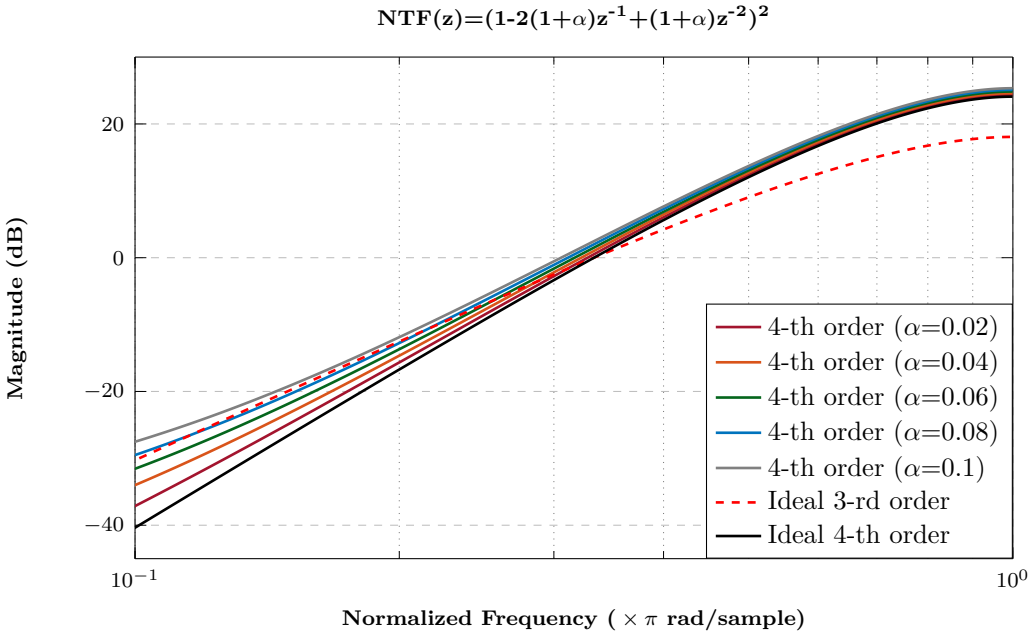



Figure 5.10 Fourth-order NTF performance for different mismatch values as compared with the ideal fourth and third-order NTFs

The relationship between the mismatch, $\alpha$, and the NTF degradation factor, $\eta$, is then investigated by fitting calculation and simulation results as follows. These results are reported in Fig. 5.11 that plots the SNDR values obtained from (5.80) for $\eta\epsilon[-0.55, 0.55]$ compared to simulation results presented in Fig. 5.9 using the tuned decimation filter for

$\alpha\epsilon[-0.0035, 0.0035]$, at $M = 24$, i.e., $M_1 = 16$ and $M_2 = 8$. Comparing $\alpha$ and $\eta$ values at each SNDR value, their relation can be estimated as:

$$\alpha \simeq \frac{0.01}{1.5} \cdot \eta = 6.7 \cdot 10^{-4} \cdot \eta \tag{5.81}$$

Combining (5.80) with (5.81), the relation between the SNDR of the proposed IADC and the FIR capacitors mismatch is expressed as follow:

$$\begin{aligned} SNDR_{mis} \simeq\ & (N_1 - 150 \cdot \alpha) \cdot 30 \cdot \log(M_1) \\ & - 20 \cdot \log((N_1 - 150 \cdot \alpha)! \cdot (\frac{N_1 - 150 \cdot \alpha}{2})!) + 20 \cdot \log(L - 1) \end{aligned} \tag{5.82}$$

The maximum proper $\alpha$ value, $\alpha_{max}$, according to the desired IADC resolution is achieved by solving (5.82) targeting a maximum 3-dB decrease in SNDR, i.e., LSB/2 degradation in IADC resolution. Therefore, using the MIM capacitor parameters and (5.68)-(5.69), the FIR and DAC capacitor sizes are expressed as follows:

$$C_{FIR} \geq \frac{K_\sigma^2 \cdot K_c}{\alpha_{max}^2} \tag{5.83}$$

$$C_{DAC-n2} \geq \frac{6 \cdot K_\sigma^2 \cdot K_c}{\alpha_{max}^2} \simeq \frac{6 \cdot 10^{-19}}{\alpha_{max}^2} \tag{5.84}$$

Replacing $C_{DAC-n1}$ in (5.72) and (5.73) with (5.84), the total FIR capacitors mismatch-limited power dissipation, $P_{t,mis2}$, is given by:

$$P_{t,mis2} \simeq \frac{1.38 \cdot 10^{-19}}{\alpha_{max}^2} \cdot (1 + 1.87 \cdot (b+1) \cdot \frac{V_{ov}}{V_{DD}}) \cdot f_s \cdot V_{DD}^2 \tag{5.85}$$

### 5.4.5 ADC CMOS Process-limited Power Consumption

The adopted CMOS fabrication process limits the ADC power consumption by determining the minimum size of the parasitic and explicitly implemented capacitors. The minimum parasitic capacitor size, $C_p$, is assumed to be comparable to the input capacitance of a minimum-sized inverter, which is less than 3 fF for 65-nm to 350-nm CMOS technologies [8,9]. However, the explicitly implemented capacitor, $C_{ex}$, size is estimated by the minimum MIM capacitor size, which varies significantly according to the utilized technology. For instance,

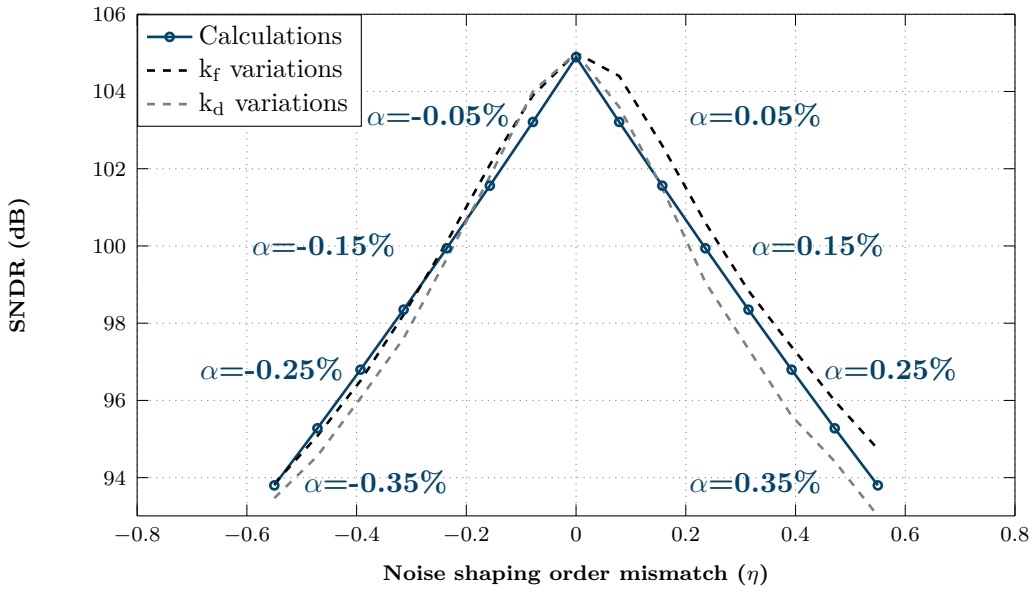



Figure 5.11 Comparisons of SNDR values, at $M = 24$, obtained from behavioral simulations for different coefficient mismatch, $\alpha$, and calculation results obtained by (5.80) for the various values of order degradation factor, $\eta$

it is approximately 5 fF and 20 fF in 65-nm and 180-nm CMOS technologies, respectively.

In the proposed IADC, $C_C$ is parasitic type, however, minimum $C_U$ size and hence $C_{DAC}$ size, i.e., $16 \cdot C_U$ for a 4-bit SAR ADC, is determined by $C_{ex}$ value. Replacing $C_{DAC}$ and $C_C$ with values achieved based on these assumptions in (5.29) and (5.40) results in power dissipation determined by the adopted CMOS process for the OAs, $P_{OA_t,process}$ and the SAR ADCs, $P_{t,SAR,process}$ as follows:

$$P_{OA_t,process} \simeq 4.62 \cdot (b+1) \cdot C_{ex} \cdot f_s \cdot V_{ov} \cdot V_{DD} \tag{5.86}$$

$$P_{t,SAR,process} \simeq (3.65 + \frac{C_p}{C_{ex}} \cdot \frac{37 \cdot V_{ov}}{V_{DD}} + \frac{214 \cdot C_p}{C_{ex}}) \cdot f_s \cdot C_{ex} \cdot V_{DD}^2 \tag{5.87}$$

Summing (5.86) and (5.87), the CMOS process-limited power consumption of the proposed IADC, $P_{t,process}$, is achieved by:

$$P_{t,process} \simeq (\frac{4.62 \cdot (b+1) \cdot V_{ov}}{V_{DD}} + 3.65 + \frac{C_p}{C_{ex}}(\frac{37 \cdot V_{ov}}{V_{DD}} + 214)) \cdot f_s \cdot C_{ex} \cdot V_{DD}^2 \tag{5.88}$$

### 5.4.6 Discussion

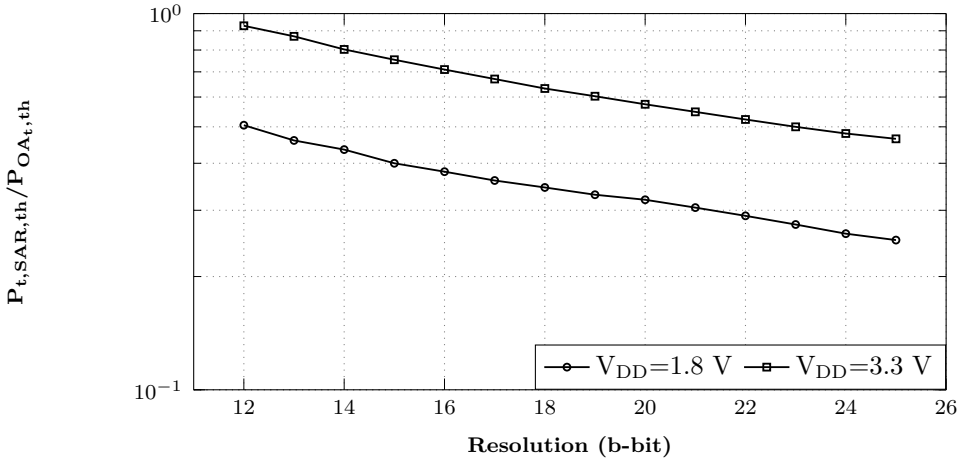
Leveraging the relationship derived earlier, it is now possible to produce a comprehensive overview of the power-efficiency of the proposed architecture. The following presented results are based on the parameters of 180-nm CMOS technology, i.e., nominal supply voltages of 1.8 V and 3.3 V, and minimum MIM capacitor size of 20 fF. It is also assumed that $V_{ov} = 200$ mV. It is worth noting that the same model and analysis can be applied in other CMOS technologies without loss of generality.

Figure 5.12 reports the ratio of the SAR ADCs power consumption to OAs power consumption. Figure 5.12(a) and (b) demonstrate that the OAs dominate the power dissipation dictated by thermal noise and DAC unit capacitor mismatch in all studied resolutions assuming $V_{DD} = 1.8$ V. However, the power consumption of the SAR ADCs is comparable with that of the OAs in low resolution NS-SAR IADCs when $V_{DD} = 3.3$ V. According to Fig. 5.12(c), SAR ADCs consume a significantly higher amount of CMOS process-limited power compared to the OAs. The higher SAR ADCs CMOS process-limited power consumption is due to the smaller $C_{DAC}$ size, which is comparable with the load capacitors of the comparator and SAR logic. In [40], the dominant OAs power consumption has been reported in amplifier-based NS-SAR ADCs. However, they achieve the highest FoMs and resolution while consuming low overall power consumption, as demonstrated in Fig. 5.1. Also, Table 5.2 confirms the accuracy of our presented analysis. It demonstrates that the expression (5.63) accurately estimates the power bound of [40] which uses static amplifiers, as assumed in this paper. However, the lower experimental power of [39], [41], and [43] is explained by the use of dynamic amplifiers.

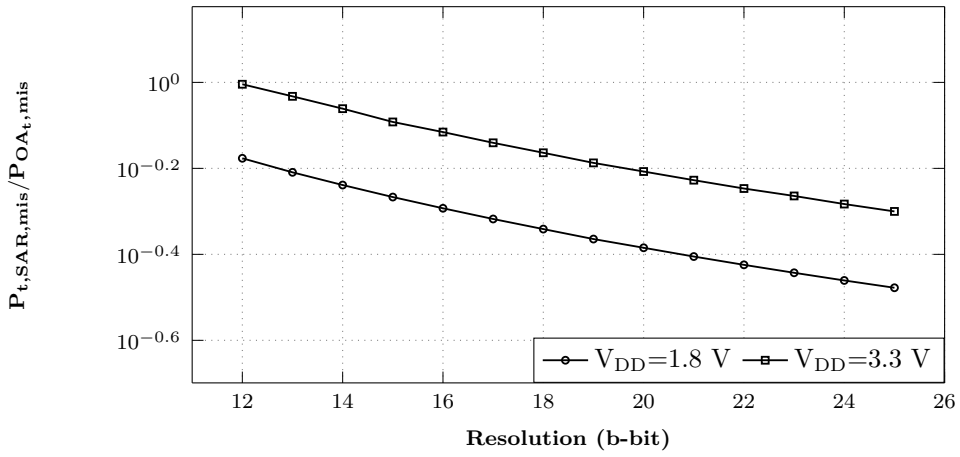
Table 5.2 Experimental and analytical results comparison

| Specifications | JSSC 2018 [39] | JSSC 2020 [41] | JSSC 2020 [40] | ISSCC 2021 [61] |
|---|---|---|---|---|
| Amplifier type | Open-loop dynamic | Closed-loop dynamic | Static | Open-loop FIDA* |
| Power ($\mu$W) Experimental | 84 | 107 | 120 | 119 |
| Power ($\mu$W) Eq. (5.63) | 221 | 263 | 108 | 343 |

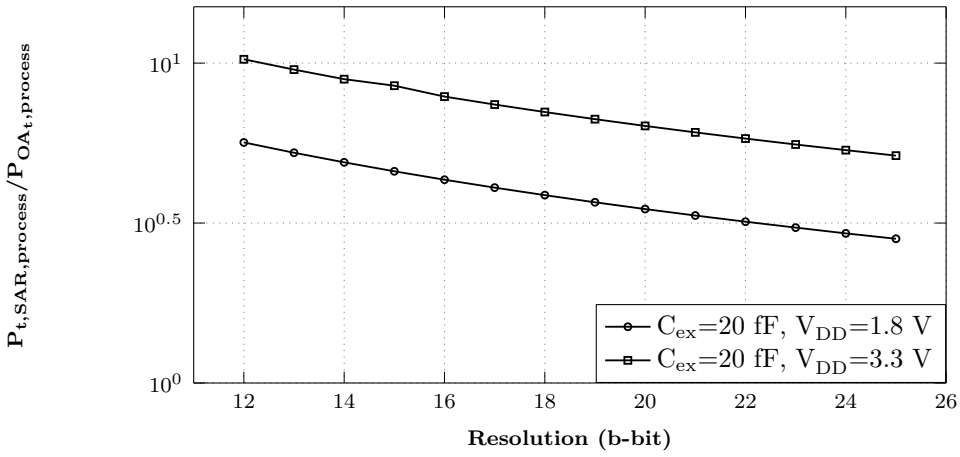
* floating inverter dynamic amplifier




(a)



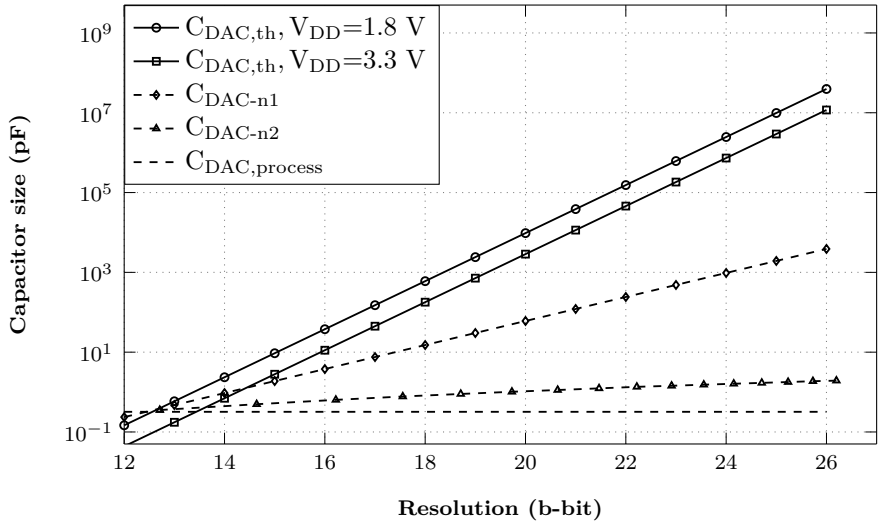

(b)



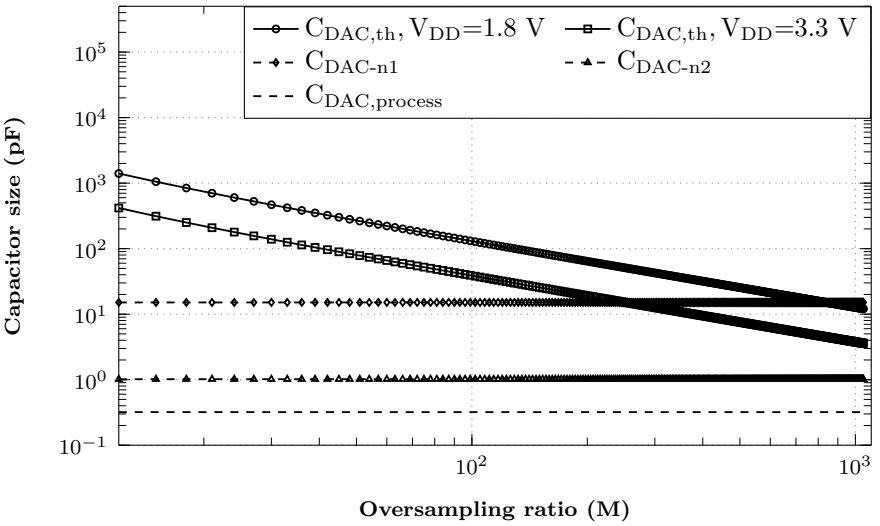

(c)

Figure 5.12 Ratio of the SAR ADCs power consumption to OAs power consumption achieved based on parameters of the 180-nm CMOS technology and by considering limitations due to (a) Thermal noise, (b) DAC unit capacitor mismatch, and (c) CMOS process

Figure 5.13(a) compares the DAC capacitor size bounded by thermal noise, mismatch, and CMOS process for a range of IADC resolutions. The analysis presented in this paper confirms that the proposed IADC power consumption is mainly related to the sampling capacitor, $C_{DAC}$, size. Therefore, significantly larger $C_{DAC,th}$ sizes in Fig. 5.13(a) predicts that thermal noise determines the minimum power consumption in high resolution values.




(a)




(b)

Figure 5.13 DAC capacitor size constrained by thermal noise, mismatch, and CMOS process considering parameters of 180-nm CMOS technology versus (a) resolution of the proposed IADC, and (b) oversampling ratio, M, for the 18-bit IADC resolution

The high values of thermal noise-limited capacitor, $C_{DAC,th}$, observed in Fig. 5.13(a) can be scaled down using techniques reported in [62, 63]. Figure 5.13(b) shows the $C_{DAC,th}$ size degradation caused by increasing the oversampling ratio when the target resolution is 18-

bit, for example. This technique was used to scale down the sampling capacitor size in [4] and [5] for 22-bit and 20-bit resolutions, respectively. In this case, the mismatch caused by the network $n_1$, i.e., the DAC array, becomes dominant in high oversampling ratios; however, employing a DAC mismatch calibration technique lowers the size of $C_{DAC-n1}$.

Figure 5.14, which compares power consumption limited by thermal noise, mismatch, and CMOS process normalized to the ADC sampling frequency, $f_s$, confirms the reported results obtained from Fig. 5.13. According to Fig. 5.14(a), thermal noise power bound is dominant for resolutions higher than 13-bit in $V_{DD} = 1.8$ V. Figure 5.14(b) also demonstrates that power bound is limited by thermal noise for resolutions higher than 15-bit in $V_{DD} = 3.3$ V. This observation agrees with the theory reported in [6], which predicts the dominant role of thermal noise in determining the ADCs performance. Figure 5.14(a) and (b) also demonstrate that the DAC unit capacitor mismatch is the second factor with the highest impact on the IADC power consumption in high resolutions. Therefore, a DAC mismatch calibration method is required to achieve a better IADC performance. However, the FIR capacitors mismatch and the CMOS process can constraint the IADC power-efficiency in resolutions less than 15-bit, as shown in Fig. 5.14(b). For a given CMOS technology, lowering the power supply voltage improves the CMOS process-limited IADC power-efficiency according to Fig. 5.14(a) compared to Fig. 5.14(b).

It must be noted that scaling down the sampling capacitor size in each resolution decreases the proposed IADC power consumption illustrated in Fig. 5.14(a) and (b) with the same rate shown in Fig. 5.13(b) as OSR is increased.

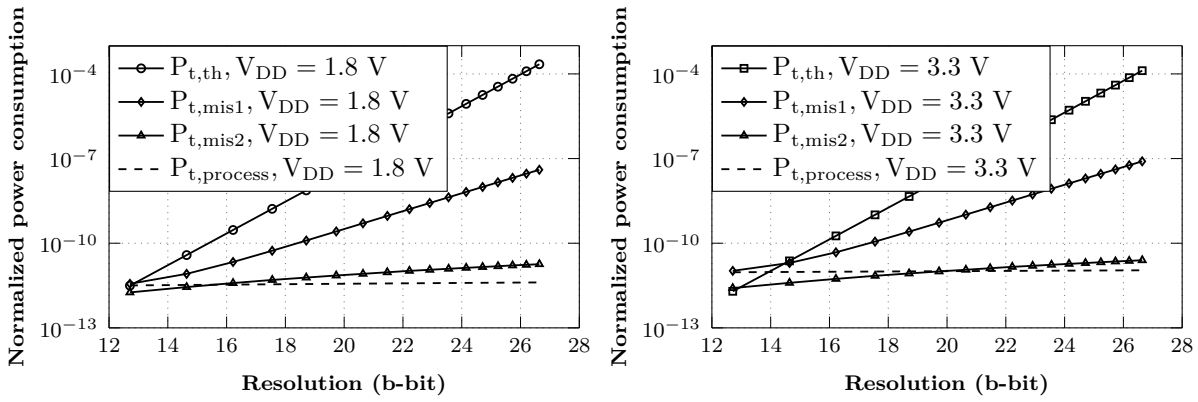



Figure 5.14 Comparing total power consumption normalized to the sampling frequency, $f_s$, limited by thermal noise, mismatch and CMOS process, considering minimum MIM capacitor size, $C_{ex} = 20$ fF, in 180-nm for (a) $V_{DD} = 1.8$ V, (b) $V_{DD} = 3.3$ V

## 5.5 Conclusion

A power bound analysis considering thermal noise, mismatch, and CMOS process limitations for our proposed two-step MASH NS-SAR IADC is presented. The obtained analytic results demonstrate that thermal noise determines the minimum power bound of the proposed structure. Assuming resolutions higher than 12-bit and $V_{DD} = 1.8$ V, the proposed IADC offers a 3-dB higher thermal noise-limited FoM than a single-loop $\Delta\Sigma$M IADC with the same parameters, i.e., noise-shaping order, OSR, and bandwidth, while the proposed architecture is expected to occupy less area. This paper predicts that the proposed IADC can achieve power and area-efficient performance in resolutions higher than 18 bits by scaling down the sampling capacitor size along with using a mismatch calibration technique and increasing the OSR. Analyzing the power consumption of the components used in the proposed IADC shows that SAR ADCs power consumption is negligible compared to the operational amplifiers. It is also demonstrated that the operational amplifier of the first stage dissipates more than 54% of the IADC total power consumption. Since the first-stage power consumption is dominant, the additional stages used to achieve higher resolutions do not considerably degrade the power-efficiency of the proposed IADC. The power bound for incremental NS-SAR ADCs, multi-stage, and multi-step topologies designed with different CMOS technologies can be obtained using the presented analysis.

# CHAPTER 6 PROTOTYPE IMPLEMENTATION: MASH 2-2 NS-SAR ADC

The following sections provide complementary information regarding the proposed MASH 2-2 NS-SAR ADC discussed in CHAPTER 3. This chapter discusses the effects of main non-idealities, circuit-level implementation of the sub-blocks, and integrated ADC chip design. The post-layout simulation results are also presented to verify the feasibility and performance of the proposed ADC.

## 6.1 Effect of Main Non-idealities

The analysis and performance presented in CHAPTER 3 are based on the ideal models. In order to investigate the effect of non-idealities and predict the performance of the proposed ADC structure before circuit implementation, a MATLAB code was generated. This code considers thermal noise, including $kT/C$ noise of capacitors and op-amps noise, capacitor mismatch, and op-amp gain error. This code also has an option to enable a DAC capacitors mismatch calibration based on the data weighted averaging (DWA) algorithm. It is worth noting that similar design parameters are considered for both stages of the proposed architecture. This section also discusses the differences in the architecture and specifications shown in CHAPTER 3 compared to what has been implemented.

### 6.1.1 Thermal Noise

#### $kT/C$ Noise of Capacitors

According to Fig. 3.2, there are two capacitance networks in the proposed structure, i.e., DAC and FILR filter. As mentioned earlier, the relationship between different capacitors is as follows:

$$C_{DAC} = 14 \cdot \ C_{FIR} \tag{6.1}$$

Fig. 6.1 shows that the $kT/C$ noise impact of smaller capacitor values on the ADC's performance is significant, especially on the SNDR of the proposed MASH structure. In order to limit the SNDR reduction of the ADC to 3-dB, the DAC capacitor size should be larger than 20 $pF$, which increases the ADC area.

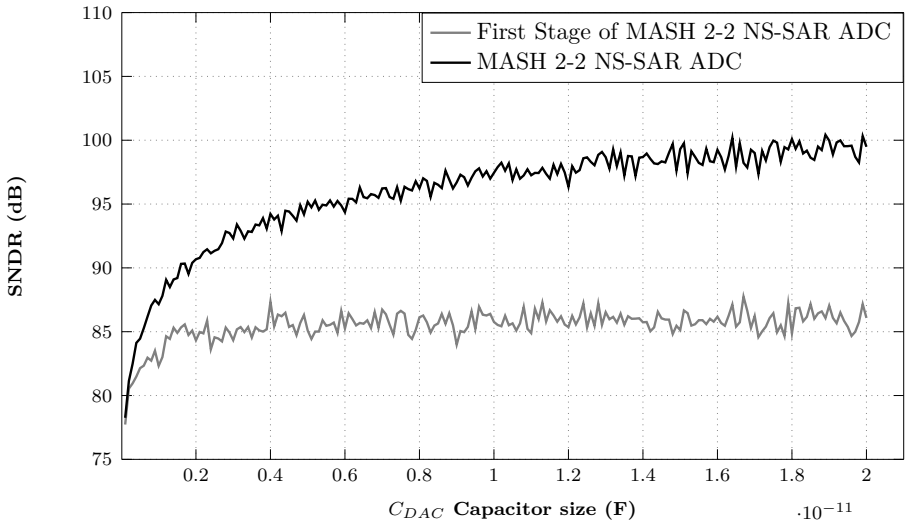



Figure 6.1 SNDR variations versus DAC capacitor size due to $kT/C$ noise effect

### Op-amp Thermal Noise

As mentioned in the literature, op-amp thermal noise significantly impacts NS-SAR ADCs' performance. Fig. 6.2 illustrates the SNDR variations of the first stage and overall output of the proposed ADC for different op-amps thermal noise values. It confirms that only a small amount of op-amps noise degrades the SNDR considerably. Also, as shown, for op-amps noise levels higher than 40 $\mu V_{rms}$, the SNDR improvement by MASH architecture degrades to less than 3-dB.

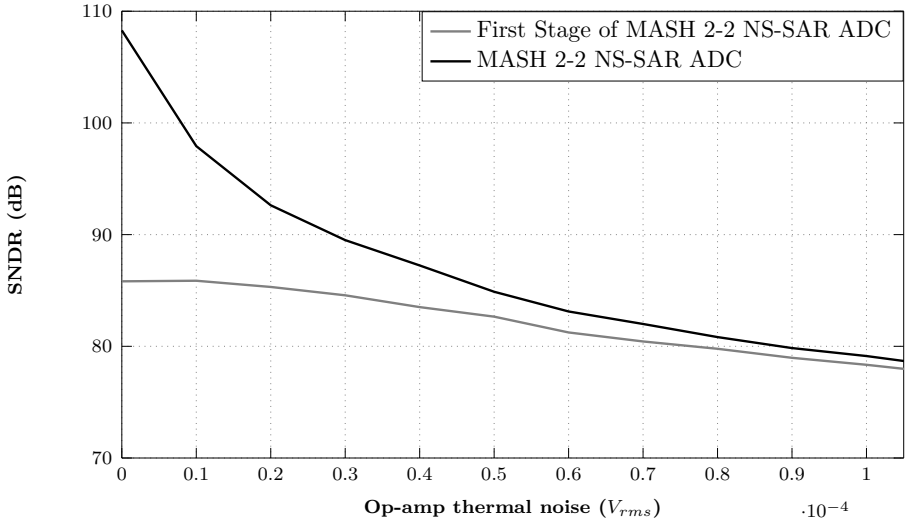



Figure 6.2 SNDR variations versus op-amp thermal noise

### 6.1.2 DAC Unit Capacitor Mismatch

Although the SAR ADC provides multi-bit quantization to obtain a power-efficient high-resolution performance, DAC mismatch limits the overall linearity [64]. Fig. 6.3 shows the SNDR variation due to a wide range of DAC unit capacitor mismatch values. As discussed earlier, the expected capacitor mismatch in modern technologies is less than 0.2%. Also, diverse mismatch calibration methods have been introduced to mitigate this issue [64–70]. A DWA algorithm was added to the MATLAB code to verify improving the proposed ADC performance using a mismatch calibration. Fig. 6.4 depicts the SNDR versus DAC mismatch after enabling the DWA algorithm. Comparing Fig. 6.4 with Fig. 6.3 illustrates that the mismatch calibration mitigates the worst-case SNDR reduction of the MASH structure by 20-dB. Also, the overall 30-dB SNDR degradation is reduced to 10-dB.

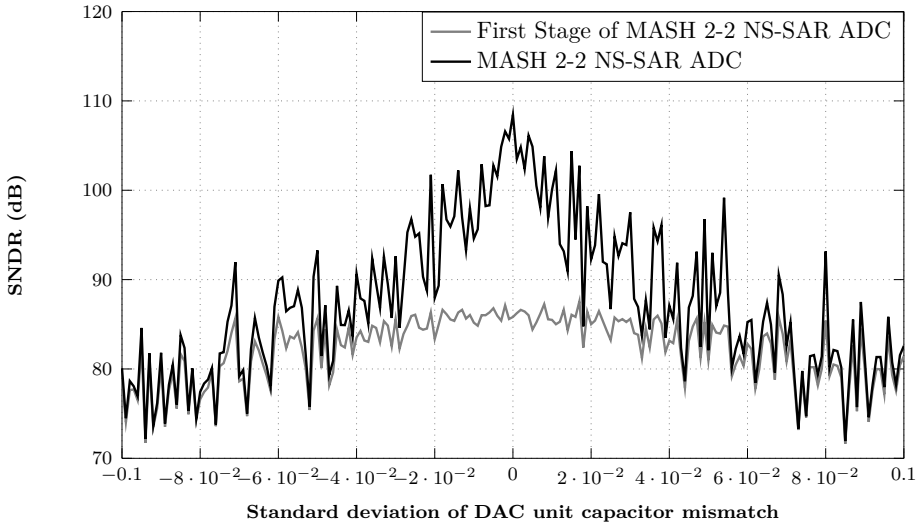



Figure 6.3 SNDR variations versus standard deviation of the DAC unit capacitor mismatch

The effect of DWA calibration on the power spectral density (PSD) of the proposed ADC and its first stage, assuming 10% DAC unit capacitor mismatch, is illustrated in Fig. 6.5 and Fig. 6.6. It is shown that the mismatch causes harmonics with significant powers. However, enabling the DWA mismatch calibration decreases the harmonics power and the base-band noise level by a first-order noise-shaping effect.

### 6.1.3 Op-amp Gain Variation

According to (3.3), the noise transfer function (NTF) of each stage and the overall proposed ADC are related to the op-amp gain used in the feedback path. Therefore, deviation in op-amp gain changes the zero positions of the NTF and, consequently, the ADC performance.

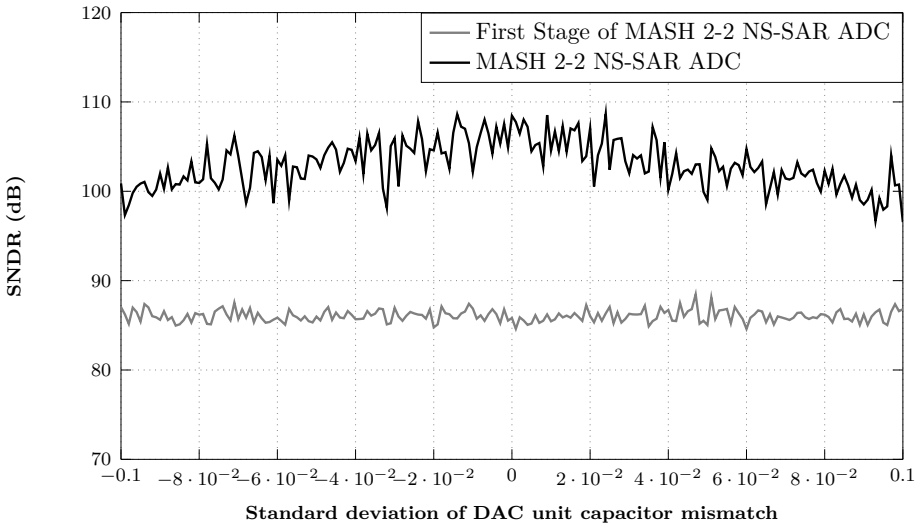



Figure 6.4 SNDR variations versus standard deviation of the DAC unit capacitor mismatch after using DWA mismatch calibration

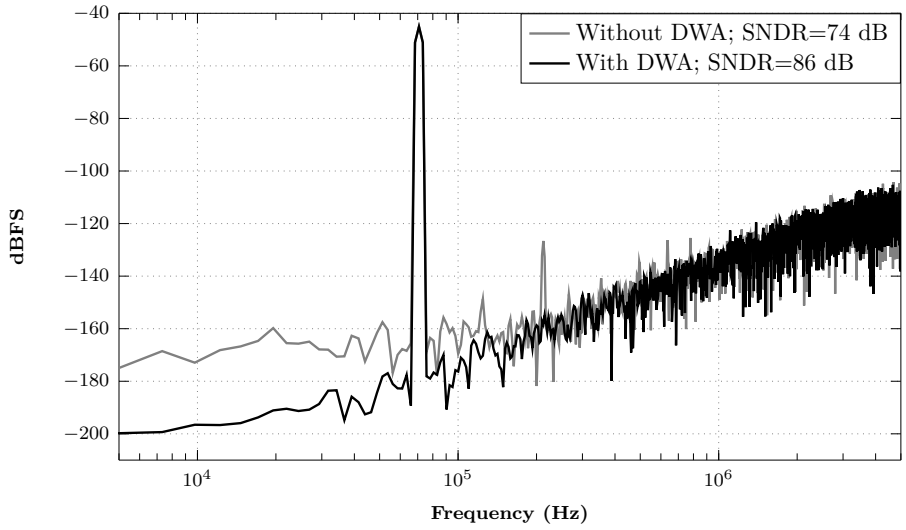



Figure 6.5 Power spectral density of the first stage of the proposed ADC considering 10% DAC unit capacitor mismatch with and without DWA mismatch calibration

The impact of the gain variation of op-amps on SNDR values of the proposed ADC and its first stage are presented in Fig. 6.7. It confirms that the proposed MASH architecture is still effective in improving the resolution since the op-amp gain variation degrades the SNDR of both cases similarly.

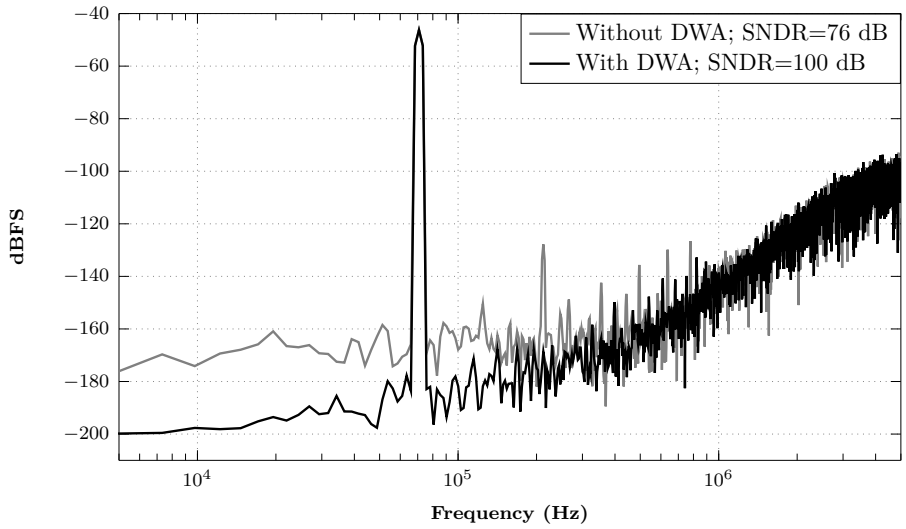



Figure 6.6 Power spectral density of the proposed ADC considering 10% DAC unit capacitor mismatch with and without DWA mismatch calibration

It is worth mentioning that the solid curve related to the MASH structure in Fig. 6.7 was generated using a digital cancellation logic (DCL) matched to the analog part. However, the dashed curve considers a DCL based on the nominal value of the op-amp gain. The leakage due to the mismatch between digital and analog parts degrades the SNDR in this case. Therefore, a calibration or tuning is required to estimate the actual value of the op-amp gain. A tuning method used in this project is discussed in the following section.

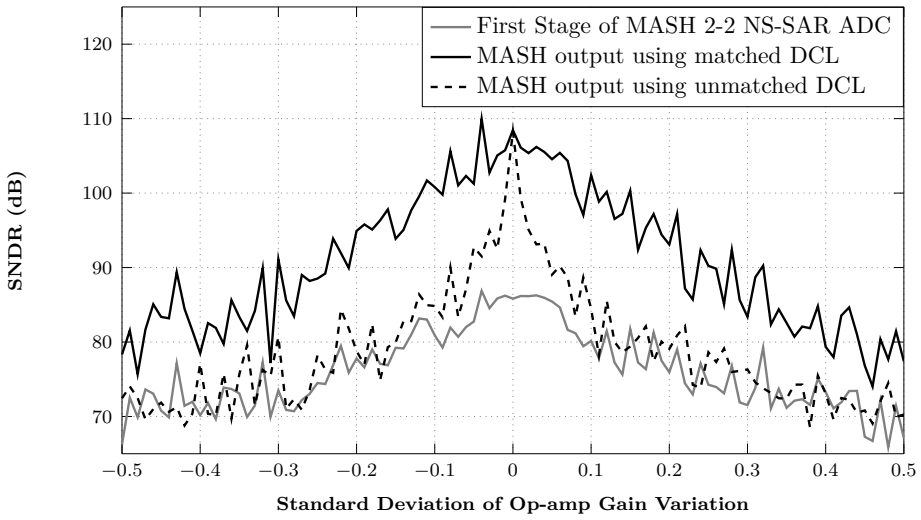



Figure 6.7 SNDR variations versus the standard deviation of op-amps gain changes ($\frac{\Delta G}{G}$)

### 6.1.4 Considerations

According to the analysis mentioned above and the results achieved by NS-SAR ADCs in the literature, we have made some changes compared to the specifications and model presented in CHAPTER 3 to relax the circuit design requirements. First, each stage uses a 6-bit quantizer instead of a 9-bit one. Second, the FIR filter was replaced by a ping-pong structure, discussed in the next section, to relax the op-amps linearity requirement. According to the mentioned changes, the required op-amp gain is reduced from 32 to 8. The simulation results for this case are discussed in the following part.

Fig. 6.8 shows that for the DAC capacitor values larger than 3 $pF$ the $kT/C$ noise impact on the SNDR is negligible.

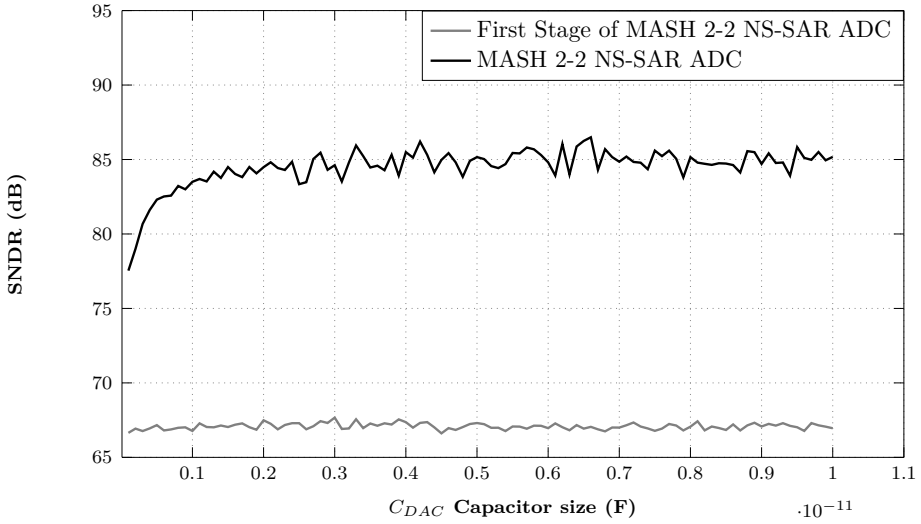



Figure 6.8 SNDR variations versus DAC capacitor size due to kT/C noise effect

According to Fig. 6.9, the SNDR improvement using the MASH structure is valid for a wide range of op-amps thermal noise levels. Also, the proposed structure tolerates an op-amps noise level of 40 $\mu V_{rms}$ with negligible degradation in the achieved SNDR compared to Fig. 6.2.

The thermal noise impact of each opamp, i.e., OA1 in the first stage and OA2 in the second stage, on the ADC performance is demonstrated in Fig. 6.10, independently. The OA1 has the dominant effect on the SNDR of the proposed ADC since its noise transfers directly to the output. However, the OA2 noise is shaped by $H_2(z)$ of the DCL.

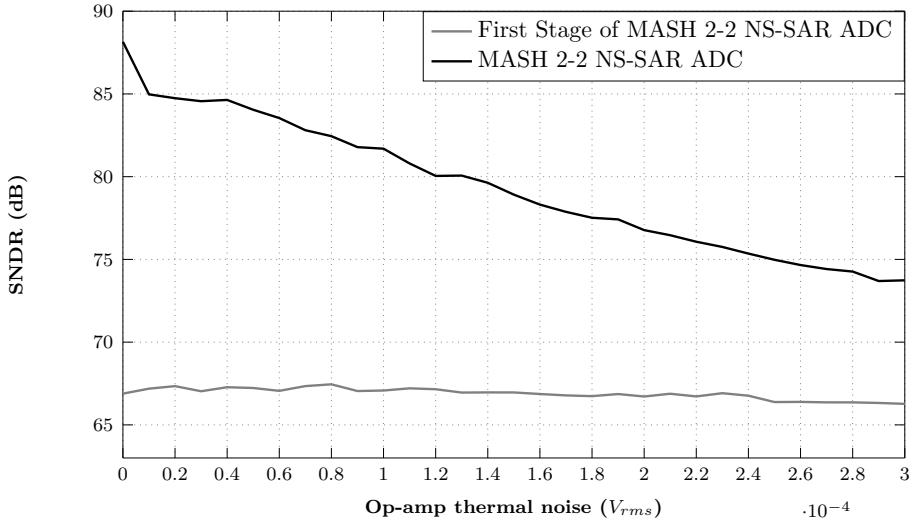



Figure 6.9 SNDR variations versus op-amps thermal noise

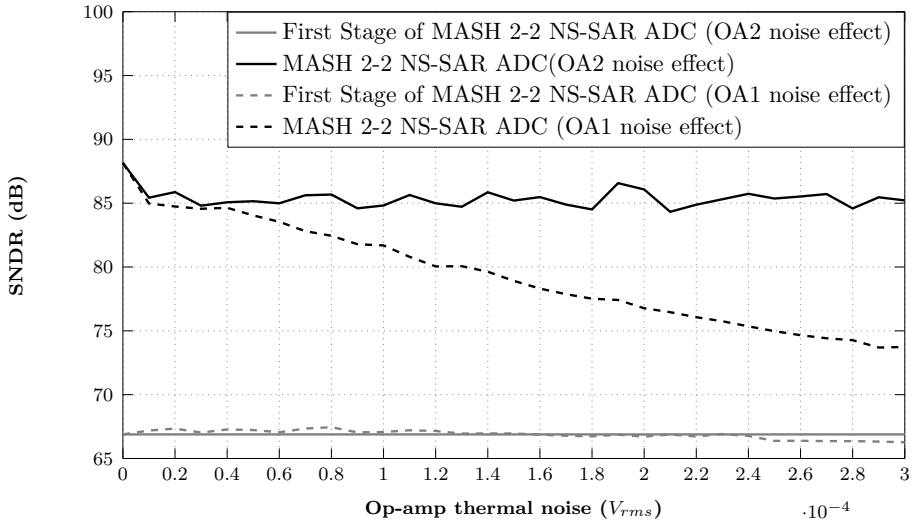



Figure 6.10 SNDR variations versus op-amps thermal noise

The impact of the DAC unit capacitor mismatch on the obtained SNDR is depicted in Fig. 6.11 with and without using the DWA calibration algorithm. It shows that the SNDR reduction of the MASH structure maintains less than 3-dB for 1% capacitor mismatch even without employing the DWA. However, using the DWA, the proposed ADC can tolerate a mismatch of 10%. Fig. 6.12 and Fig. 6.13 illustrate the effect of DWA calibration on the power spectral density (PSD) of both stages of the proposed ADC, assuming 10% DAC unit capacitor mismatch.

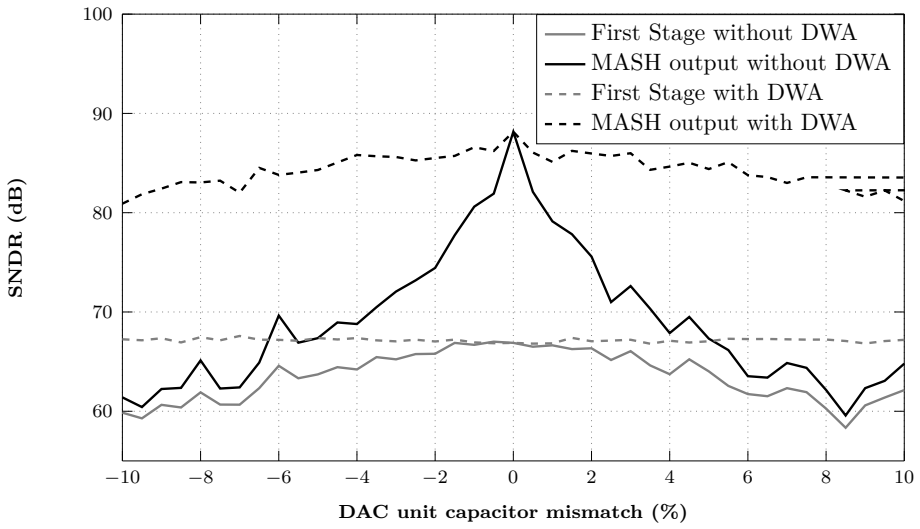



Figure 6.11 SNDR variations versus standard deviation percentage of DAC unit capacitor mismatch with and without using DWA calibration algorithm

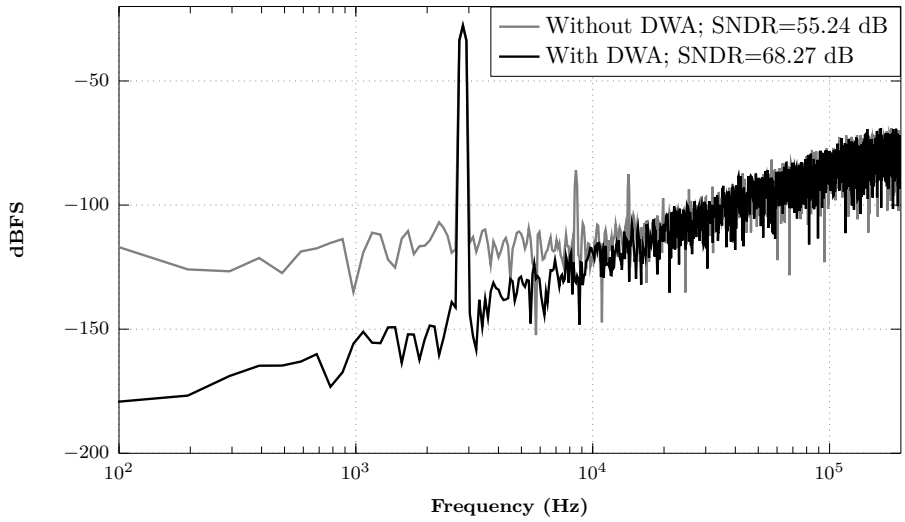



Figure 6.12 Power spectral density of the first stage of the proposed ADC considering 10% DAC unit capacitor mismatch with and without DWA mismatch calibration

Fig. 6.14 illustrates the impact of the op-amp gain variation on the performance of the ADC. Using a DCL matched to the NTF of the first stage, the MASH structure provides a 10-20 dB improvement in obtained SNDR. However, using the nominal value of op-amp gain in modeling the DCL, the SNDR degrades considerably. As mentioned earlier, the DCL tuning method is discussed in the next section.

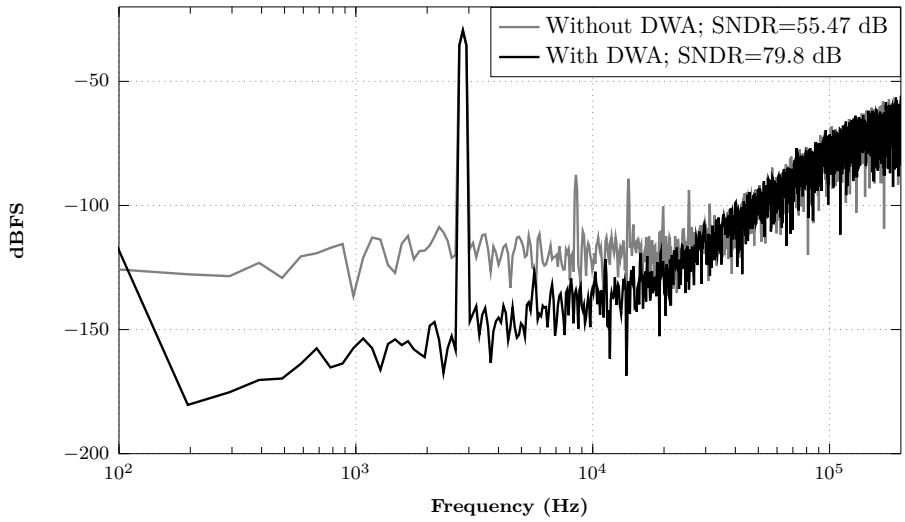



Figure 6.13 Power spectral density of the proposed ADC considering 10% DAC unit capacitor mismatch with and with DWA mismatch calibration

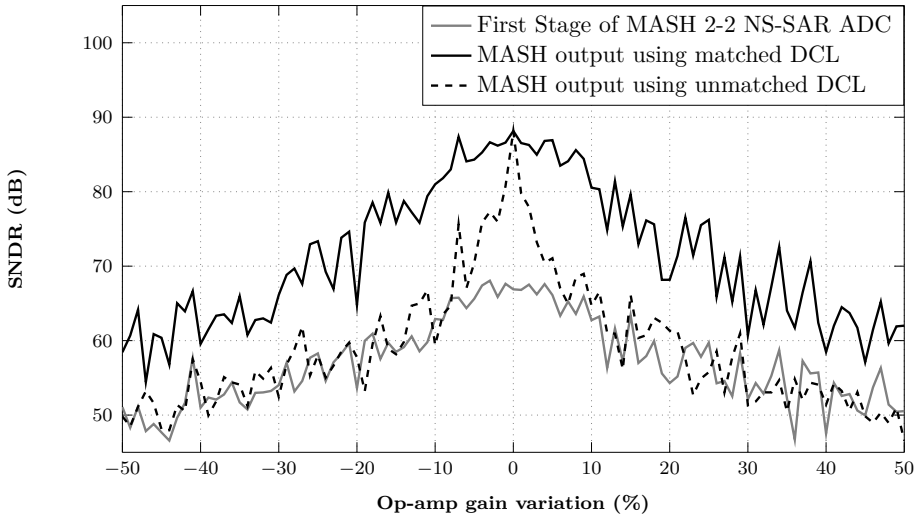



Figure 6.14 SNDR variations versus standard deviation percentage of op-amp gain variation considering the matched and unmatched DCL

## 6.2 Circuit Implementation

Circuit-level design of sub-blocks like transmission gate switch, comparator, digital control logic, capacitor array, and FIR filter are discussed in this section. Since matching is critical for NS-SAR ADCs, layout considerations to guarantee the matching are also discussed. Finally, the post-layout simulation results and the designed chip for the fabrication will be presented.

This circuit has been implemented using ST28-nm FD-SOI technology. It provides access to two main types of transistors, i.e., regular-threshold voltage (RVT) and low-threshold voltage (LVT). Also, three voltages, i.e., 1 $V$, 1.5 $V$, and 1.8 $V$, are available for each type of transistor. For designing the analog sub-blocks of the proposed ADC, 1-V and 1.8-V RVT transistors were used to have a higher signal level and follow the application requirements. However, the digital sub-blocks were implemented utilizing 1-V LVT transistors to achieve higher speed and lower power consumption. Therefore, level-up/down shifter sub-blocks have been used for changing the voltage level.

Fig. 6.15 and Fig. 6.16 illustrate the circuit design and the timing diagram for the proposed MASH 2-2 NS-SAR ADC, respectively. It is worth noting that there are the following differences compared to Fig. 3.2 presented in CHAPTER 3.

- Each stage uses a 6-bit SAR ADC instead of a 9-bit one to relax the circuit design requirements and challenges. This change increases the residue voltage amplitude at the op-amp input, limiting the op-amp voltage headroom and linearity. Therefore, it is required to decrease the op-amp gain.
- The FIR filter structure has been replaced by a ping-pong architecture which provides an inherent gain of 2. Therefore, op-amp gain can be decreased to half. The FIR filter circuit and operation are discussed in Section 6.2.
- According to the two first changes, the op-amp gain was decreased to $G = 8$. The residue voltage is amplified by a gain of 16 considering the inherent gain of the ping-pong FIR filter. Also, in order to achieve $NTF_{1,2}(z) = (1 - z^{-1})^2$ in each stage, the capacitor size ratios were chosen as follows:

$$NTF_1 = 1 - 2 \cdot G \cdot \frac{C_{F1.1}}{C_{DAC1} + C_{F2/3.1} + C_{F1.1}} \cdot z^{-1} + 2 \cdot G \cdot \frac{C_{F2/3.1}}{C_{DAC1} + C_{F2/3.1} + C_{F1.1}} \cdot z^{-2} \quad (6.2)$$

$$C_{F1.1} = 2 \cdot C_{F2/3.1} \quad (6.3)$$

$$C_{CDAC1} = 13 \cdot C_{F2/3.1} \quad (6.4)$$

According to CHAPTER 3, the signal transfer function (STF) and DCL transfer functions, i.e., $H_1(z)$ and $H_2(z)$ are described as follows:

$$STF_{1,2} = \frac{C_{DAC1/2}}{C_{DAC1/2} + C_{F1/2.1} + C_{F1/2.2}} = 0.8125 \quad (6.5)$$

$$H_1(z) = STF_2 = 0.8125 \quad (6.6)$$

$$H_2(z) = NTF_1 = 1 - 0.25 \cdot G \cdot z^{-1} + 0.125 \cdot G \cdot z^{-2} = (1 - z^{-1})^2 \quad (6.7)$$

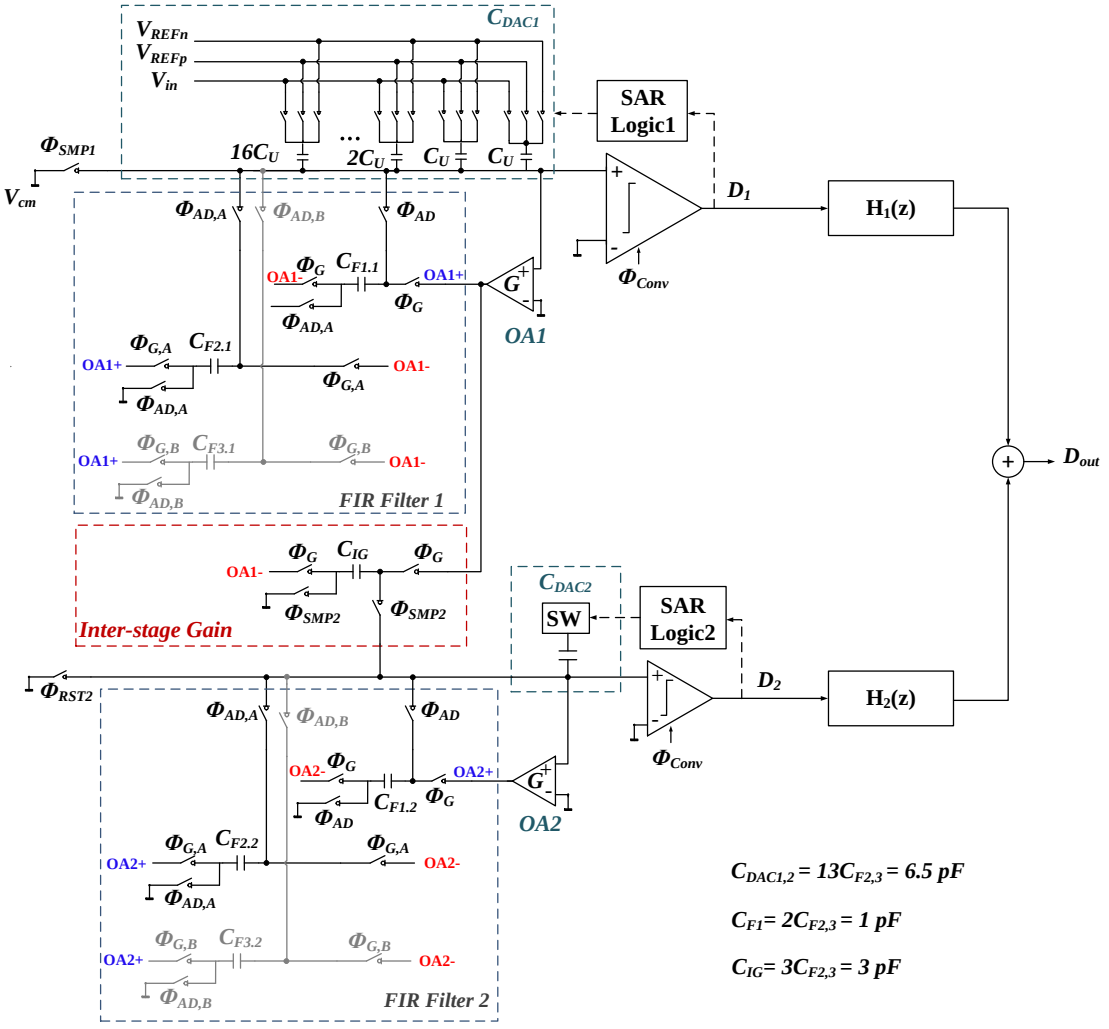



Figure 6.15 Circuit design of the proposed MASH 2-2 NS-SAR ADC using 6-bit SAR ADCs, ping-pong FIR filters and inter-stage gain

Investigating the effect of non-idealities shows that the real NTF and STF of the proposed ADC differ from what was mentioned above. As discussed in Fig. 6.7 and Fig. 6.14, and since the precise real NTF and STF is not available, a DCL tuning method is required. Therefore, the following expressions, i.e., $H_1'(z)$ and $H_2'(z)$, are assumed to estimate the tuned DCL.

$$H_1'(z) = 0.8125 \cdot (1 + \alpha_1) \tag{6.8}$$

$$H_2'(z) = NTF_1 = 1 - 0.25 \cdot G \cdot (1 + \alpha_2) \cdot z^{-1} + 0.125 \cdot G \cdot (1 + \alpha_2) \cdot z^{-2} \tag{6.9}$$

where $\alpha_1$ and $\alpha_2$ are due to $C_{DAC2}$ mismatch and op-amp gain error, respectively.

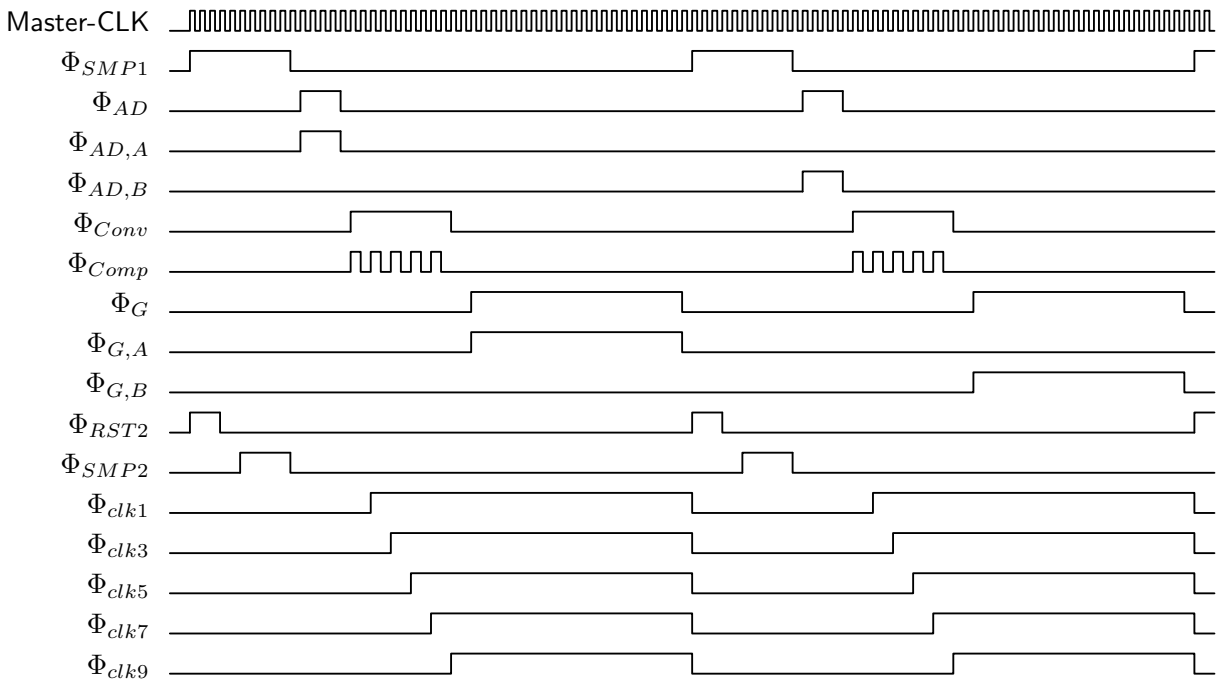



Figure 6.16 Timing diagram of the proposed MASH 2-2 NS-SAR ADC using 6-bit SAR ADCs, ping-pong FIR filters and inter-stage gain

The first and second stage output signals of the proposed ADC are post-processed in MATLAB using (6.8) and (6.9). Changing $\alpha_1$ and $\alpha_2$ tunes the DCL to search the maximum SNDR value for the proposed ADC. A calibration method can be used to estimate and tune the op-amp gain, but it is out of the scope of this thesis [39].

### 6.2.1 Capacitive DAC Array Design

According to Fig. 6.15, a 6-bit binary-weighted capacitive DAC is used to implement the proposed ADC. Table 6.1 lists the specifications and energy-saving of different DAC switching methods compared to the conventional one. It is illustrated that the $V_{cm}$-based method achieves around 90% energy saving with low logic complexity and no dependency on accuracy of $V_{cm}$ voltage. The $V_{cm}$-based switching method procedure is depicted in Fig. 5.6 while Fig. 6.17 shows the waveform of this switching method.

#### DAC Layout Considerations

The switched-capacitor circuit performance in ADCs is related to the accuracy of capacitor ratios. Capacitor mismatch causes two primary error sources, i.e., random mismatch and

systematic mismatch. The first type of error is because of the PVT variations. However, the latter is due to the asymmetrical layout, parasitic capacitances, and wire interconnections [81]. Paralleling unit capacitors (UC) with a common-centroid structure mitigates the systematic mismatch significantly. Several works have discussed parasitic-aware placement and routing for binary-weighted capacitors [81–84].

Table 6.1 Specifications of different DAC switching methods

| Schemes | Energy Saving | Logic Complexity | Dependency on the accuracy of $V_{cm}$ |
|---|---|---|---|
| Conventional [71] | Reference | Low | – |
| Capacitor splitting [72] | 37.48 % | Medium | No |
| Set and down [73] | 81.2 % | Low | – |
| Tri-level [74] | 96.89 % | Medium | Very high (except MSB) |
| $V_{cm}$-based Monotonic [75] | 97.66 % | Medium | Very high (except MSB) |
| $V_{cm}$-based [76] | 87.52 % | Low | No |
| Rahimi (2014) [77] | 93.7 % | Low | Very low (only LSB) |
| Xie (2015) [78] | 96.91 % | Medium | Very low |
| Yousefi (2018) [79] | 100 % | High | No |

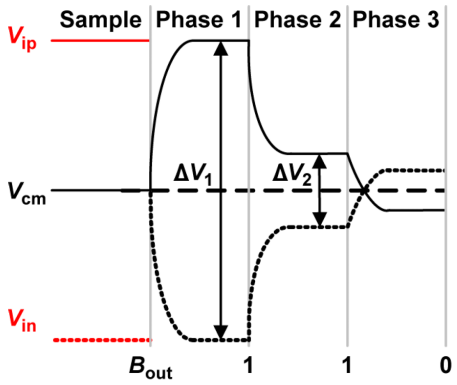



Figure 6.17 Waveform of $V_{cm}$-based DAC switching [80] (©[2010] IEEE)

Since generating an optimized UC placement is highly complex, the common-centroid UC placement and routing method presented in [81, 83] is employed for implementing the proposed ADC, as presented in Fig. 6.18. In this floor plan, the upper-plate and lower-plate routing channels are interchanged to facilitate the interconnection of unit capacitors. Dummy unit capacitors surround the floor-plan to degrade the mismatch due to unequal fringing caused by adjacent structures.

In ST28-nm FD-SOI technology, a metal-oxide-metal (MOM) capacitor can be used as the unit capacitor. A 1000-sample Monte-Carlo simulation has been performed to investigate the

impact of mismatch and process variations on the extracted UC value. As illustrated in Fig. 6.19, the variation of the extracted value of UC is less than 0.08%, which means the effect of this random mismatch on ADC performance is negligible according to Fig. 6.11.

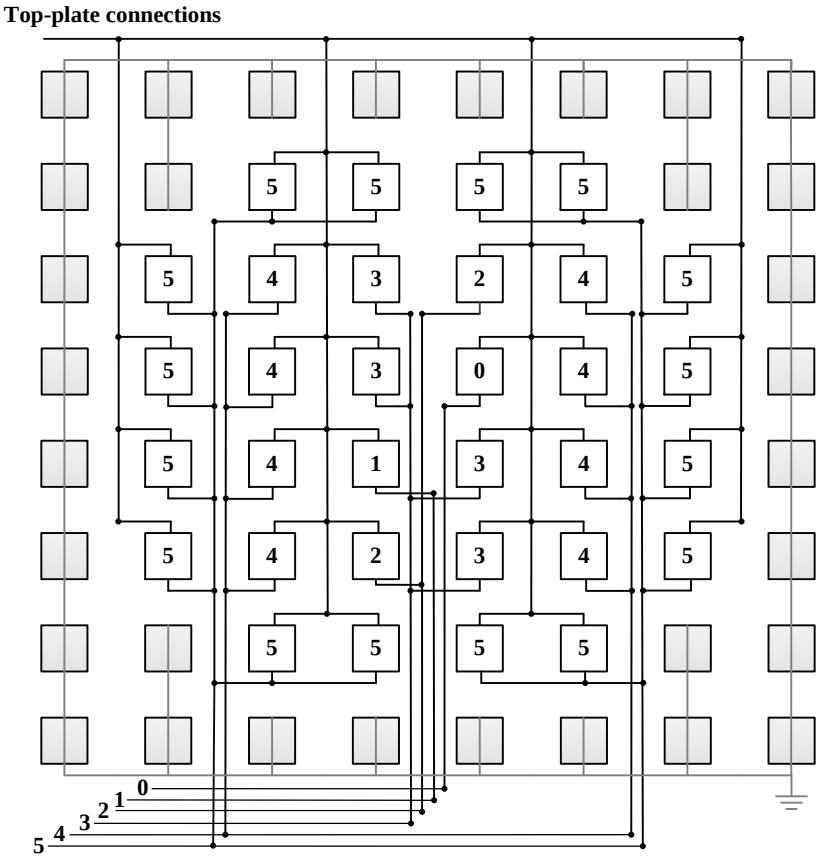



Figure 6.18 The floor-plan of 6-bit capacitive DAC used for implementing the proposed ADC

### 6.2.2 Comparator

The block diagram of the comparator used to design the proposed ADC is illustrated in Fig. 6.20. Ideally, a single latch block is required for the comparison operation. However, it is not feasible since it may suffer from the high offset, kickback noise, and meta-stability. Employing a pre-amplifier mitigates the offset and kickback noise, and the digital output logic reduces the meta-stability effect. Fig. 6.21 depicts the transistor-level design employed for each block of the comparator used in this work.

As discussed in CHAPTER 2, one of the most important advantages of NS-SAR ADC is shaping the comparator noise. Therefore, using a high-gain (or multi-stage) pre-amplifier

is not required to suppress the input-referred noise of the comparator. A single-stage amplifier with a cross-coupled load and gain of 20 dB has been used in this work. In order to suppress the effect of kickback noise from the amplifier to the CDAC, a pair of dummy NMOS transistors with shorted drain and source is connected between input and output of the pre-amplifier [85].

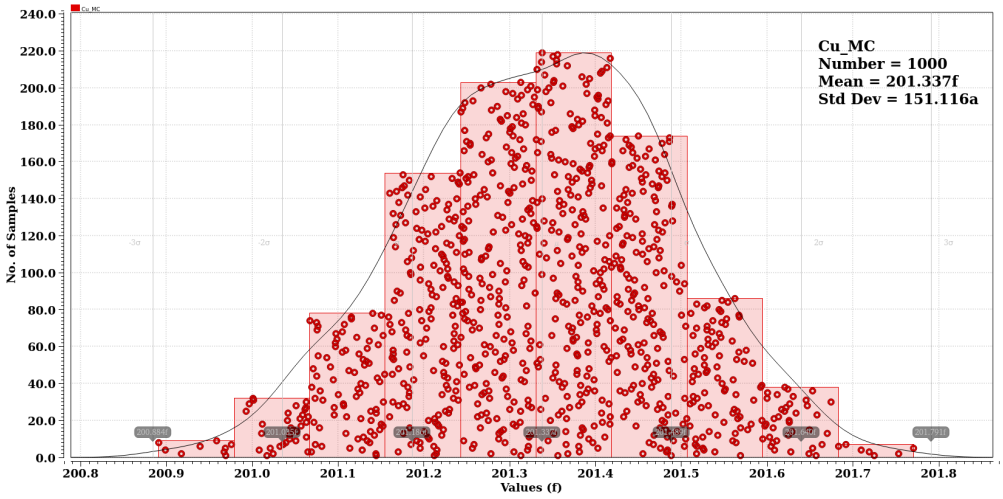



Figure 6.19 Monte-Carlo simulation results considering process and mismatch for the extracted value of DAC unit capacitor

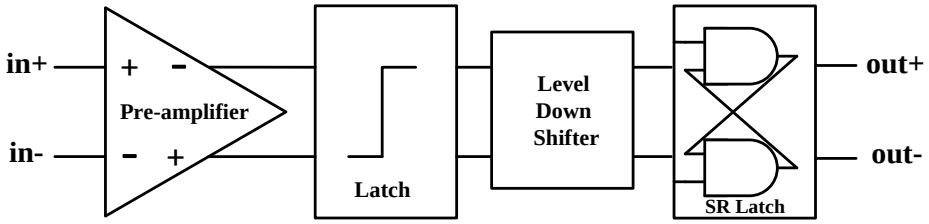



Figure 6.20 Comparator block diagram

After the pre-amplifier stage, a StrongARM latch is used because of its zero static power consumption and rail-to-rail output. Also, the input NMOS differential pair provides a gain that helps reduce the offset and input-referred noise [86].

An SR-latch is required at the output of the latch to mitigate the meta-stability issue. In case of a meta-stability error, both output nodes of the StrongARM latch remain close to $V_{DD}$, and the SR-latch keeps the previous values. Therefore, the error caused by metastability is limited to $\pm 1$ LSB of the comparator.

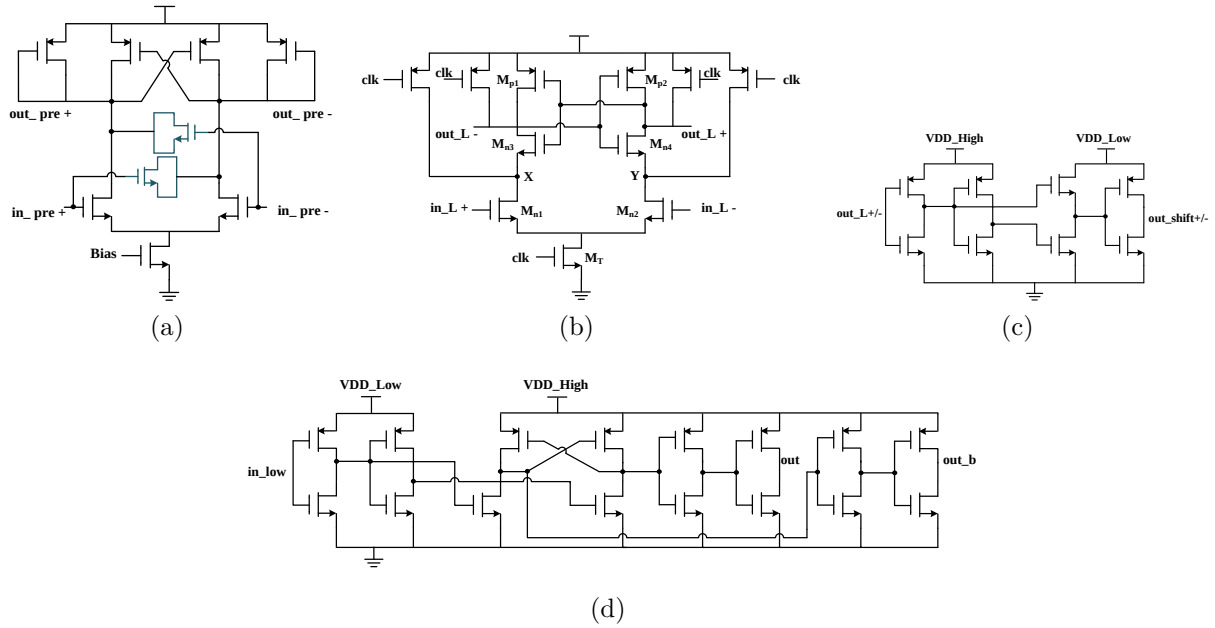



Figure 6.21 Comparator sub-blocks circuit scheme: (a) pre-amplifier, (b) StrongARM latch, (c) level-down shifter, (d) level-up shifter

Since the comparator block output is sent to the digital control logic of the SAR ADC, which is designed at a lower supply voltage, the SR-Latch has been designed with $V_{DD} = 1\ V$. However, pre-amplifier and StrongARM latch work with 1.8 $V$ supply voltage. Therefore, a level-down shifter has been employed between StrongARM and SR-latch.

It is also worth noting that the low-voltage control logic generates the *clk* signal for the comparator. The level-up shifter illustrated in Fig. 6.21(d) is used to change the level of digital logic signals required to control the analog part.

### Comparator Layout Design

The StrongARM latch layout design has the highest impact on the offset which is a nonlinear function of $V_{th}$ mismatch and parasitics [82]. As shown in Fig. 6.21(b), the StrongARM latch consists of a differential pair (DP) of $M_{n1}$ and $M_{n2}$, an NMOS cross-coupled pair (CCP) of $M_{n3}$ and $M_{n4}$, and an PMOS CCP ($M_{p1}$, $M_{p2}$). The mismatch between $X$ and $Y$ nodes impacts the input offset. Three main transistor placing methods, i.e., clustered, common centroid (CC), and interdigitated (ID), are used for DP and CCP structures in the literature. CC and ID usually provide better matching but cause routing and parasitic challenges in modern FinFET technologies. In this work, the CC method is still practical.

The dummy transistors are also placed on two sides of the layout design to avoid the fringe effect.

The layout design of the comparator is presented in Fig. 6.22. The design's orientation is regarding the proposed ADC's final floor-plan.

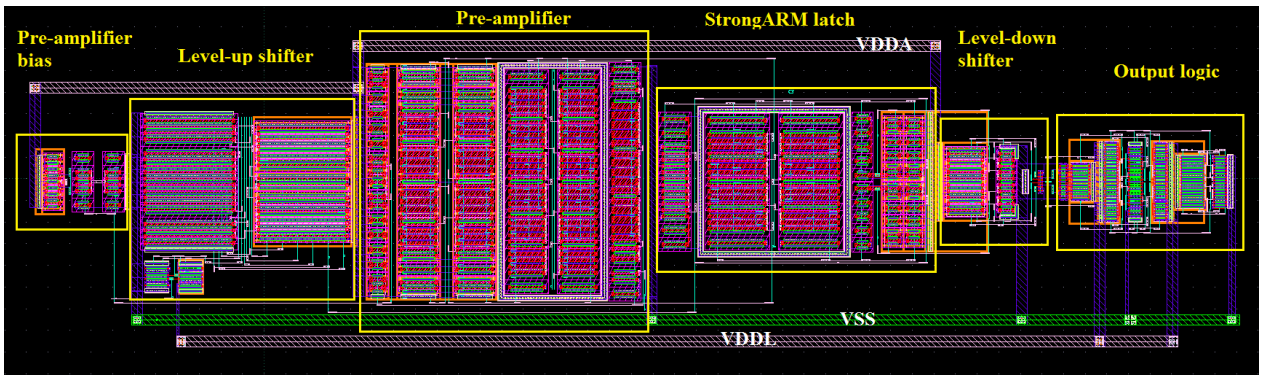



Figure 6.22 Layout design of the comparator

## PVT Consideration

In order to verify the offset performance of the designed comparator, a 500-sample Monte-Carlo simulation considering both mismatch and process variations has been done. Fig. 6.23 shows that the mean value of offset is $-63\ \mu V$, approximately. Since the 2 $mV$ standard deviation of the offset is less than $LSB = \frac{1}{2^6} = 15.625\ mV$ of a 6-bit SAR ADC used in each stage, the comparator offset does not affect the proposed ADC performance.

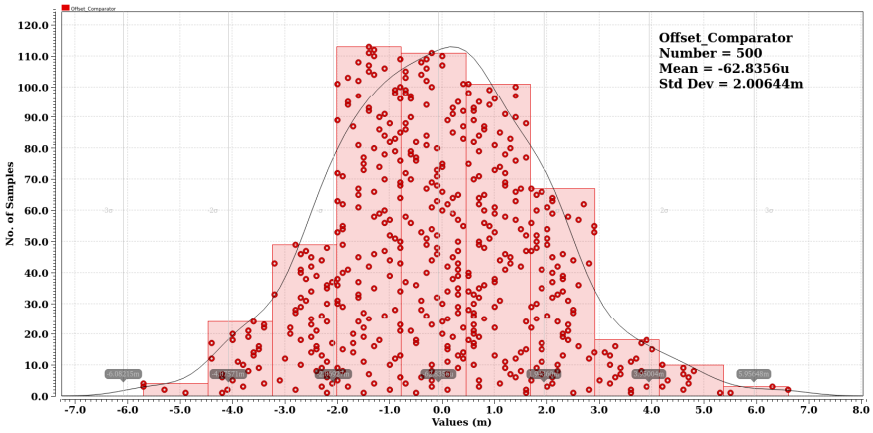



Figure 6.23 Post-layout Monte-Carlo simulation results considering mismatch and process variations for the comparator offset

Fig. 6.24 demonstrates the effect of supply voltage variation on the comparator offset in three different temperatures, i.e., 0, 27, and 70 degrees Celsius. The maximum ±0.3% change in the offset value has a negligible impact on the ADC performance.

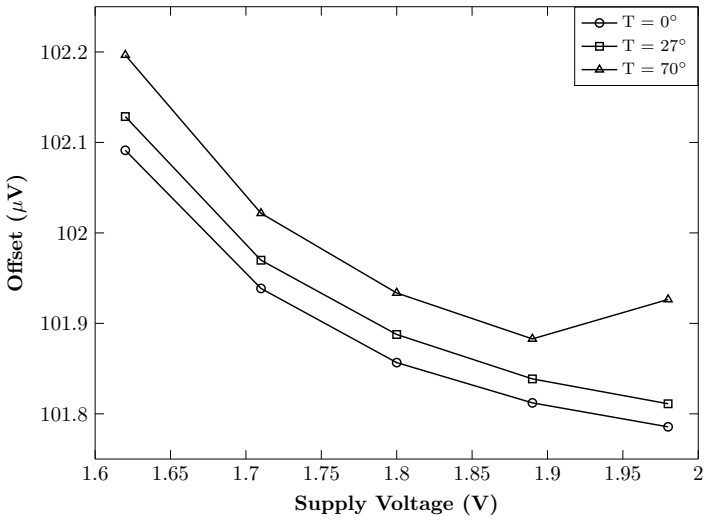



Figure 6.24 Post-layout simulation results considering supply voltage and temperature variations for the comparator offset

### 6.2.3 Digital Control Logic

For the NS-SAR ADCs, control logic units are required to control both SAR ADC, i.e., sampling switches and DAC switching, and FIR filter switching. In order to save power and area, both control units are combined in this work. According to the ADC speed, a control clock generation based on dividers and shift registers is appropriate.

Fig. 6.15 and Fig. 6.25 show the required timing diagram and the digital control logic circuit, respectively.

The $\Phi_{clki}$ signals generated using the circuit illustrated in Fig. 6.25 are utilized to control the SAR output register as depicted in Fig. 6.26. It is worth noting that only $\Phi_{clki};\ i : odd$ are required for controlling the DAC switches of a 6-bit SAR ADC; however, the digital control logic has been designed to be also used for a 9-bit SAR ADC for the sake of future phase of the project.

In order to implement the bottom plate sampling method, four switches are needed, as shown in detail in Fig. 6.27. All switches are implemented using a transmission gate structure with dummy transistors to reduce the charge injection and clock feed-through impacts.

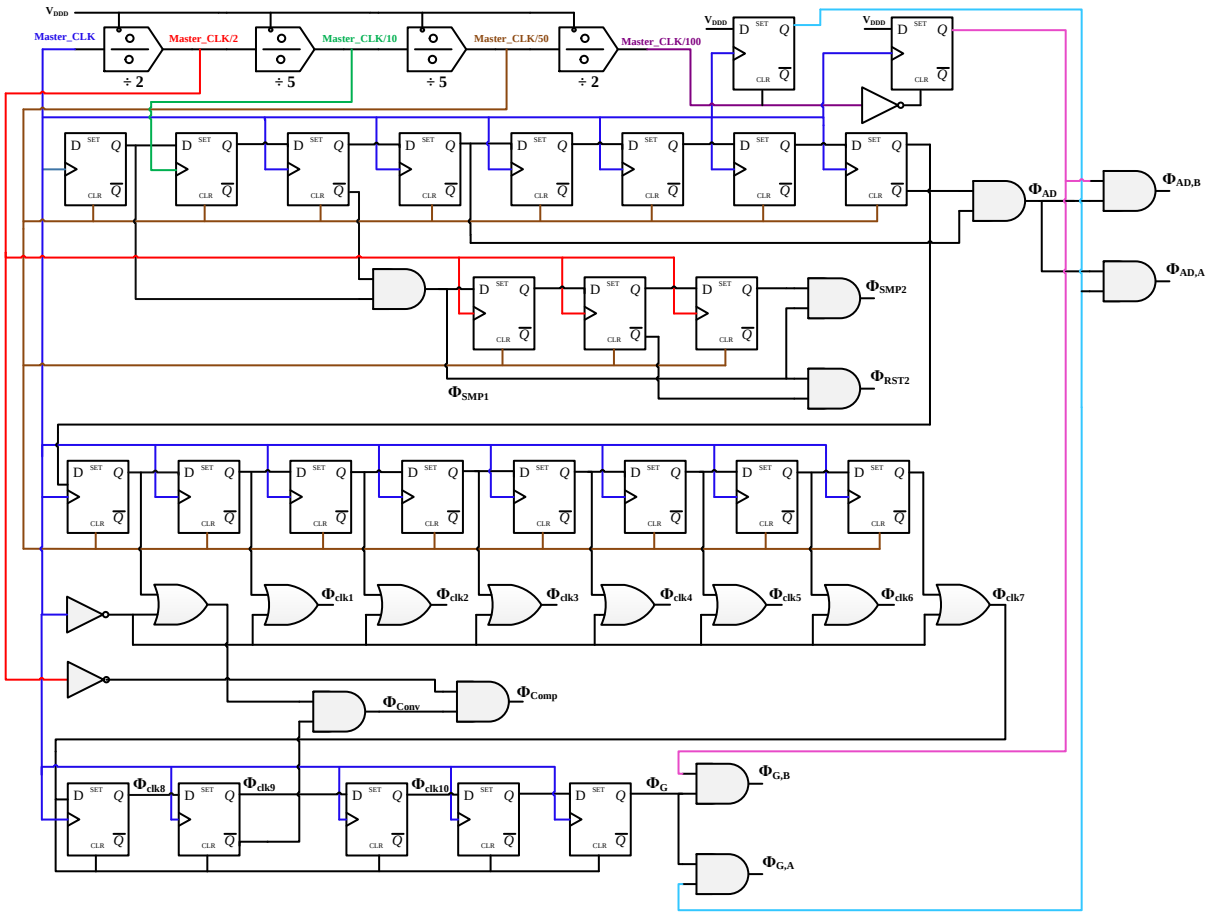



Figure 6.25 Successive approximation register for binary search combined with the logic required to control the NS-SAR ADC used in the proposed MASH 2-2 NS-SAR ADC

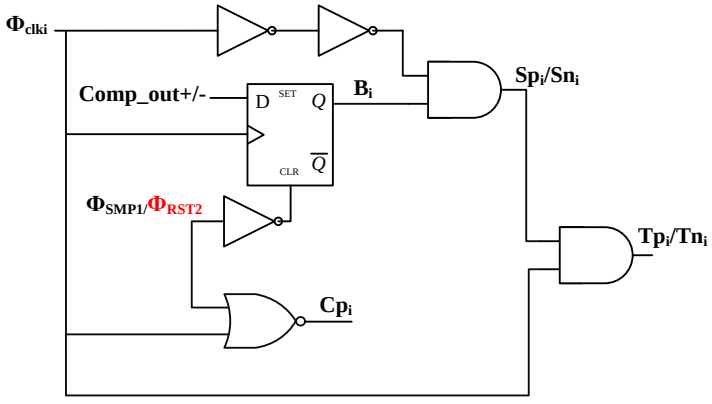



Figure 6.26 Output SAR register for controlling the DAC switches

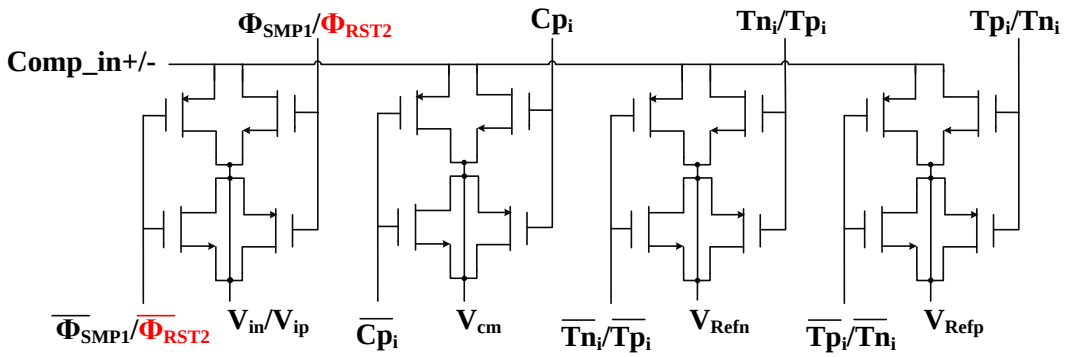



Figure 6.27 Required DAC switches and signals for controlling the DAC in the bottom-plate sampling SAR ADC

### 6.2.4 Op-amp Circuit and Layout Design

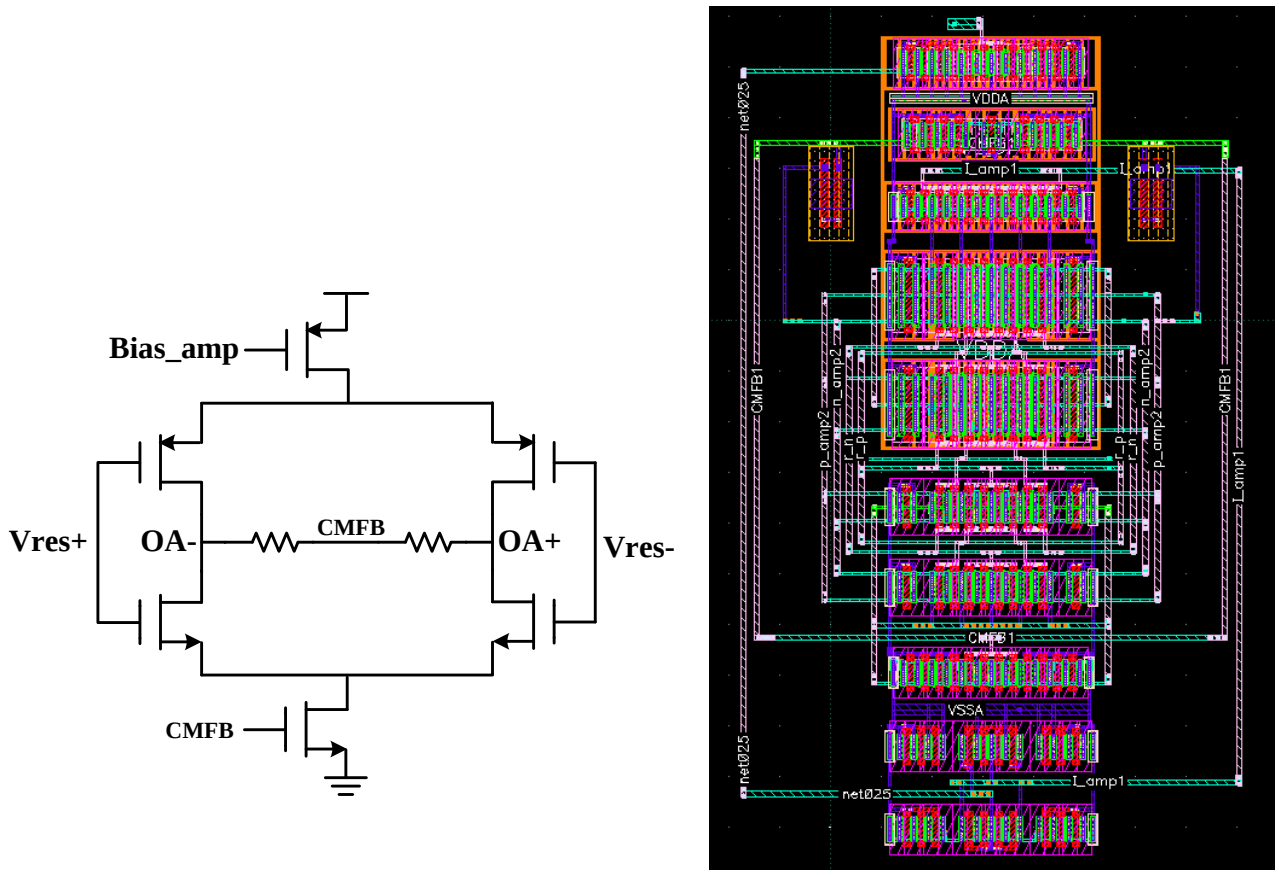
As discussed, an op-amp with a gain of $G = 8$ is required in the feedback path to amplify the residue voltage of SAR ADC. Different types of amplifiers have been used in prior works. Recent works have focused on the PVT sensitivity of dynamic amplifiers. According to the results of modeling the effect of non-idealities using a MATLAB code, the op-amp noise significantly impacts the proposed MASH 2-2 NS-SAR ADC performance. Also, the op-amp gain variation due to the PVT degrades the SNDR of the proposed ADC and its first stage similarly, so it does not significantly affect the SNDR improvement achieved by the MASH structure. Therefore, despite the PVT variations, the main advantage of the proposed ADC is valid.

Consequently, for implementing the proposed ADC, an open-loop static inverter-based amplifier was used as its circuit and layout design shown in Fig. 6.28. Although a static amplifier is sensitive to PVT variations, it has shown better noise performance than dynamic amplifiers. Furthermore, an open-loop structure provides higher bandwidth and does not require a high open-loop gain like closed-loop amplifiers. Table 6.2 presents the specifications of designed op-amp.

Table 6.2 Op-amp specifications

| Specification | Gain | Bandwidth | Input referred noise |
|---|---|---|---|
| Value | 8 $\frac{V}{V}$ | 300 MHz | 50$\mu$ $V_{rms}$ |

Similar to the StrongARM layout design, the common centroid technique has been used for the layout design of both NMOS and PMOS differential pairs of the op-amp (Fig. 6.28).




(a) (b)

Figure 6.28 Static open-loop inverter-based op-amp circuit used in the proposed MASH 2-2 NS-SAR ADC: (a) Circuit design, (b) Layout design

### Non-linear Op-amp Input Capacitance

As discussed in [38], the op-amp input capacitor has been increased to suppress the flicker noise. Therefore, the op-amp non-linear input capacitor size is large enough to change the voltage on DAC capacitors and cause distortion.

However, increasing the DAC capacitor size alleviates this issue. To verify this statement, a simulation has been done with transistor-level blocks for the first stage of the proposed ADC using two different DAC capacitor values. Figure 6.29 demonstrates that increasing the DAC capacitor size removes the distortion (harmonics) caused by the op-amp non-linear input capacitor. This effect is another factor in determining the minimum DAC capacitor size.

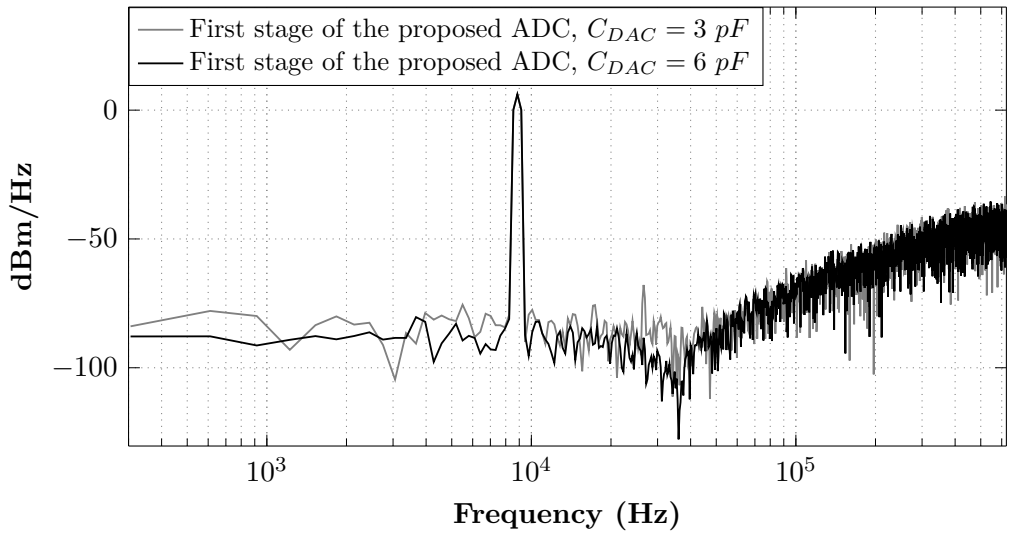



Figure 6.29 Transistor-level simulations in Cadence: 4096 points PSD of the proposed ADC's first-stage output for $f_s = 1.25\ MHz$, $f_{in} = 8.85\ kHz$, $OSR = 10$

### Mismatch and Process Variation Considerations

As discussed, Fig. 6.14 in the first part of this chapter illustrates the impact of op-amp gain variation on the ADC performance. In order to estimate the gain variation of the designed op-amp, a post-layout 1000-sample Monte-Carlo considering both mismatch and process variation has been done, as depicted in Fig. 6.30. It illustrates that the standard deviation is less than 8%, which estimates a 6-dB SNDR reduction for the proposed ADC and its first stage according to Fig. 6.14.

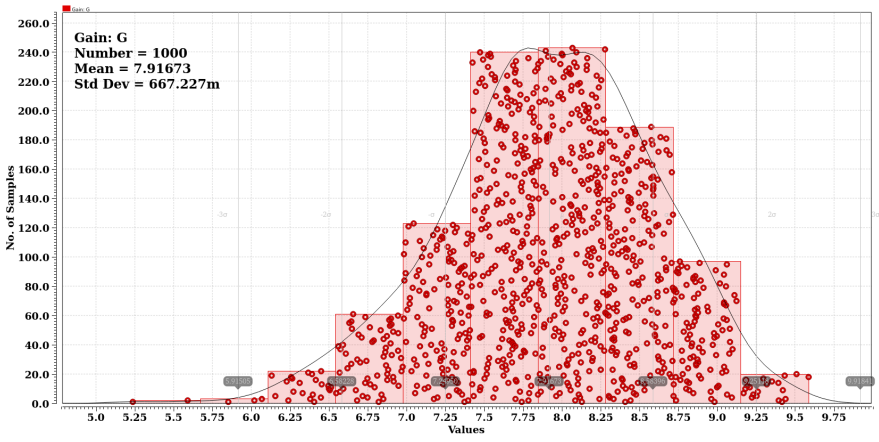



Figure 6.30 Static open-loop inverter-based op-amp circuit used in the proposed MASH 2-2 NS-SAR ADC

### 6.2.5 SC FIR Filter

As mentioned, a ping-pong switching FIR filter is utilized to design the proposed ADC. Fig. 6.31 shows the operation of the ping-pong FIR filter. Three capacitors are at the op-amp output to sample the amplified residue voltage. $C_{F1.1}$ transfer charges to $C_{DAC1}$ one cycle later; however, $C_{F2.1}$ and $C_{F3.1}$ perform this operation alternatively two cycles later. A simpler switching logic is required for the ping-pong switching since there is only a single charge-sharing step in each conversion cycle [40]. The MOM capacitor has been used for implementing the unit capacitor of the FIR filter with a size of 500 $fF$. The employed switches are also transmission gates with dummies.

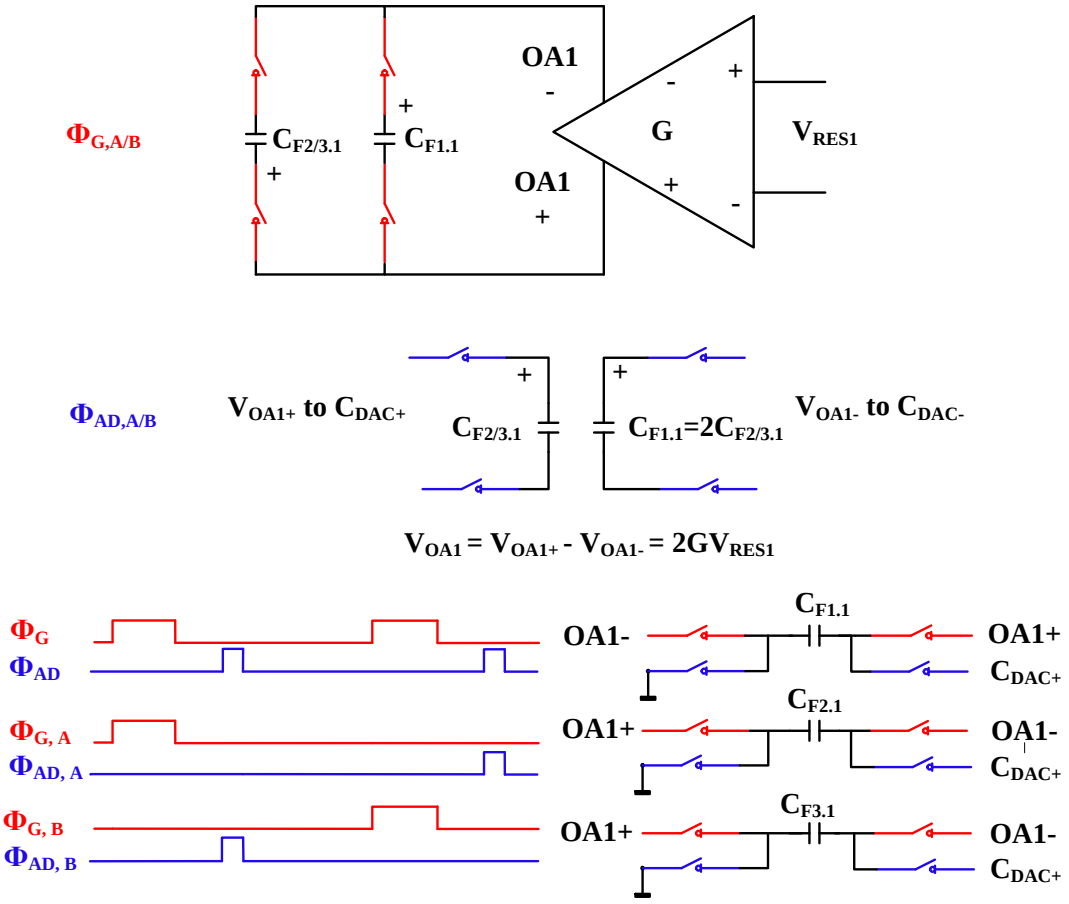



Figure 6.31 FIR filter: ping-pong switching operation and timing [40]

### 6.2.6 Inter-stage Block

As discussed earlier, one of the advantages of the proposed MASH NS-SAR ADC compared to conventional MASH structure is less complexity and no need for extra hardware for extracting the residue voltage of the first stage. However, a sample-and-hold is required to connect the ADC's two stages for feeding the residue to the second stage. A pipeline NS-SAR presented in [87] uses an OTA-based integrator in the first stage and a fully-passive integrator in the second stage. It reuses the OTA-based integrator as the inter-stage block. However, the OTA requires wide-bandwidth, high DC gain, and wide output swing.

In order to avoid challenges related to designing an OTA-based sample and hold, capacitor charge sharing is used in our work. For this purpose, the feedback path of the first stage is shared to implement the inter-stage block as shown in Fig. 6.32. A capacitor, $C_{IG} = 3\cdot C_{F2/3.1}$, in parallel with FIR filter capacitors, samples the amplified residue voltage. Before charge sharing phase, i.e., $\Phi_{AD}$, the DAC2 capacitor is reset ($\Phi_{RST2}$) and then, in $\Phi_{SMP2}$, $C_{IG}$ transfers its charge to $C_{DAC2}$. According to the chosen ratio for capacitor values, the transferred voltage to the second stage is as follows:

$$V_{SMP2} = \frac{C_{GI}}{C_{GI} + C_{DAC2}} \cdot 2 \cdot \ V_{RES1} = 3 \cdot V_{RES1} \tag{6.10}$$

Transferring $3 \cdot \ V_{RES}$ instead of $V_{RES}$ avoids SNDR reduction due to op-amp gain variation or leakage in charge sharing operation.

## 6.3 ADC Integration

This section provides the layout considerations for integrating the ADC sub-block component. The chip prototype designed for the fabrication and along with the post-layout simulation results are also discussed to verify the feasibility of the proposed MASH 2-2 NS-SAR ADC.

### 6.3.1 Core Design

Fig. 6.33 depicts the layout design of the core of the proposed ADC. It has been designed for fabrication in ST28-nm FD-SOI technology. The two stages and their sub-components, along with the inter-stage block and digital control logic, are mentioned in the figure. Using similar second-order NS-SAR designs in two stages of the ADC simplifies the layout integration process. As discussed earlier, layout asymmetry impacts the performance of analog designs. Therefore, all the analog components are placed symmetrically, considering a horizontal line. The overall design is also symmetrical to some extent considering a vertical line.

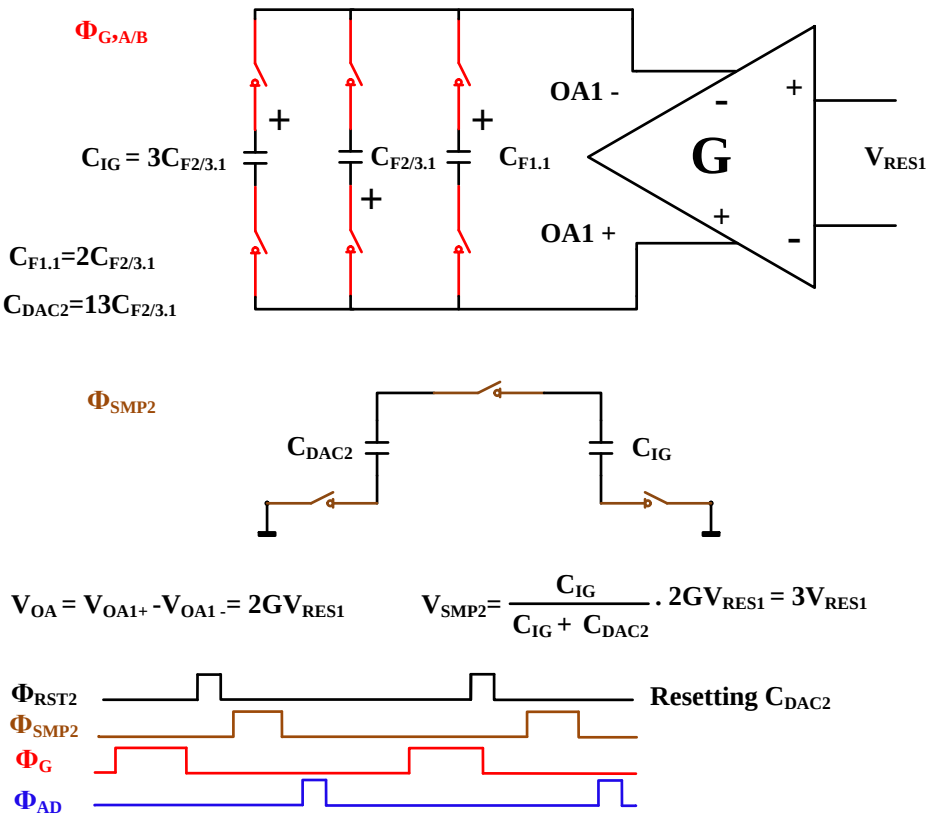



Figure 6.32 First-stage feedback path hardware sharing to transfer the residue voltage to the second stage of the proposed ADC

The overall dimension of the core design is 860$\mu m$ by 360$\mu m$; however, the total area without considering the empty area is 0.23 $mm^2$. Since the standard logic cells with very compact layouts are used to design the digital circuit, it has a small area compared to the analog part. However, DAC capacitors occupy the majority of chip area. Fig. 6.34 illustrates the breakdown of area.

### 6.3.2 Chip Design

Creating an IO ring and padring surrounding the core is required to connect the core design to the outside world for wire-bonded circuits. Fig. 6.35 depicts the simplified schematic view of the IO ring with the core design block inside it. The analog section of the IO ring consists of signal and supply IOs. In the analog section, four different supply IOs are separated by power cut fillers in the layout (not shown in Fig. 6.35). The $V_{DDAE}$ provides the supply voltage required for the IO cells. However, $V_{DDA}$, $V_{DDL}$ and $V_{Refp}$ are needed to supply the high-level (1.8 V), low-level (1 V) analog components and as the DAC reference voltage

(1.8 V), respectively. The digital section includes three supply IOs for driving digital IO cells ($V_{DDDE}$), the digital core ($V_{DDD}$), and controlling the signal IOs input/output state ($V_{DDDC}$). The ST28-nm FD-SOI provides special fillers and layers to isolate the digital IO ring section from the analog one.

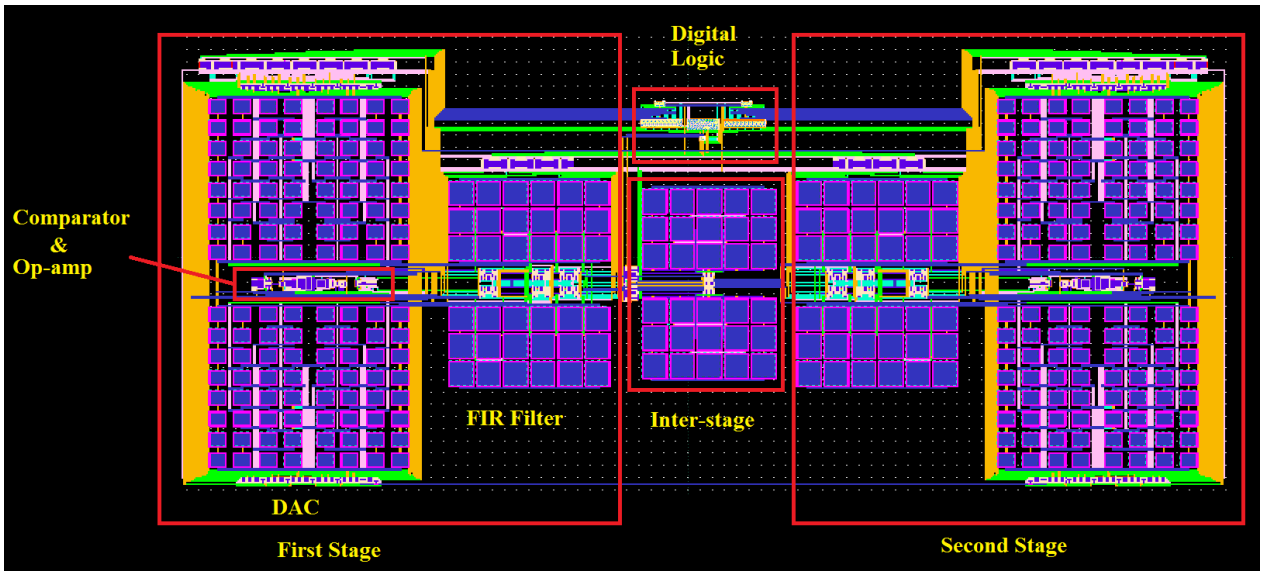



Figure 6.33 Layout design of the proposed MASH 2-2 NS-SAR ADC

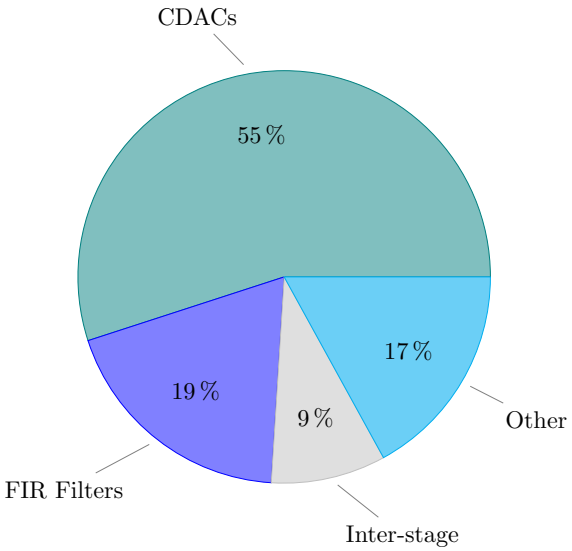



Figure 6.34 Breakdown of area for the proposed MASH 2-2 NS-SAR ADC

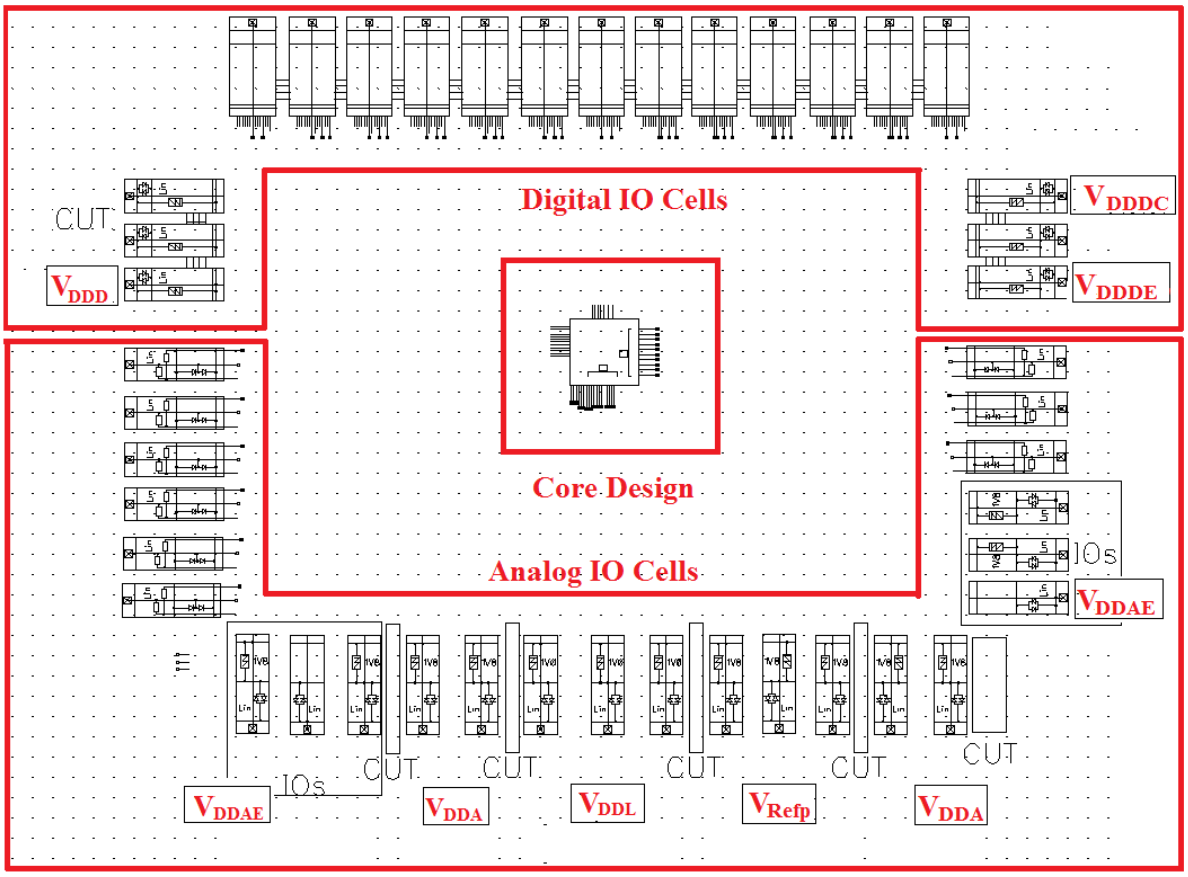



Figure 6.35 The top-view of the chip IO ring design for the proposed MASH 2-2 NS-SAR ADC

Fig. 6.36 illustrates the complete chip design of the proposed MASH 2-2 NS-SAR ADC. The padring has been constructed using the pad design provided by the technology. The empty space inside the IO ring and around the core design is filled by decoupling capacitors with size of 15-20 pF connected between supply voltage nodes and ground. The complete chip dimension considering the IO ring and padring is 1.2 mm by 1 mm.

### 6.3.3 Post-layout Simulation Results

The post-layout simulation using the parasitic extracted model of the designed chip with 7.08 kHz full-scale input signal (1.8-Vp), over a 100 kHz bandwidth obtains a peak SNDR of 75 dB and 66 dB for the proposed ADC and its first stage, respectively. As shown in Fig. 6.37, a fourth-order noise-shaping with an 80 dB per decade slope is evident in the output spectrum of the MASH architecture. The output spectrum of the first stage also obtains a second-order

noise-shaping with a 40 dB per decade slope. It confirms that the MASH structure effectively achieves a 9-dB SNDR improvement and increases the noise-shaping order compared to the first-stage output.

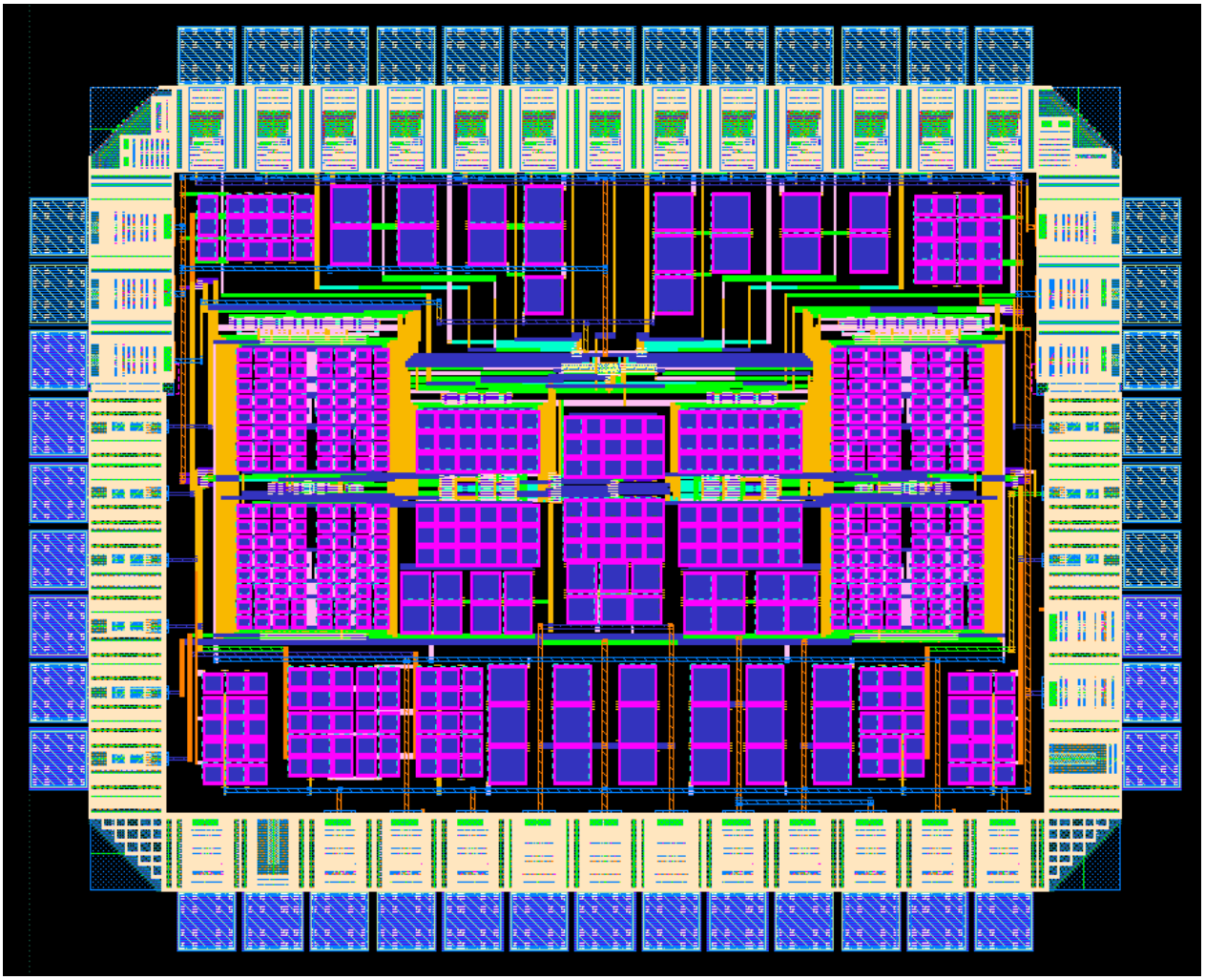


Figure 6.36 The complete chip layout design of the proposed MASH 2-2 NS-SAR ADC

Fig. 6.38 illustrates a breakdown of the power consumption resulting from the post-layout simulation. The ADC consumes 498 $\mu$W at 2 MS/s. It is worth noting that some sub-blocks, such as comparators and digital parts, are overdesigned to be suitable for a 9-bit SAR ADC, resulting in an extra number of level-up shifters. Furthermore, as discussed earlier, the second-stage op-amp requires more relaxed noise performance, which can be achieved by implementing a very low-power structure. However, similar components are used in both stages to accelerate and simplify the proposed ADC implementation.

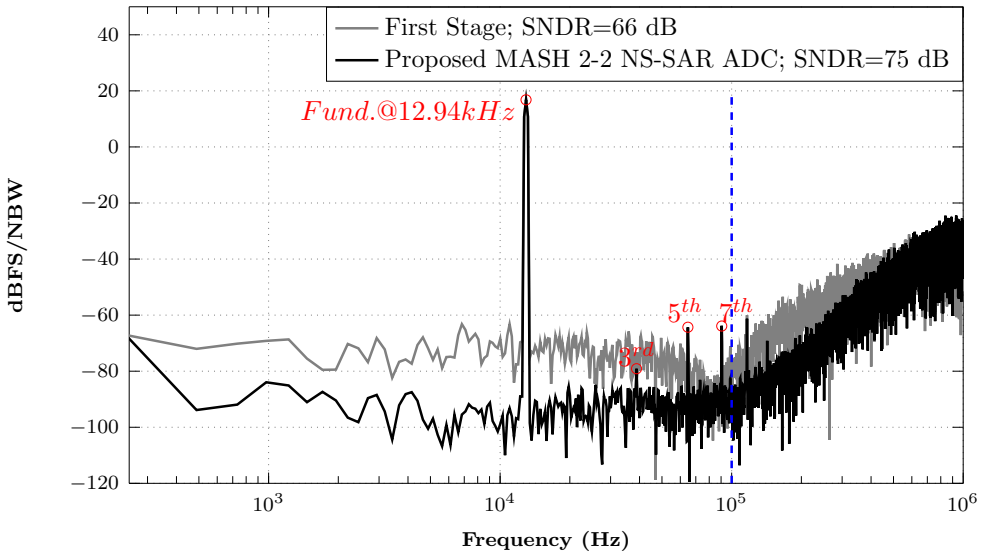



Figure 6.37 Post-layout simulation result: 8192-point power spectral density of the proposed MASH 2-2 NS-SAR ADC and its first-stage output

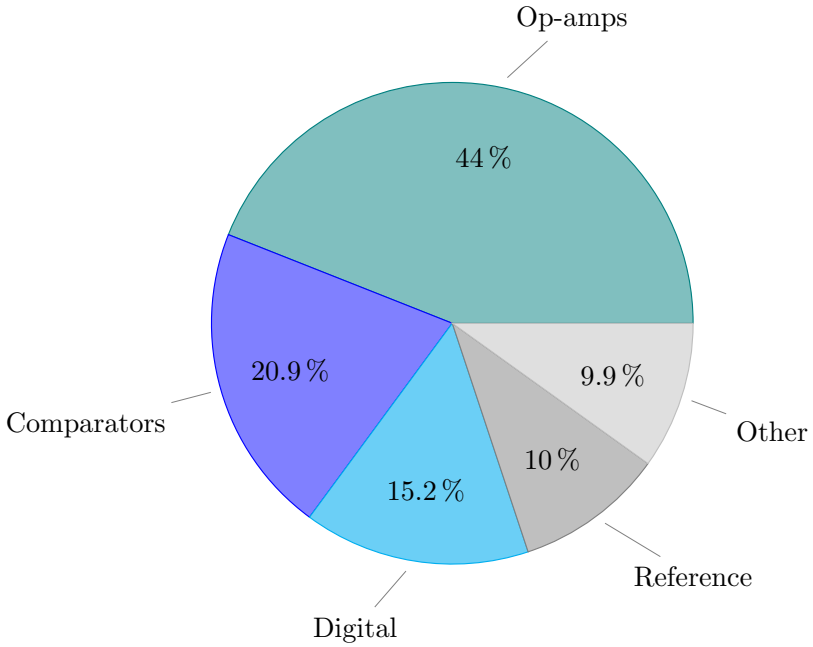



Figure 6.38 Breakdown of power consumption for the proposed MASH 2-2 NS-SAR ADC

Finally, Table 6.3 compares this work with some other state-of-the-art sub-MHz ADCs. It is worth noting that other works have been silicon verified, but our work results are based on the post-layout simulations. The proposed ADC exhibits the highest noise-shaping order reported in the literature. It does not use any calibration method, while other works in the table have used at least the DAC mismatch calibration to achieve higher resolutions. Considering the SNDR and FoMs results without using calibration methods, the proposed ADC achieves values comparable with the recent prior works, despite the higher power consumption due to overdesigned sub-blocks.

Table 6.3 Comparison table

| Specifications | JSSC 2022 [65] | JSSC 2022 [67] | JSSC 2021 [43] | ISSCC 2021 [42] | TVLSI 2021 [88] | JSSC 2020 [41] | JSSC 2020 [40] | JSSC 2019 [37] | JSSC 2018 [39] | This $work^{+}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| Architecture | EF-CIFF | CIFF | EF-CIFF | CIFF | CIFF | CIFF | EF | CIFF | EF | MASH-EF |
| Loop Filter Type | Static Amp. | Fully passive | Open loop FIDA | Cap. Stack. Dynamic Buff. | Fully passive | Closed loop Dynamic Amp. | Static Amp. | Fully passive | Dynamic Amp. | Static Amp. |
| Comparator input-pair | 2 | 2 | 1 | 2 | 2 | 3 | 1 | 3 | 1 | 1 |
| Process (nm) | 130 | 40 | 65 | 40 | 130 | 40 | 28 | 40 | 40 | 28 FD-SOI |
| Supply (V) | 1.2 | 1.1 | 1.1 | 1.1 | 1.2 | 1.1 | 1.2 | 1.1 | 1.1 | Dual 1.8 & 1 |
| $F_s$ (Ms/s) | 2 | 2 | 10 | 5 | 2 | 10 | 2 | 8.4 | 10 | 2 |
| OSR | 8 | 25 | 8 | 10 | 8 | 8 | 10 | 16 | 8 | 10 |
| Bandwidth (MHz) | 0.125 | 0.04 | 0.625 | 0.25 | 0.125 | 0.625 | 0.1 | 0.262 | 0.625 | 0.1 |
| Power ($\mu$W) | 96 | 67.4 | 119 | 340 | 59.9 | 107 | 120 | 252.9 | 59.9 | 498 |
| Calibration | LMS+AF | $2^{nd}$-order MES | Miamatch +SNC | Mismatch | DWA +PRN | Mismatch | Mismatch | Mismatch | Mismatch +PRN | No |
| SNDR (dB) w. calibration | 79.57 | 90.5 | 84.8 | 93.3 | 78.69 | 83.8 | 87.6 | 78.4 | 79 | - |
| SNDR (dB) w.o. calibration | 67.16 | 76.4 | 78.1** | n.a | 71.38 | n.a | n.a | 74 | n.a | 75 |
| SFDR (dB) | 94.75 | 102.2 | 103 | 104.4 | 92.9 | 94.3 | 102.8 | 78.4 | 89 | 80.5 |
| NS order | 3 | 1 | 3 | 4 | 2 | 2 | 4 | 2 | 2 | 4 |
| DAC resolution (bit) | 8+2 Redun. | 11+2 Redun. | 10+1 Redun. | 9 | 9 | 10+1 Redun. | 8 | 9+1 Redun. | 9 | 6 Each stage |
| DAC/Other capacitor size (pf) | 2.18/14.11* | 9/27* | 1.17/7.06 | 16/20 | 4.13/2.97 | 4/21.5* | 15.36/2.84 | 8.45/19.55* | 4/0.9 | 26/5.5* |
| Area ($mm^2$) | 0.165 | 0.061 | 0.04 | 0.094 | n.a | 0.037 | 0.02 | 0.04 | 0.024 | 0.23 |
| $FoM_s^{\dagger}$ (dB) w. calibration | 170.7 | 178.2 | 182 | 182 | 171.9 | 181.5 | 176.8 | 171 | 178 | - |
| $FoM_s$ (dB) w.o. calibration | 158.3 | 164.1 | 175.3** | n.a | 164.6 | n.a | n.a | 166.6 | n.a | 158 |

$^{+}$ Post-layout Simulation Results
$^{*}$ MOM Capacitor
$^{**}$ with DAC Mismatch Calibration
$^{\dagger} FoM_s = SNDR + 10 \cdot log(\frac{Bandwidth}{Power})$

Architecturally, the proposed structure comprises lower DAC resolution and single-input pair comparators. This table also compares the DAC and total capacitor size for different structures. The larger DAC capacitor for our structure is mainly because of using two SAR ADCs. As mentioned earlier, we increased the DAC capacitor size to mitigate the effects of switches charge leakage and op-amps input non-linear capacitance. A smaller capacitor value is required by employing a linearization technique. However, the total size of other capacitors is significantly smaller or comparable with most high-performance NS-SAR ADCs. The larger area of the proposed ADC is mainly related to the DAC layout design. As discussed, only MOM capacitors are available in ST28nm FD-SOI technology. MOM capacitors provide a smaller minimum size than the MIM type (for example, 2.5 fF and 9.5 fF in TSMC 65nm). However, the MIM one has a smaller area for the same capacitor size. Compared to the works using MOM type with approximately similar total capacitor size, the proposed ADC still has the larger area. The first reason is the larger unit capacitor, hence more giant dummies in our structure. The second reason is using large IO transistors to design the sub-blocks. Therefore, using a DAC floorplan leveraging a smaller unit capacitor size and implementing sub-block components utilizing standard transistors could decrease the area considerably.

## 6.4 Summary of Prototype Design and Results

The implementation of the proposed MASH 2-2 NS-SAR ADC, in CHAPTER 3, was discussed. A MATLAB code modeling is presented to predict the performance of the ADC in the presence of main non-ideality effects. The circuit-level and layout design considerations of sub-blocks have been discussed, along with the Monte-Carlo simulation results for the critical blocks. The circuit is implemented in ST-28nm FD-SOI technology. The post-layout simulation results prove the ability of the MASH structure to increase the NS order of the conventional NS-SAR ADCs without adding significant complexity and power consumption. Based on the post-layout simulations, the proposed ADC achieves an SNDR and SFDR of 75 dB and 80.5 dB, respectively. The circuit consumes 498 $\mu W$ using a dual supply voltage of 1.8 V and 1 V. The proposed ADC obtains the highest reported NS order with higher power consumption due to overdesigning the sub-blocks for the future work. Therefore, power-optimized designs and DAC mismatch calibration are required to exhibit a cutting-edge performance compared to the state-of-the-art.

# CHAPTER 7 GENERAL DISCUSSION

Analog to digital conversion is a key part of many electronic systems. As they are critical components, they have been the subject of numerous contributions, and several fundamental ADC architectures have been proposed. In addition to the fundamental architectures, many hybrid architectures combining features of the fundamental architectures have been proposed. Despite the numerous previous contributions, new options are discovered, and exploring them can lead to breakthroughs.

This led us to propose two architectures based on noise-shaping SAR ADCs. The first structure, i.e., MASH 2-2 NS-SAR ADC, has been implemented in ST-28nm FD-SOI technology. However, the macro-model of the second architecture, a two-step MASH NS-SAR incremental ADC, is designed in Cadence Spectre®. An analysis is also presented to investigate the power consumption of this structure. The proposed analysis can be used to estimate the power-bound of conventional NS-SAR ADCs.

As mentioned in CHAPTER 2, noise-shaping SAR ADCs have provided better power efficiency than $\Delta\Sigma$ modulators by using SAR ADCs as the multi-bit quantizers. However, the noise-shaping order is limited by the charge leakage in passive filters. Using buffers to mitigate this problem degrades the power efficiency. On the other hand, amplifier-based NS-SAR ADCs suffer from op-amp noise, limiting the achieved resolution. Furthermore, employing multi-input comparators, capacitor stacking techniques in fully-passive structures, and hybrid EF-CIFF combined with noise cancellation techniques in amplifier-based NS-SAR ADCs make their structure complex. Therefore, a MASH structure is proposed in CHAPTER 3 to increase the NS order to fourth-order using components with requirements for designing a second-order NS-SAR ADC. Since this chapter discusses the system-level and macro-model of the proposed structure, we compared it with the prior works architecturally. It is less complex than the conventional $\Delta\Sigma$M-based MASH ADCs since the residue voltage is extracted from analog nodes of SAR ADC's CDAC. Also, only one extra capacitor at the output of the first-stage op-amp samples the residue voltage simultaneously with the FIR capacitors. So, it does not add extra time to ADC's operation. As discussed in CHAPTER 6, modeling the non-idealities in MATLAB shows that the noise of the first-stage op-amp is the design bottleneck, and the second-stage op-amp can be designed with much less noise and power requirements. Therefore, increasing the NS order is possible without a significant complexity and power penalty.

While implementing the proposed ADC, comparator kick-back noise, op-amp input capacitor, and FIR filter switches charge injection limited the ADC's performance. Therefore, a pre-amplifier with input dummy transistors, larger CADC capacitors size, and larger FIR capacitors values are utilized to address those issues. Another limiting factor is the non-linearity of the DAC due to the design parasitics and wire connections. The MATLAB code in CHAPTER 6 shows that a data weighted averaging (DWA) calibration method effectively alleviates this problem. However, since the number of IO pins for an academic chip is limited, implementing this technique requires designing a serial-to-parallel-interface (SPI) for realizing the algorithm at the circuit level, which is not covered by this thesis.

This proposed ADC comprises two supply voltages of 1.8 V and 1 V and an OSR of 10 at a bandwidth of 100 kHz. The ADC's first and second stages achieve a second and fourth-order noise-shaping performance, respectively. The post-layout simulation results show a 498 $\mu$W power consumption. However, it should be considered that the comparator, logic circuits, and level-up shifters are designed for a higher speed 9-bit SAR ADC, which is required for future work. Also, the op-amps in the two stages are similar for layout simplicity, while the second-stage one can be designed with negligible power consumption. The fabrication of the designed prototype is under process at the factory; however, delays are experienced due to the high demand for silicon products and industry financial considerations. Since the fabricated chip will be delivered after completing this thesis, we relied on the post-layout simulation results to validate the proposed architectures and solutions. Based on the experience that exists in our group, the post-layout simulation provides results close to the experimental one. The post-layout simulation results combining the system-level analysis prove that the proposed ADC achieves a fourth-order NS performance, the highest reported order in the literature. Also, considering the effect of DAC mismatch calibration and implementation of the power-optimized components, the proposed ADC achieves a higher figure of merits comparable with the state-of-the-art NS-SAR ADCs. Furthermore, the Monte-Carlo simulation results for the comparator and op-amp show that only the op-amp gain might be degraded after fabrication. However, it can be mitigated by tuning the op-amp bias or by employing a calibration method.

Also, in CHAPTER 2, we discussed the conventional and hybrid $\Delta\Sigma$-based incremental ADCs. Hybrid hardware sharing multi-step IADCs improve power and area efficiency. However, extended counting structures are complex, and their linearity is limited to the Nyquist rate ADC performance. All discussed types of IADCs suffer from the high-power consumption of the OTAs and comparators used in multi-bit quantizers. The achieved bandwidth is also limited due to the high required OSR values. The second proposed ADC combines the advantages of the hardware sharing two-step structures with the first proposed architecture

to mitigate the IADCs mentioned issues. The macro-model simulations achieve a sixth-order NS performance. It comprises power-efficient low-resolution multi-bit SAR ADCs instead of flash-based quantizers. Using the simple low-gain op-amps in the EF structure removes the need for power-hungry OTA-based integrators in CIFF $\Delta\Sigma$-based IADCs. Benefiting from high-order NS and SAR quantizers decreases the required OSR value, resulting in a wider bandwidth. The proposed IADC is not implemented at the transistor level. However, the performance of the $\Delta\Sigma$ mode corresponds directly to that of the incremental mode. Most notably, any distortion in the $\Delta\Sigma$ translates directly into the incremental mode. Also, the proposed MASH 2-2 NS-SAR ADC is operated in incremental mode as the first-step structure of the proposed IADC. Therefore, the non-idealities discussed in CHAPTER 6 impact the performance of both proposed ADCs similarly. Consequently, the design requirements of the IADC first stage can become dynamically relaxed in the second-step operation to save power. The body-biasing feature provided by the ST-28nm FD-SOI is essential for achieving this goal.

Not only does the power-bound analysis presented in CHAPTER 5 estimate the performance of the proposed IADC, but it also addresses the lack of an analytic study of the conventional NS-SAR ADCs. It was confirmed by comparing the experimental results of prior NS-SAR ADCs with the achieved analytical results. Furthermore, a method is employed to tune the decimation filter to reduce the effects of the circuit imperfections on the ADC SNDR. It is worth noting that a power-bound represents the minimum power consumption required to achieve a specific resolution and speed, considering the dominant imperfection effects. This bound may not be easily achievable and it is not the exact value reached by a practical implementation for the specified power consumption. The proposed bound is generally valid for different structures and sub-blocks. For example, the general rule for calculating the power consumption of the op-amp, independent of the architecture and being static or dynamic, is to have its settling error less than the LSB/2 of the ADC. Also, assuming MIM capacitors properties and equations in our analysis provides the worst-case process-limited power-bound since the minimum available MOM capacitor size is smaller than that of the MIM capacitor in each technology. For instance, in TSMC 65nm, the minimum MOM and MIM capacitor values are 2.5 fF and 9.5 fF, respectively. On the other hand, the power bound limited by DAC capacitor mismatch is 2-4 times higher assuming MOM capacitors since it has a larger mismatch parameter ($K_Q$) and smaller density ($K_c$). For example, in TSMC 65nm, the parameters are $K_Q = 1.5\%$ and $K_c = 1.5 - 2.8\ fF/\mu m^2$ for MOM capacitors, while these values are $K_Q = 0.5\%$ and $K_c = 1.6 - 5\ fF/\mu m^2$ for MIM capacitors. Therefore, assuming typical MOM capacitor properties in our proposed analysis negligibly affects the resulting power-bound at low resolutions.

# CHAPTER 8 CONCLUSION AND RECOMMENDATIONS

Analog to digital converters are inherently complicated architectures that require particular considerations in designing their sub-blocks. The circuit imperfections of each component can degrade the overall ADC specifications such as resolution, power, and speed; therefore, it is necessary to predict and identify their respective impacts. Hence, a top-down design process has been used in this thesis. This strategy also helps the designer to use the primary level models to debug the timing errors. Furthermore, it determines the required specifications for components according to their non-ideality effects on the final result to avoid repeating the design process or overdesigning. Another fundamental approach is to know the layout constraints in the used CMOS technology to achieve the best performance for the system, especially after integrating the sub-blocks. In addition to these considerations, calibration techniques are still required to achieve the optimized performance of the ADC. However, using more accurate models when designing sub-blocks relaxes the complexity of the calibration techniques.

The rest of this chapter summarizes this thesis's main achievements, contributions, and related publications. Some approaches are also suggested for future work to implement the proposed ADCs or a high-performance single-stage NS-SAR ADC.

## 8.1 Summary of Works and Contributions

The main contribution of this research is to seek architectural solutions to tackle the limitations of $\Delta\Sigma$-based IADCs and NS-SAR ADCs. Therefore, two hybrid architectures based on conventional NS-SAR ADCs are proposed. The first one is implemented in the ST-28nm FD-SOI CMOS process, and post-layout simulation results are presented to verify its performance. The macro-model simulation results and power-bound analysis are presented to estimate the performance of the second proposed structure. The contributions are detailed as follows:

1. Implementing a MASH 2-2 NS-SAR ADC in ST-28nm FD-SOI CMOS process for a 100 kHz signal bandwidth with dual supply voltages of 1.8 V and 1 V. A MASH structure comprising two similar second-order NS-SAR ADCs is implemented. A fourth-order noise shaping performance is obtained using the FIR filter required for a second-order NS-SAR ADC, with no need for power-hungry OTAs. The second stage can be designed with more relaxed specifications and power consumption. The proposed ADC comprises

lower resolution SAR quantizers and less complex architecture than prior works.

2. In the proposed ADC, cascading NS-SAR ADCs addresses concerns about inaccuracies caused by extra hardware compared with conventional MASH $\Delta\Sigma$ solutions since the analog error signal of the first stage exits on the SAR DAC at the end of each conversion.

3. The op-amp in the first stage of the proposed ADC is used simultaneously to amplify the residue and sample it on hold capacitors to be transferred to the second stage. It reduces the complexity and extra hardware required for the MASH structure and saves the power.

4. Using the first proposed ADC in a two-step incremental mode to improve the resolution makes it suitable for multi-channel applications. Compared to prior IADCs, the proposed sixth-order multi-step architecture does not suffer from the high-power consumption caused by OTAs and multi-bit flash-based quantizers. This ADC also benefits from the advantages of the first proposed ADC. Therefore, wider bandwidth is achievable because of the lower required OSR.

5. An analytic process is proposed to calculate the power-bound of the second proposed ADC. This analysis considers the effect of thermal noise, capacitor mismatch, and minimum feature size of CMOS technology. The presented equations predict better performance for the proposed NS-SAR IADC compared to a conventional $\Delta\Sigma$-based IADC with similar specifications.

6. The proposed analytic method estimates the power consumption of conventional amplifier-based NS-SAR ADCs, either $\Delta\Sigma$ or incremental mode with multi-stage and multi-step topologies, designed in various CMOS technologies.

## 8.2 Recommandation for Future Research

Future work can focus on the proposed ADCs to complete their implementation and improve their performance. As mentioned, the main sub-blocks are overdesigned. Another approach for future research is to propose a high-performance single-stage NS-SAR ADC.

1. The fabrication process of the first proposed ADC, i.e., MASH 2-2 NS-SAR ADC, has not been completed. It can be tested after the fabrication to access the measurement results and to perform a fairer comparison with the prior works. Also, the experience gained while developing the prototype will be used in future designs.

2. The second proposed ADC, i.e., two-step MASH NS-SAR IADC, is not entirely implemented and silicon verified. The sub-blocks designed for the first proposed ADC and body-biasing feature of ST-28nm FD-SOI technology can be used in this regard.

3. MASH structures are sensitive to the mismatch between analog loop-filter and digital cancellation logic. Implementing the proposed MASH 2-2 NS-SAR ADC through the SMASH architecture can achieve improved results without requiring a tuned DCL.

4. The utilized op-amp is an inverter-based structure. However, using a floating-inverter amplifier (FIA) can offer lower input-referred noise.

5. Using time-domain methods in designing the feedback path is beneficial in decreasing the required power supply and PVT sensitivity for the proposed architectures or a single-stage NS-SAR ADC.

6. A calibration method to mitigate the DAC mismatch impact and tune the DCL/decimation filter is required to optimize the proposed ADCs' performance.

7. Employing other types of SAR ADCs with better DAC performance is an excellent practice to obtain better results for the proposed NS-SAR ADCs or a single-stage one.

## 8.3 Publications

- Akbari, Masoume, and Mohamad Sawan. "Analog-to-digital conversion device comprising two cascaded noise-shaping successive approximation register analog-to-digital conversion stages, and related electronic sensor." U.S. Patent No. 11,152,950. 19 Oct. 2021.

- M. Akbari, M. Honarparvar, Y. Savaria and M. Sawan, "Power Bound Analysis of a Two-Step MASH Incremental ADC Based on Noise-Shaping SAR ADCs," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 68, no. 8, pp. 3133-3146, Aug. 2021, doi: 10.1109/TCSI.2021.3077366.

- M. Akbari, M. Honarparvar, Y. Savaria and M. Sawan, "OTA-Free MASH 2–2 Noise Shaping SAR ADC: System and Design Considerations," 2020 IEEE International Symposium on Circuits and Systems (ISCAS), 2020, pp. 1-5,

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- M. Akbari, M. Honarparvar, Y. Savaria and M. Sawan, "OTA-Free MASH Two-Step Incremental ADC based on Noise Shaping SAR ADCs," 2020 18th IEEE International New Circuits and Systems Conference (NEWCAS), 2020, pp. 138-141, doi: 10.1109/NEWCAS49341.2020.9159802.

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# APPENDIX A ARTICLE 4 : ANALOG-TO-DIGITAL CONVERSION DEVICE COMPRISING TWO CASCADED NOISE-SHAPING SUCCESSIVE APPROXIMATION REGISTER ANALOG-TO-DIGITAL CONVERSION STAGES, AND RELATED ELECTRONIC SENSOR

This appendix consists of the granted US patent which proposes the linear model of the proposed MASH NS-SAR ADC. It is worth noting that the macro-model and circuit implementation of this architecture are discussed in CHAPTER 3 and CHAPTER 6, respectively.

- Akbari, Masoume, and Mohamad Sawan. "Analog-to-digital conversion device comprising two cascaded noise-shaping successive approximation register analog-to-digital conversion stages, and related electronic sensor." U.S. Patent No. 11,152,950. 19 Oct. 2021 [46].


(12) **United States Patent**
**Akbari et al.**

(10) **Patent No.: US 11,152,950 B2**
(45) **Date of Patent: Oct. 19, 2021**

(54) **ANALOG-TO-DIGITAL CONVERSION DEVICE COMPRISING TWO CASCADED NOISE-SHAPING SUCCESSIVE APPROXIMATION REGISTER ANALOG-TO-DIGITAL CONVERSION STAGES, AND RELATED ELECTRONIC SENSOR**

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(72) Inventors: **Masoume Akbari**, Montréal (CA); **Mohamad Sawan**, Montréal (CA)

(73) Assignee: **THALES**, Courbevoie (FR)

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(21) Appl. No.: **17/127,528**

(22) Filed: **Dec. 18, 2020**

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(30) **Foreign Application Priority Data**

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***H03M 1/46*** (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ..... ***H03M 1/462*** (2013.01); ***H03M 1/0626*** (2013.01); ***H03M 1/1205*** (2013.01)

(58) **Field of Classification Search**
CPC ..... H03M 3/458; H03M 1/468; H03M 3/464; H03M 1/12; H03M 3/426; H03M 1/46;
(Continued)

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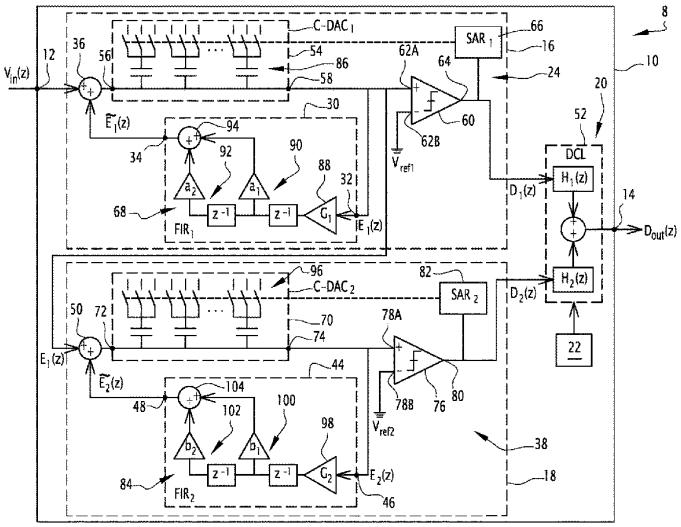
*Primary Examiner* — Linh V Nguyen
(74) *Attorney, Agent, or Firm* — Arent Fox LLP

(57) **ABSTRACT**

This analog-to-digital converting device comprises:
an input terminal for receiving the analog input signal;
an output terminal for issuing the digital output signal;
a first successive approximation register analog-to-digital conversion module, called first SAR ADC module, connected to the input terminal;
a first feedback module associated to the first SAR ADC module;
a second successive approximation register analog-to-digital conversion module, called second SAR ADC module, connected in a cascaded manner to the first SAR ADC module;
a second feedback module associated to the second SAR ADC module; and
a multiplexing module connected to the first and second SAR ADC modules, to deliver the digital output signal.

**13 Claims, 4 Drawing Sheets**



(51) **Int. Cl.**
***H03M 1/06*** (2006.01)
***H03M 1/12*** (2006.01)

(58) **Field of Classification Search**
CPC ..... H03M 3/46; H03M 1/68; H03M 3/30; H03M 3/424; H03M 3/454; H03M 1/00; H03M 3/416; H03M 3/414; H03M 7/3022; H03M 3/332; H03M 3/374; H03M 3/394; H03M 3/45; H03M 3/452; H03M 3/506; H03M 1/06; H03M 1/0641; H03M 1/145; H03M 1/164; H03M 1/44; H03M 3/32; H03M 3/338; H03M 3/35; H03M 3/352; H03M 3/358
USPC ..... 341/118–120, 143, 155, 163, 172
See application file for complete search history.

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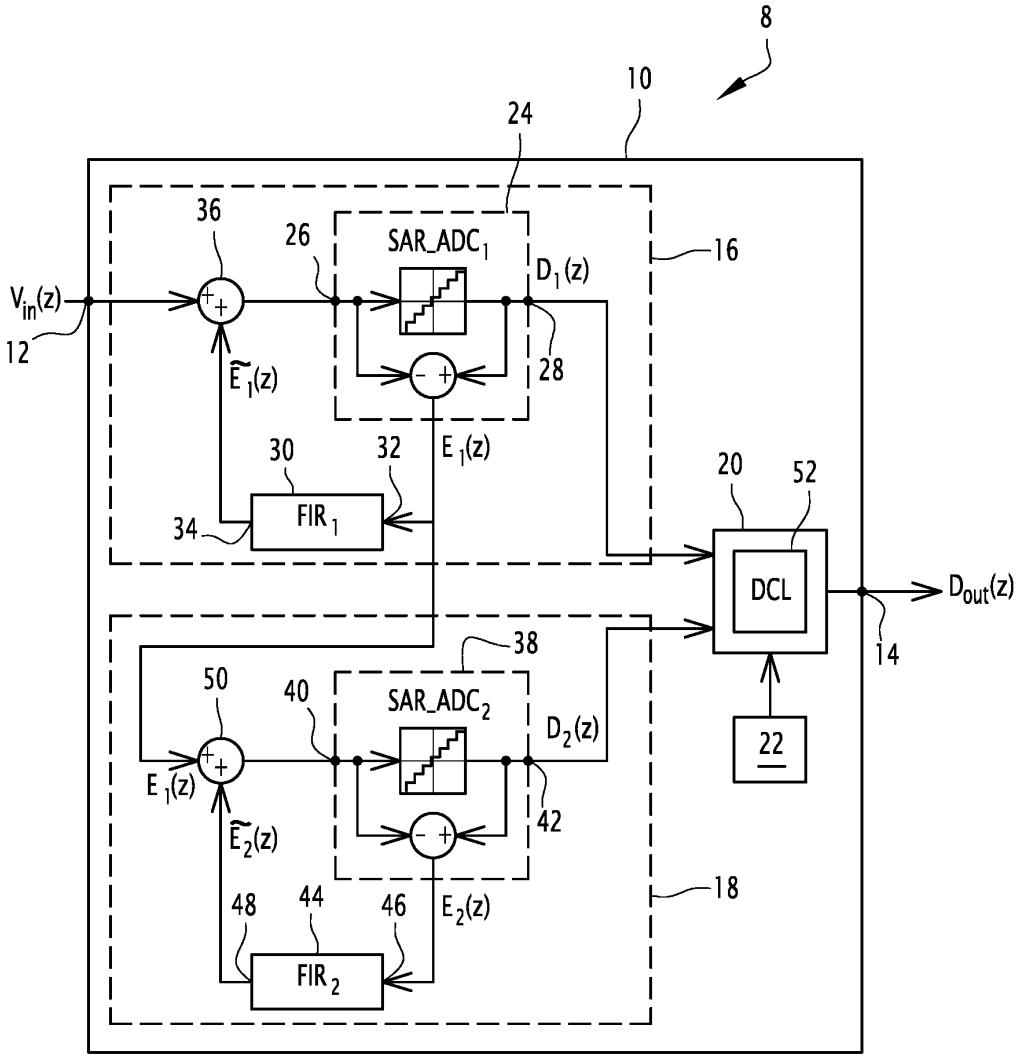
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10
24
36
26
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D1(z)
16
Vin(z)
12
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28
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E1(z)
20
52
FIR1
34
DCL
Dout(z)
14
38
50
40
SAR_ADC2
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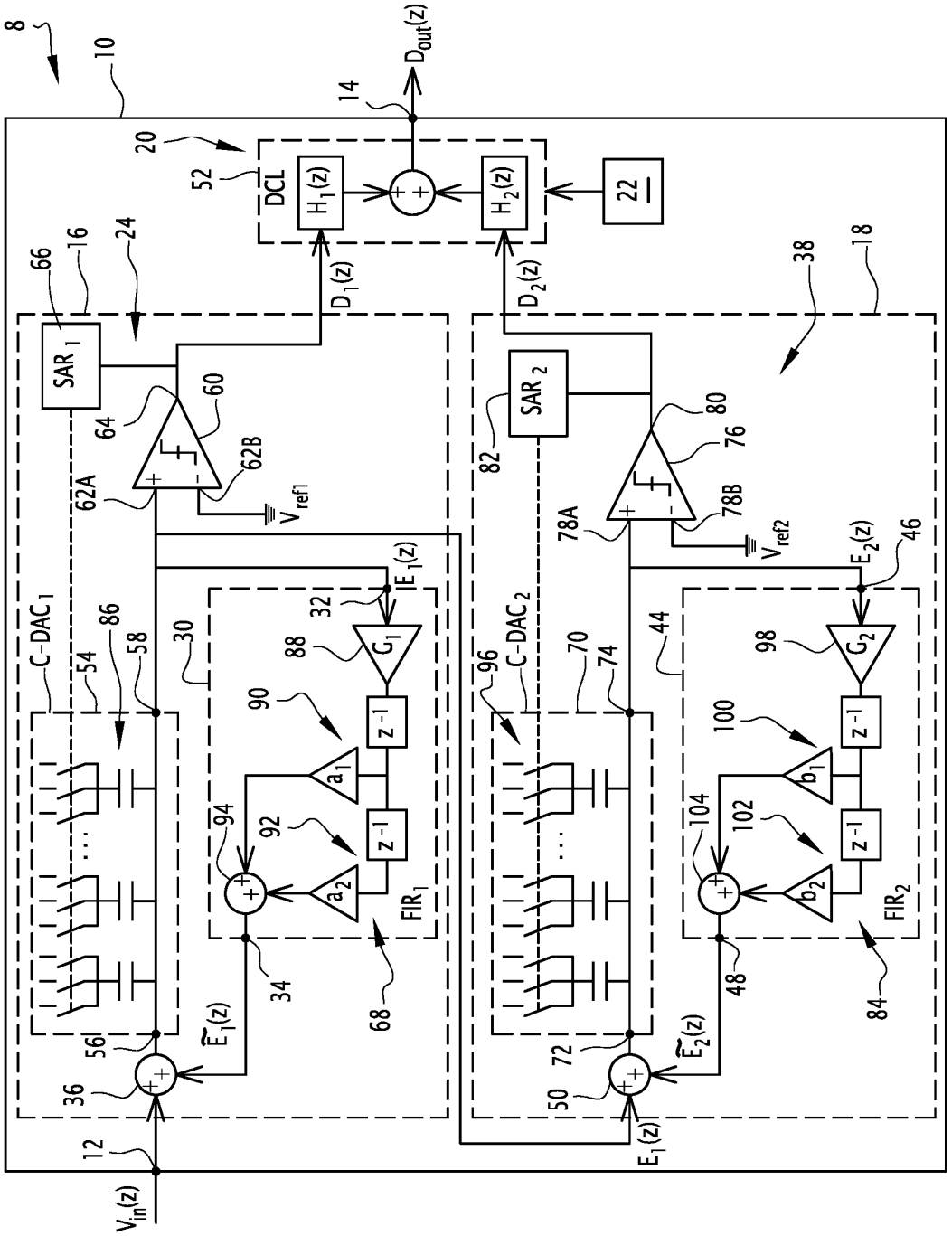
E2(z)
FIR2

FIG.1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38
18
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$SAR_2$
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76
78B
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30
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94
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68
96
70
74
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102
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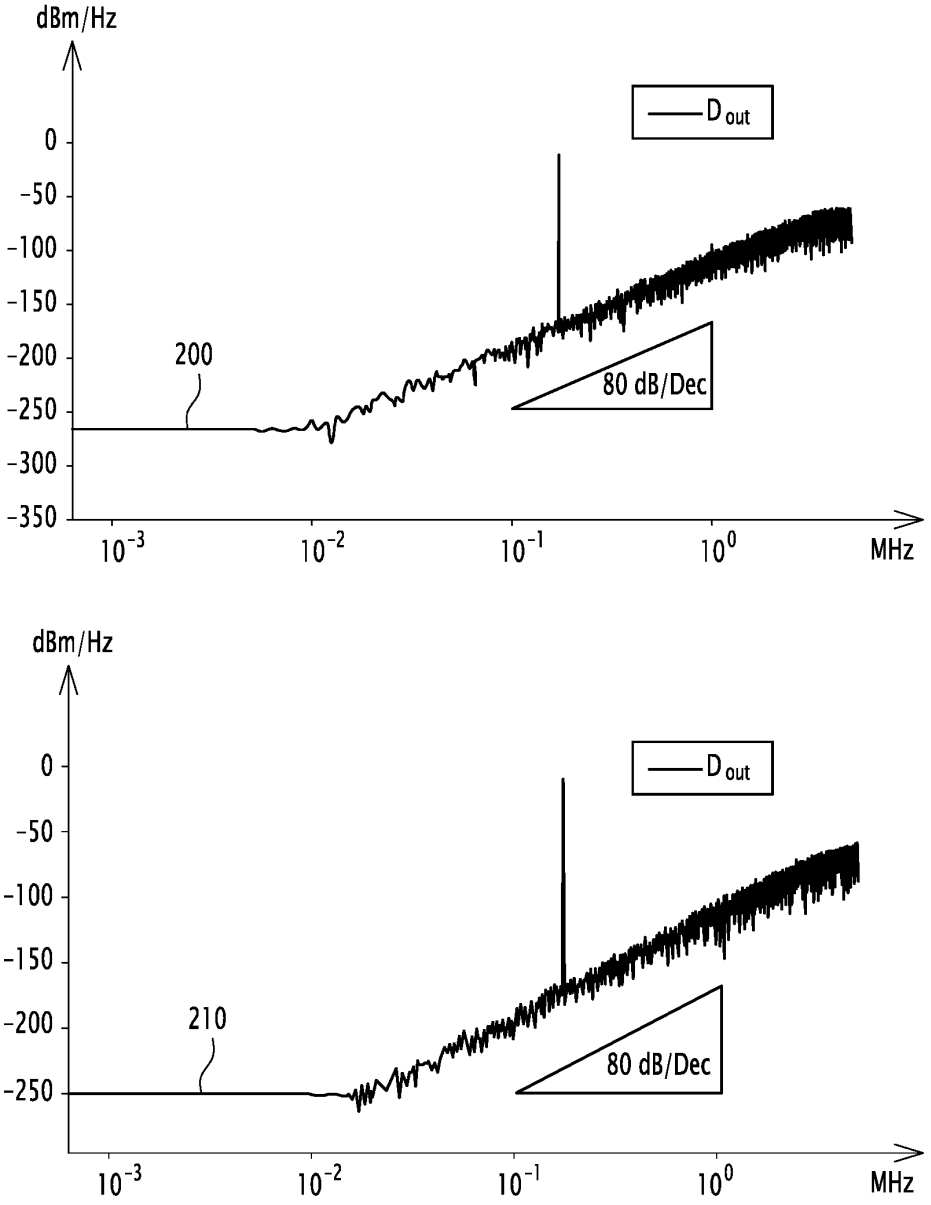
$V_{in}(z)$

FIG.2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-150
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-300
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80 dB/Dec
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$10^{-2}$
$10^{-1}$
$10^{0}$
MHz
dBm/Hz
0
-50
-100
-150
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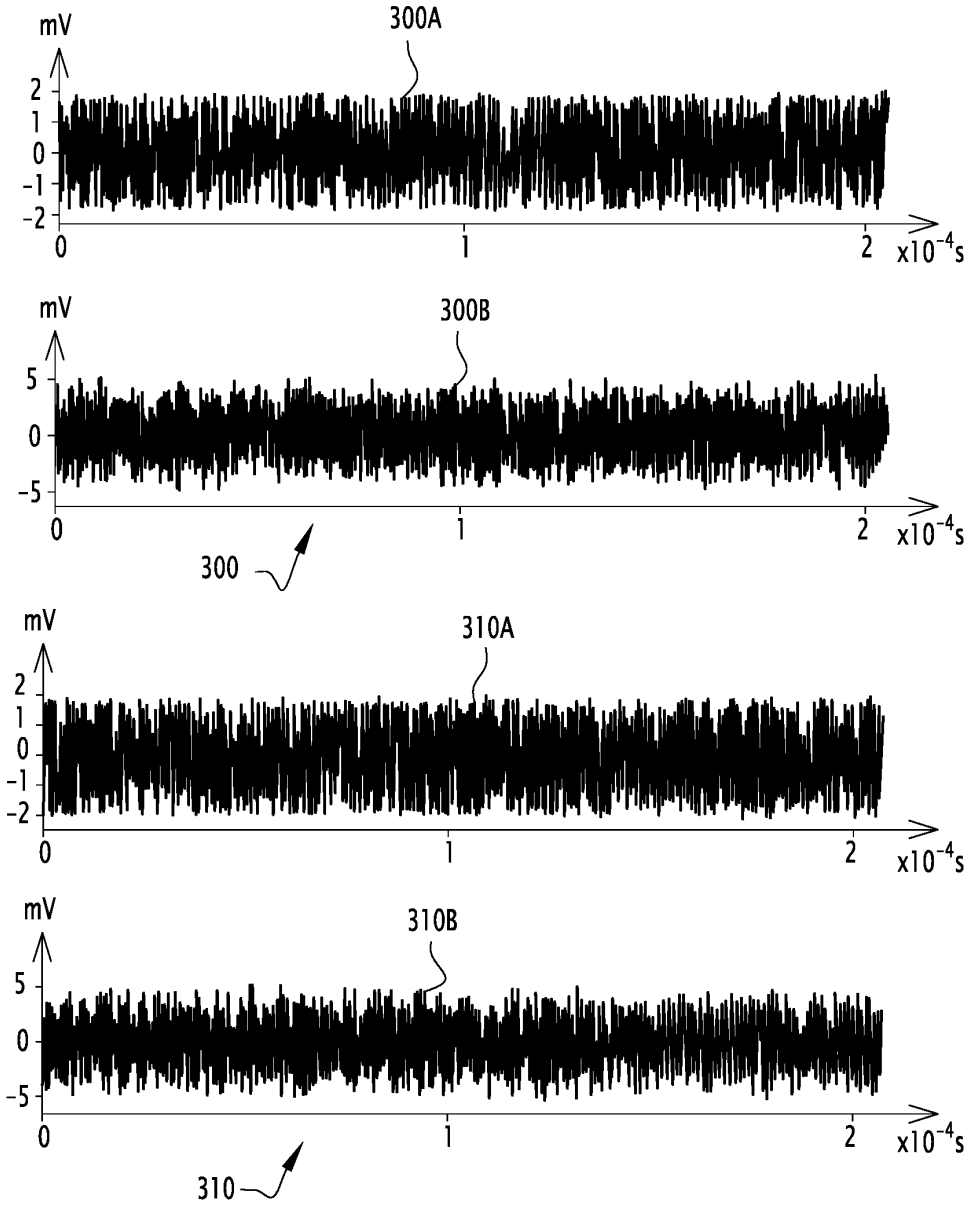
MHz

FIG.3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300B
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0
-5
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x10^-4s
300
mV
310A
2
1
0
-1
-2
0
1
2
x10^-4s
mV
310B
5
0
-5
0
1
2
x10^-4s
310

FIG.4

# ANALOG-TO-DIGITAL CONVERSION DEVICE COMPRISING TWO CASCADED NOISE-SHAPING SUCCESSIVE APPROXIMATION REGISTER ANALOG-TO-DIGITAL CONVERSION STAGES, AND RELATED ELECTRONIC SENSOR

## CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a U.S. non-provisional application claiming the benefit of French Application No. 19 15610, filed on Dec. 26, 2019, which is incorporated herein by reference in its entirety.

## FIELD

The present invention relates to an analog-to-digital converting device for converting an analog input signal into a digital output signal.

The invention also relates to an electronic sensor comprising such an analog-to-digital converting device.

## BACKGROUND

This invention concerns the field of analog-to-digital converters, also denoted ADC, in particular in high-channel-density data-acquisition systems. Such analog-to-digital converters are typically used in biomedical and instrumentation applications.

Successive approximation register analog-to-digital converters, also denoted SAR ADC, are popular in multiplexed systems because of their low latency and fast response, even to a full-scale input step without any settling issues, as explained in the article "*Demystifying High-Performance Multiplexed Data-Acquisition Systems*" from M. Pachchigar, in Analog Dialogue, 2014. Successive approximation register analog-to-digital converters have been widely used in energy-efficient applications due to their simplicity and power efficiency.

A successive approximation register analog-to-digital converter typically includes a digital-to-analog converter, also denoted DAC, with an input and an output; a comparator with two inputs and an output, one input being connected to the output of the digital-to-analog converter and the other input being adapted to receive a reference signal; and a SAR logic unit connected to the output of the comparator, the SAR logic unit being adapted to control the digital-to-analog converter. The digital-to-analog converter generally contains a capacitor array.

US 2018/0183450 A1 concerns an interleaving successive approximation register analog-to-digital converter (SAR ADC) with noise-shaping having a first successive approximation register block, also called first SAR block, a second successive approximation register block, also called second SAR block, and a noise-shaping circuit. The first and second SAR blocks take turns to sample an input voltage for successive approximation of the input voltage and observation of a digital representation of the input voltage. The noise-shaping circuit receives a first residue voltage from the first SAR block and receives a second residue voltage from the second SAR block alternately, and outputs a noise-shaping signal to be fed into the first SAR block and the second SAR block. Such a successive approximation register analog-to-digital converter allows increasing the speed of the process, because when one SAR block is in conversion mode, the other one samples the next input.



However, successive approximation register analog-to-digital converters are suffering from significant noise of the comparator, as well as extra power needed to drive a large DAC capacitor array. Therefore, such successive approximation register analog-to-digital converters are barely used for more than 10-12 bit resolution applications.

## SUMMARY

An object of the invention is therefore to provide an improved analog-to-digital converting device comprising at least one successive approximation register analog-to-digital converter.

For this purpose, the subject-matter of the invention is an analog-to-digital converting device for converting an analog input signal into a digital output signal, comprising:

- an input terminal for receiving the analog input signal;
- an output terminal for issuing the digital output signal;
- a first successive approximation register analog-to-digital conversion module, called first SAR ADC module, connected via its input to the input terminal and configured to deliver via its output a first digital signal;
- a first feedback module configured to receive a first residue signal from the first SAR ADC module and to process and inject it back at input of the first SAR ADC module;
- a second successive approximation register analog-to-digital conversion module, called second SAR ADC module, connected via its input to the first SAR ADC module to receive the first residue signal and configured to deliver via its output a second digital signal;
- a second feedback module configured to receive a second residue signal from the second SAR ADC module and to process and inject it back at input of the second SAR ADC module; and
- a multiplexing module connected to the output of the first SAR ADC module and to the output of the second SAR ADC module, the multiplexing module being configured to deliver the digital output signal at the output terminal.

The analog-to-digital converting device according to the invention therefore comprises two cascaded noise-shaping successive approximation register analog-to-digital conversion stages, also called NS-SAR ADC stages, namely a first NS-SAR ADC stage and a second NS-SAR ADC stage, each NS-SAR ADC stage including a SAR ADC module and a respective error feedback module to noise-shape a quantization noise of the SAR ADC module. The quantization noise of the first NS-SAR ADC stage, in particular of the first SAR ADC module, is fed into the second NS-SAR ADC stage to form a multi-stage noise-shaping (MASH) SAR ADC.

The skilled person will further note that the noise-shaping is performed by an error feedback technique such that the analog-to-digital converting device according to the invention is no longer using any operational transconductance amplifier (OTA). Therefore, it is indeed an OTA-free topology.

In optional addition, the multiplexing module is able to operate either in a first operating mode wherein the delivered digital output signal is the first digital signal or in a second operating mode wherein the delivered digital output signal is a combination of the first and second digital signals. Therefore, a further advantage of the analog-to-digital converting device according to the invention is the configurability such

that it can be configured as either single-stage or multi-stage to support different bandwidths and resolutions.

In optional addition, each feedback module includes a respective second-order filter for filtering the respective residue signal before injecting it back at input of the respective SAR ADC module. Therefore, a further advantage of the analog-to-digital converting device according to the invention is to provide a fourth-order noise-shaping performance while being as stable as a second-order analog-to-digital converter.

According to other advantageous aspects of the invention, the analog-to-digital converting device comprises one or several of the following features, taken individually or according to any technically possible combination:

- the multiplexing module is configured to operate in a first operating mode wherein the delivered digital output signal is the first digital signal or in a second operating mode wherein the delivered digital output signal is a combination of the first and second digital signals;
- the converting device further comprises a selection module for selecting an operating mode among the first operating mode and the second operating mode of the multiplexing module;
- the first feedback module comprises a first filter for filtering the first residue signal before injecting it back at input of the first SAR ADC module,
- the first filter being preferably a second-order filter;
- the first filter being still preferably a finite impulse response filter;
- the second feedback module comprises a second filter for filtering the second residue signal before injecting it back at input of the second SAR ADC module,
- the second filter being preferably a second-order filter;
- the second filter being still preferably a finite impulse response filter;
- the first SAR ADC module comprises:
  - a first digital-to-analog converter with an input and an output;
  - a first comparator with two inputs and an output, one input being connected to the output of the first digital-to-analog converter and the other input being adapted to receive a reference signal; and
  - a first successive approximation register logic unit connected to the output of the first comparator, the first successive approximation register logic unit being adapted to control the first digital-to-analog converter;
  - the input of the first digital-to-analog converter forming the input of the first SAR ADC module;
  - the output of the first comparator forming the output of the first SAR ADC module;
- the input of the second SAR ADC module is connected to the output of the first digital-to-analog converter;
- the second SAR ADC module comprises:
  - a second digital-to-analog converter with an input and an output;
  - a second comparator with two inputs and an output, one input being connected to the output of the second digital-to-analog converter and the other input being adapted to receive a reference signal; and
  - a second successive approximation register logic unit connected to the output of the second comparator, the second successive approximation register logic unit being configured to control the second digital-to-analog converter;
  - the input of the second digital-to-analog converter forming the input of the second SAR ADC module;
  - the output of the second comparator forming the output of the second SAR ADC module;
- the multiplexing module comprises a digital cancellation logic unit adapted to apply a first transfer function to the first digital signal and a second transfer function to the second digital signal, so as to cancel the first residue signal.

The subject-matter of the invention is also an electronic sensor comprising an analog-to-digital converting device for converting an analog input signal into a digital output signal, the converting device being as defined above.

## BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be better understood upon reading of the following description, which is given solely by way of example and with reference to the appended drawings, wherein:

FIG. **1** is a schematic view of an electronic sensor comprising an analog-to-digital converting device according to the invention, the converting device including a first NS-SAR ADC stage and a second NS-SAR ADC stage, the second NS-SAR ADC stage being connected in a cascaded manner to the first NS-SAR ADC stage, in order to feed a quantization noise of the first NS-SAR ADC stage into the second NS-SAR ADC stage; this view being in the form of a block diagram, also called linear model;

FIG. **2** is a view similar to the one of FIG. **1**, in the form of a time-domain behavioral model;

FIG. **3** is a set of two curves, each representing a simulated power spectral density of a digital output signal delivered by the analog-to-digital converting device, a first curve corresponding to the linear model of FIG. **1** and a second curve corresponding to the time-domain behavioral model of FIG. **2**; and

FIG. **4** is a set of two pairs of curves, each representing a time-domain error signal and respectively a filtered error signal for the second SAR ADC stage, a first pair of curves corresponding to the linear model of FIG. **1** and a second pair of curves corresponding to the time-domain behavioral model of FIG. **2**.

## DETAILED DESCRIPTION

In the following description, NS stands for Noise-Shaping; SAR stands for Successive Approximation Register; and ADC stands for Analog-to-Digital Converter or Analog-to-Digital Conversion. Thus, NS-SAR ADC stands for a noise-shaping successive approximation register analog-to-digital converter, or conversion stage.

In FIG. **1**, an electronic sensor **8** comprises an analog-to-digital converting device **10** for converting an analog input signal $V_{in}(z)$ into a digital output signal $D_{out}(z)$. The electronic sensor **8** is adapted to be used in various applications, such as biomedical and/or instrumentation applications.

The analog-to-digital converting device **10** is configured to convert the analog input signal $V_{in}(z)$ into the digital output signal $D_{out}(z)$ and comprises an input terminal **12** for receiving the analog input signal $V_{in}(z)$ and an output terminal **14** for issuing the digital output signal $D_{out}(z)$.

The analog-to-digital converting device **10** further comprises a first noise-shaping successive approximation register analog-to-digital conversion stage **16**, also called first NS-SAR ADC stage, and a second noise-shaping successive approximation register analog-to-digital conversion stage **18**, also called second NS-SAR ADC stage, the second NS-SAR ADC stage **18** being connected in a cascaded

manner to the first NS-SAR ADC stage **16**, and a multiplexing module **20** connected respectively to the output of first NS-SAR ADC stage **16** and to the output of second NS-SAR ADC stage **18**, the multiplexing module **20** being configured to deliver the digital output signal $D_{out}(z)$ at the output terminal **14**, from a first digital signal $D_1(z)$ coming from the first stage NS-SAR ADC **16**, or additionally from a second digital signal $D_2(z)$ coming from the second stage NS-SAR ADC **18**.

The skilled person will understand that the term "multiplexing" generally refers to the act of grouping information or signals from several channels on a single channel. The multiplexing module **20** shall then be understood as a module capable of grouping together at output terminal **14** the signals coming from several channels, i.e. the signals coming from the NS-SAR ADC stages **16**, **18**, the multiplexing module **20** being configured to deliver the digital output signal $D_{out}(z)$ at the output terminal **14**, this from the first digital signal $D_1(z)$ coming from the first NS-SAR ADC **16** stage, or even additionally from the second digital signal $D_2(z)$ coming from the second NS-SAR ADC **18** stage, i.e. from the combination of the first digital signal $D_1(z)$ and the second digital signal $D_2(z)$.

As an optional addition, the multiplexing module **20** is configured to operate in a first operating mode M**1** wherein the delivered digital output signal $D_{out}(z)$ is the first digital signal $D_1(z)$ or in a second operating mode M**2** wherein the delivered digital output signal $D_{out}(z)$ is a combination of the first and second digital signals $D_1(z)$, $D_2(z)$.

According to this optional addition, the converting device **10** further comprises a selection module **22** configured to select an operating mode among the first operating mode M**1** and the second operating mode M**2** of the multiplexing module **20**.

The first NS-SAR ADC stage **16** includes a first successive approximation register analog-to-digital conversion module **24**, called first SAR ADC module **24**, also denoted $SAR\_ADC_1$, connected via its input **26** to the input terminal **12** and configured to deliver via its output **28** a first digital signal $D_1(z)$.

The first NS-SAR ADC stage **16** also includes a first feedback module **30** configured to receive via its input **32** a first residue signal $E_1(z)$ from the first SAR ADC module **24** and to process and inject it back, via its output **34**, at input **26** of the first SAR ADC module **24**.

In the example of FIG. **1**, the first NS-SAR ADC stage **16** includes a first adder **36** connected on one hand to the input terminal **12** and to the output **34** of the first feedback module **30**, and on the other hand to the input **26** of the first SAR ADC module **24**. The first adder **36** is configured for adding the signal processed by the first feedback module **30**, also denoted $\widetilde{E_1}(z)$, to the analog input signal $V_{in}(z)$ and for delivering this sum of signals $\widetilde{E_1}(z)+V_{in}(z)$ to the input **26** of the first SAR ADC module **24**.

The second NS-SAR ADC stage **18** includes a second successive approximation register analog-to-digital conversion module **28**, called second SAR ADC module **38**, also denoted $SAR\_ADC_2$, connected via its input **40** to the first SAR ADC module **24** to receive the first residue signal $E_1(z)$ and configured to deliver via its output **42** a second digital signal $D_2(z)$.

The second NS-SAR ADC stage **18** also includes a second feedback module **44** configured to receive via its input **46** a second residue signal $E_2(z)$ from the second SAR ADC module **38** and to process and inject it back, via its output **48**, at input **40** of the second SAR ADC module **38**.

In the example of FIG. **1**, the second NS-SAR ADC stage **18** includes a second adder **50** connected on one hand to the first NS-SAR ADC stage **16** and to the output **48** of the second feedback module **44**, and on the other hand to the input **40** of the second SAR ADC module **38**. The second adder **50** is configured for adding the signal processed by the second feedback module **44**, also denoted $\widetilde{E_2}(z)$, to the first residue signal $E_1(z)$ and for delivering this sum of signals $\widetilde{E_2}(z)+E_1(z)$ to the input **40** of the second SAR ADC module **38**.

The multiplexing module **20** is configured to deliver the digital output signal $D_{out}(z)$ from the first digital signal $D_1(z)$ and the second digital signal $D_2(z)$. The multiplexing module **20** is connected to the output **28** of the first SAR ADC module **24** and to the output **42** of the second SAR ADC module **38**.

The multiplexing module **20** is preferably configured to deliver, as the digital output signal $D_{out}(z)$ at the output terminal **14**, either the first digital signal $D_1(z)$ or the combination of the first $D_1(z)$ and second $D_2(z)$ digital signals.

The multiplexing module **20** includes a digital cancellation logic unit **52**, also denoted DCL, adapted to apply a first transfer function $H_1(z)$ to the first digital signal $D_1(z)$ and a second transfer function $H_2(z)$ to the second digital signal $D_2(z)$, as shown in FIG. **2**. The digital cancellation logic unit **52** is adapted to cancel the first residue signal $E_1(z)$.

In the example of FIG. **2**, the first SAR ADC module **24** includes a first digital-to-analog converter **54**, also denoted $C\text{-}DAC_1$, with an input **56** and an output **58**. The input **56** of the first digital-to-analog converter **54** forms the input **26** of the first SAR ADC module **24**.

The skilled person will observe that the input **56**, which forms the input of the first SAR ADC module **24** whose function is to perform analog-to-digital conversion, is an input of the first digital-to-analog converter **54**, but not its single input. The skilled person will then understand that the input **56** is an analog input corresponding to an additional input, known per se for a SAR ADC module, of said digital-to-analog converter **54**, and not the digital input intended to receive the digital signal for conversion to an analog signal. The additional input **56** is configured for receiving a reference voltage used to normalize said digital input. In the example of FIG. **2**, said reference voltage corresponds to the signal delivered by the first adder **36** to the first SAR ADC module **24**, i.e. corresponds to the sum of signals $\widetilde{E_1}(z)+V_{in}(z)$.

The first SAR ADC module **24** also includes a first comparator **60** with two inputs **62**A, **62**B, namely a first input **62**A and a second input **62**B, and an output **64**. One input of the first comparator **60**, such as the first input **62**A, is connected to the output **58** of the first digital-to-analog converter **54** and the other input, such as the second input **62**A, is adapted to receive a reference signal, such a first reference voltage $V_{ref1}$. The output **64** of the first comparator **60** forms the output **28** of the first SAR ADC module **24**.

The first SAR ADC module **24** further includes a first successive approximation register logic unit **66**, also called first SAR logic unit **66** and denoted $SAR_1$, connected to the output **64** of the first comparator **60**, the first SAR logic unit **66** being adapted to control the first digital-to-analog converter **54**.

The first feedback module **30** includes a first filter **68** for filtering the first residue signal $E_1(z)$ before injecting it, as a first filtered residue signal $\widetilde{E_1}(z)$, back at input **26** of the first SAR ADC module **24**.

In the example of FIG. **2**, the second SAR ADC module **38** includes a second digital-to-analog converter **70**, also denoted C-DAC$_2$, with an input **72** and an output **74**. The input **72** of the second digital-to-analog converter **70** forms the input **40** of the second SAR ADC module **38**.

The skilled person will observe that the input **72**, which forms the input of the second SAR ADC module **58** whose function is to perform analog-to-digital conversion, is an input of the second digital-to-analog converter **70**, but not its single input. The skilled person will then understand that the input **72** is an analog input corresponding to an additional input, known per se for a SAR ADC module, of said digital-to-analog converter **70**, and not the digital input intended to receive the digital signal for conversion to an analog signal. The additional input **72** is configured for receiving a reference voltage used to normalize said digital input. In the example of FIG. **2**, said reference voltage corresponds to the signal delivered by the second adder **50** to the second SAR ADC module **38**, i.e. corresponds to the sum of signals $\widetilde{E_2}(z)$+E$_1$(z).

The second SAR ADC module **38** also includes a second comparator **76** with two inputs **78**A, **78**B, namely a first input **78**A and a second input **78**B, and an output **80**. One input of the second comparator **76**, such as the first input **78**A, is connected to the output **74** of the second digital-to-analog converter **70** and the other input, such as the second input **78**B, is adapted to receive a reference signal, such a second reference voltage $V_{ref2}$. The output **80** of the second comparator **76** forms the output **42** of the second SAR ADC module **38**.

The second SAR ADC module **38** further includes a second successive approximation register logic unit **82**, also called second SAR logic unit **82** and denoted SAR$_2$, connected to the output **80** of the second comparator **76**, the second SAR logic unit **82** being adapted to control the second digital-to-analog converter **70**.

The second feedback module **44** includes a second filter **84** for filtering the second residue signal E$_2$(z) before injecting it, as a second filtered residue signal $\widetilde{E_2}(z)$, back at input **40** of the second SAR ADC module **38**.

The digital cancellation logic unit **52** is for example configure to apply the first transfer function H$_1$(z) to the first digital signal D$_1$(z) and the second transfer function H$_2$(z) to the second digital signal D$_2$(z), according to the following equation:

$$D_{out}(z)=H_1(z)\cdot D_1(z)+H_2(z)\cdot D_2(z) \quad \text{[Math 1]}$$

where D$_{out}$ represents the digital output signal,
H$_1$ represents the first transfer function,
D$_1$ represents the first digital signal,
H$_2$ represents the second transfer function, and
D$_2$ represents the second digital signal.

The first digital signal D$_1$(z) verifies for example the following equation:

$$D_1(z)=\mathrm{STF}_1(z)\cdot V_{in}(z)+\mathrm{NTF}_1(z)\cdot E_1(z) \quad \text{[Math 2]}$$

where D$_1$ represents the first digital signal,
STF$_1$ represents a first signal transfer function,
$V_{in}$ represents the analog input signal,
NTF$_1$ represents a first noise transfer function, and
E$_1$ represents the first residue signal.

The second digital signal D$_2$(z) verifies for example the following equation:

$$D_2(z)=\mathrm{STF}_2(z)\cdot E_1(z)\mathrm{NTF}_2(z)\cdot E_2(z) \quad \text{[Math 3]}$$

where D$_2$ represents the second digital signal,
STF$_2$ represents a second signal transfer function,
E$_1$ represents the first residue signal,
NTF$_2$ represents a second noise transfer function, and
E$_2$ represents the second residue signal.

According to aforementioned equations (1), (2) and (3), the digital output signal D$_{out}$(z) verifies the following equation, written in a condensed manner:

$$D_{out}(z)=H_1\cdot[\mathrm{STF}_1\cdot V_{in}(z)+\mathrm{NTF}_1\cdot E_1(z)]+H_2\cdot[\mathrm{STF}_2\cdot E_1(z)+\mathrm{NTF}_2\cdot E_2(z)] \quad \text{[Math 4]}$$

thereby leading to the following equation, written in a condensed manner:

$$D_{out}(z)=H_1\cdot\mathrm{STF}_1\cdot V_{in}(z)+[H_1\cdot\mathrm{NTF}_1+H_2\cdot\mathrm{STF}_2]\cdot E_1(z)+H_2\cdot\mathrm{NTF}_2\cdot E_2(z) \quad \text{[Math 5]}$$

Therefore, according to equation (5), the following equation is verified so as to cancel the first residue signal E$_1$(z):

$$H_1(z)\cdot\mathrm{NTF}_1(z)+H_2(z)\cdot\mathrm{STF}_2(z)=0 \quad \text{[Math 6]}$$

In the example of FIG. **2**, the first digital-to-analog converter **54**, denoted C-DAC$_1$, contains a first capacitor array **86**.

The first filter **68** is preferably a Finite Impulse Response filter, also called FIR filter, and accordingly denoted FIR$_1$.

The first filter **68** is preferably a second-order filter.

The first noise transfer function NTF$_1$(z) typically verifies the following equation:

$$\mathrm{NTF}_1(z)=1-H_{F1}(z) \quad \text{[Math 7]}$$

where NTF$_1$ represents the first noise transfer function, and
H$_{F1}$ represents a transfer function of the first filter **68**.

In the example of FIG. **2**, the first filter **68** is preferably a second-order FIR filter. According to this example, the first filter **68** includes a first gain unit **88** for applying a gain G**1** to the first residue signal E$_1$(z), a first first-stage delay unit **90** with gain a$_1$ connected to output of the first gain unit **88**, a first second-stage delay unit **92** with gain a$_2$ connected to output of the first first-stage delay unit **90**, and a third adder **94** connected to both outputs of the first first-stage delay unit **90** and the first second-stage delay unit **92**.

According to this example, the transfer function of the first filter **68** verifies the following equation:

$$H_{F1}(z)=G_1\cdot(a_1z^{-1}+a_2z^{-2}) \quad \text{[Math 8]}$$

An ideal first noise transfer function NTF$_1$(z) for second order noise shaping verifies the following equation, which requires G$_1$=2, a$_1$=1 and a$_2$=−0.5 as parameter values:

$$\mathrm{NTF}_1(z)=(1-z^{-1})^2 \quad \text{[Math 9]}$$

In the example of FIG. **2**, the second digital-to-analog converter **70**, denoted C-DAC$_2$, contains a second capacitor array **96**.

The second filter **84** is preferably a Finite Impulse Response filter, also called FIR filter, and accordingly denoted FIR$_2$.

The second filter **84** is preferably a second-order filter.

The second noise transfer function NTF$_2$(z) typically verifies the following equation:

$$\mathrm{NTF}_2(z)=1-H_{F2}(z) \quad \text{[Math 10]}$$

where NTF$_2$ represents the second noise transfer function, and
H$_{F2}$ represents a transfer function of the second filter **84**.

In the example of FIG. **2**, the second filter **84** is preferably a second-order FIR filter. According to this example, the second filter **84** includes a second gain unit **98** for applying a gain G**2** to the second residue signal E$_2$(z), a second first-stage delay unit **100** with gain b$_1$ connected to output of

the second gain unit **98**, a second second-stage delay unit **102** with gain $b_2$ connected to output of the second first-stage delay unit **100**, and a fourth adder **104** connected to both outputs of the second first-stage delay unit **100** and the second second-stage delay unit **102**.

According to this example, the transfer function of the second filter **84** verifies the following equation:

$$H_{F2}(z)=G_2\cdot(b_1z^{-1}+b_2z^{-2}) \quad \text{[Math 11]}$$

An ideal second noise transfer function $NTF_2(z)$ for second-order noise-shaping verifies the following equation, which requires $G_2=2$, $b_1=1$ and $b_2=-0.5$ as parameter values:

$$NTF_2(z)=(1-z^{-1})^2 \quad \text{[Math 12]}$$

Assuming that the first and second signal transfer functions $STF_1(z)$, $STF_2(z)$ are ideal and verify the following equation:

$$STF_1(z)=STF_2(z)=1 \quad \text{[Math 13]}$$

and also considering that the first transfer function $H_i(z)$ verifies the following equation:

$$H_1(z)=1 \quad \text{[Math 14]}$$

then aforementioned equations (6) and (9) lead to the following equation:

$$H_2(z)=-NTF_1(z)=-(1-z^{-1})^2 \quad \text{[Math 15]}$$

Therefore, in this example and according to equations (5), (6) and (12) to (15), the digital output signal $D_{out}(z)$ verifies the following equation:

$$D_{out}(z)=V_{in}(z)-(1-z^{-1})^4\cdot E_2(z) \quad \text{[Math 16]}$$

Thus, the aforementioned equation (16) confirms that when each feedback module **30**, **44** includes a respective second-order filter **68**, **84** for filtering the respective residue signal $E_1(z)$, $E_2(z)$ before injecting it back at input of the respective SAR ADC module **24**, **38**, the analog-to-digital converting device **10** according to the invention provides a fourth-order noise-shaping performance.

The analog-to-digital converting device **10** according to the invention therefore allows obtaining improved results in comparison with state-of-the-art analog-to-digital converting devices, as it will be explained hereinafter in view of FIGS. **3** and **4**.

FIG. **3** is a set of two curves **200**, **210**, namely a first curve **200** and a second curve **210**, each curve **200**, **210** representing a simulated power spectral density of the digital output signal $D_{out}$ delivered by the analog-to-digital converting device **10**, the first curve **200** corresponding to the linear model of FIG. **1** and the second curve **210** corresponding to the time-domain behavioral model of FIG. **2**.

FIG. **3** therefore shows the power spectral density of the linear model and the behavioral model of the invention and demonstrates similar results for the two realizations. The 80 dB/Dec slope of each curve **200**, **210** further proves the fourth-order noise-shaping performance of the analog-to-digital converting device **10** according to the invention.

FIG. **4** is a set of two pairs **300**, **310** of curves, namely a first pair **300** and a second pair **310**, each pair **300**, **310** representing a time-domain error signal and respectively a filtered error signal for the second NS-SAR ADC stage **18**. The first pair **300** corresponds to the linear model of FIG. **1** and the second pair **310** corresponds to the time-domain behavioral model of FIG. **2**.

In FIG. **4**, the first pair **300** includes a third curve **300**A representing the time-domain error signal and a fourth curve **300**B representing the filtered error signal for the second NS-SAR ADC stage **18**, according to the linear model of FIG. **1**. Similarly, the second pair **310** includes a fifth curve **310**A representing the time-domain error signal and a sixth curve **310**B representing the filtered error signal for the second NS-SAR ADC stage **18**, according to the time-domain behavioral model of FIG. **2**.

FIG. **4** therefore compares the time-domain error signal of the second NS-SAR ADC stage **18** for the two realizations. It also shows how filtering affects this error. As can be seen, it adds some noise to the analog-to-digital converting device **10**, but it is not significant and cannot destroy the performance of the analog-to-digital converting device **10**.

Thus, the analog-to-digital converting device **10** according to the invention offers several advantages in comparison to conventional noise-shaping successive approximation register analog-to-digital converters, as it will explained hereinafter.

First, the analog-to-digital converting device **10** according to the invention obtains a higher noise-shaping order by cascading NS-SAR ADC stages **16**, **18** with a lower noise-shaping order capability and without stability concerns.

Then, extra circuit components are not required for the extraction of the error signal in the first NS-SAR ADC stage **16** to feed it as the input of the second NS-SAR ADC stage **18**. So, the analog-to-digital converting device **10** has a simpler architecture because the analog error signal $E_1(z)$, $E_2(z)$ already exists on the respective digital-to-analog converter **54**, **70**, such as on the respective capacitor array **86**, **96**, at the end of a conversion. Further, the analog error signal $E_1(z)$ of the first digital-to-analog converter **54**, such as on the first capacitor array **86**, is usable as the input of the second NS-SAR ADC stage **18**.

This also makes the analog-to-digital converting device **10** according to the invention more precise than conventional MASH converters, because of removing a digital-to-analog conversion of the respective output **28**, **42** of SAR ADC module **24**, **38**, i.e. the quantizer's output, and also because of removing a subtracting step.

Further, each NS-SAR ADC stage **16**, **18** provides a digital signal, namely the respective first and second digital signals $D_1(z)$, $D_2(z)$, with a specific resolution, so that the analog-to-digital converting device **10** allows providing two different resolutions simultaneously, namely a first resolution corresponding to the first operating mode M**1** wherein the digital output signal $D_{out}(z)$ delivered is the first digital signal $D_1(z)$, and a second resolution corresponding to the second operating mode M**2** wherein the digital output signal $D_{out}(z)$ delivered is a combination of the first and second digital signals $D_1(z)$, $D_2(z)$, for example at output of the digital cancellation logic **52**.

The analog-to-digital converting device **10** according to the invention also offers flexibility for changing the noise-shaping order and resolution using a combination of the different NS-SAR ADC stages **16**, **18**, in particular via the selection module **22**, which is able to select an operating mode from the first operating mode M**1** and the second operating mode M**2** of the multiplexer module **20**. Therefore, the analog-to-digital converting device **10** provides a reconfigurable resolution architecture.

In addition, there is no restriction on the type of the feedback modules **30**, **44**, such as loops, loop filters or FIR filters, in the NS-SAR ADC stages **16**, **18**.

Further, the noise-shaping is performed by an error feedback technique, and the analog-to-digital converting device **10** according to the invention is no longer using operational transconductance amplifier (OTA). In other words, the analog-to-digital converting device **10** offers preferably an OTA-free topology.

The invention claimed is:

1. An analog-to-digital converting device for converting an analog input signal into a digital output signal, comprising:

an input terminal for receiving the analog input signal;

an output terminal for issuing the digital output signal;

a first successive approximation register analog-to-digital conversion module, called first SAR ADC module, connected via its input to the input terminal and configured to deliver via its output a first digital signal;

a first feedback module configured to receive a first residue signal from the first SAR ADC module and to process and inject it back at input of the first SAR ADC module;

a second successive approximation register analog-to-digital conversion module, called second SAR ADC module, connected via its input to the first SAR ADC module to receive the first residue signal and configured to deliver via its output a second digital signal;

a second feedback module configured to receive a second residue signal from the second SAR ADC module and to process and inject it back at input of the second SAR ADC module; and

a multiplexing module connected to the output of the first SAR ADC module and to the output of the second SAR ADC module, the multiplexing module being configured to deliver the digital output signal at the output terminal,

the first feedback module comprising a first filter for filtering the first residue signal before injecting it back at input of the first SAR ADC module.

2. The converting device according to claim 1, wherein the multiplexing module is configured to operate in a first operating mode wherein the delivered digital output signal is the first digital signal or in a second operating mode wherein the delivered digital output signal is a combination of the first and second digital signals.

3. The converting device according to claim 2, wherein the converting device further comprises a selection module for selecting an operating mode among the first operating mode and the second operating mode of the multiplexing module.

4. The converting device according to claim 1, wherein the first filter is a second order filter.

5. The converting device according to claim 1, wherein the first filter is a finite impulse response filter.

6. The converting device according to claim 1, wherein the second feedback module comprises a second filter for filtering the second residue signal before injecting it back at input of the second SAR ADC module.

7. The converting device according to claim 6, wherein the second filter is a second order filter.

8. The converting device according to claim 6, wherein the second filter is a finite impulse response filter.

9. The converting device according to claim 1, wherein the first SAR ADC module comprises:

a first digital-to-analog converter with an input and an output;

a first comparator with two inputs and an output, one input being connected to the output of the first digital-to-analog converter and the other input being adapted to receive a reference signal; and

a first successive approximation register logic unit connected to the output of the first comparator, the first successive approximation register logic unit being adapted to control the first digital-to-analog converter;

the input of the first digital-to-analog converter forming the input of the first SAR ADC module;

the output of the first comparator forming the output of the first SAR ADC module.

10. The converting device according to claim 9, wherein the input of the second SAR ADC module is connected to the output of the first digital-to-analog converter.

11. The converting device according to claim 1, wherein the second SAR ADC module includes:

a second digital-to-analog converter with an input and an output;

a second comparator with two inputs and an output, one input being connected to the output of the second digital-to-analog converter and the other input being adapted to receive a reference signal; and

a second successive approximation register logic unit connected to the output of the second comparator, the second successive approximation register logic unit being configured to control the second digital-to-analog converter;

the input of the second digital-to-analog converter forming the input of the second SAR ADC module;

the output of the second comparator forming the output of the second SAR ADC module.

12. The converting device according to claim 1, wherein the multiplexing module comprises a digital cancellation logic unit adapted to apply a first transfer function to the first digital signal and a second transfer function to the second digital signal, so as to cancel the first residue signal.

13. An electronic sensor comprising an analog-to-digital converting device for converting an analog input signal into a digital output signal, wherein the converting device is according to claim 1.

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