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Auteurs: Authors: Brahim Aïssa, Mourad Nedil, A. H. Esam, N. Tabet, Daniel Therriault, & Federico Rosei

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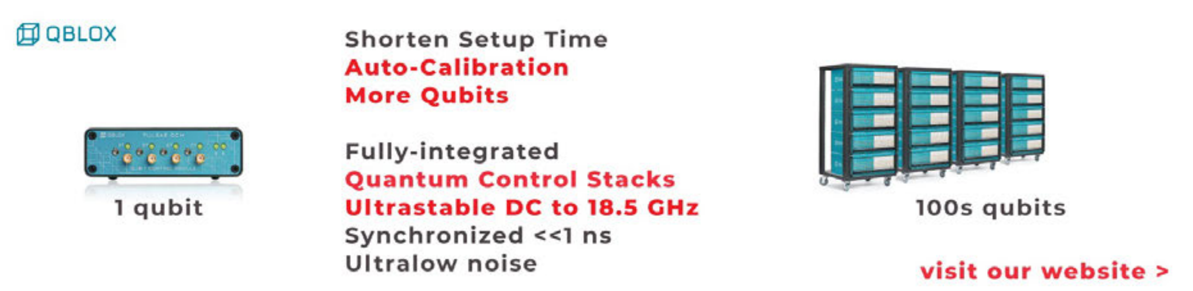

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Ambipolar operation of hybrid SiC-carbon nanotube based thin film transistors for logic circuits applications

B. Aïssa,[1,a)] M. Nedil,[2] A. H. Esam,[3] N. Tabet,[4] D. Therriault,[5] and F. Rosei[6,a)]
[1]Department of Smart Materials and Sensors for Space Missions, MPB Technologies Inc., 151 Hymus Boulevard, Montreal H9R 1E9, Canada
[2]Laboratoire de Recherche Télébec en Communications Souterraines, UQAT. 450, 3e Avenue, Val-d'Or J9P 1S2, Canada
[3]Department of High Energy Physics, Yanbu University College, P.O. Box 30031, Kingdom of Saudi Arabia
[4]Department of Physics, Center of Excellence in Nanotechnology (CENT), P.O. 477, KFUPM, Kingdom of Saudi Arabia
[5]Center for Applied Research on Polymers (CREPEC), Department of Mechanical Engineering, École Polytechnique de Montréal, P.O. Box 6079, Montreal H3C 3A7, Canada
[6]Centre Énergie, Matériaux et Télécommunications, INRS-EMT, 1650 Boulevard Lionel-Boulet, Varennes, Quebec J3X 1S2, Canada

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We report on the ambipolar operation of back-gated thin film field-effect transistors based on hybrid n-type-SiC/p-type-single-walled carbon nanotube networks made with a simple drop casting process. High-performances such an on/off ratio of 10^5, on-conductance of 20 μS, and a subthreshold swing of less than 165 mV/decades were obtained. The devices are air-stable and maintained their ambipolar operation characteristics in ambient atmosphere for more than two months. Finally, these hybrid transistors were utilized to demonstrate advanced logic NOR-gates. This could be a fundamental step toward realizing stable operating nanoelectronic devices. © 2012 American Institute of Physics. [http://dx.doi.org/10.1063/1.4739939]

In recent years, thin-film transistors (TFTs) technology has undergone significant developments for applications in logic systems, especially for advanced electronic applications such as radio frequency identification tags and flat panel displays.[1–5] Due to the excellent properties of silicon carbide (SiC), such as wide band-gap, high electron saturation drift velocity, and high thermal conductivity, transistor devices based on SiC have been studied extensively.[6] Moreover, SiC is a wide-band-gap semiconductor on which a high quality thermal oxide of SiO_2 can be grown. For example, 4H–SiC, with its high band gap of 3.2 eV, could function well in a wide band- gap heterostructure as logic circuit if combined with a suitable complementary material. Among the various molecular switching units suggested to date as TFT, single-walled carbon nanotubes (SWNT) are an exemplary case due to their known excellent electronic properties.[7,8] Several research groups have reported the fabrication of SWNT based logic gates.[9–12] Nevertheless, a key technological challenge remains the fabrication of air stable ambipolar n-type and p-type TFTs, which is necessary for complementary logic circuits. SWNTs, without special treatments, normally tend to exhibit p-type behavior, which is attributed to either Fermi-level alignment at the contact or hole doping in the channel by environmental oxygen species.[13,14] Therefore, the TFT channel doping or the Schottky metal-contact barrier engineering,[15,16] achieving long-term stability operation under ambient conditions, remains a great challenge because of the oxidation phenomenon under ambient air.[17] Meanwhile, to construct logic gates, the complementary metal-oxide-semiconductor (CMOS) architecture is preferred because it has lower power consumption compared with other logic families such as the resistor transistor logic.

[a)]Authors to whom correspondence should be addressed. Electronic addresses: brahim.aissa@mpbc.ca and rosei@emt.inrs.ca.

In this letter, we describe an air-stable hybrid n-type SiC/p-type-SWNT based TFT, protected with poly(methyl methacrylate) (PMMA) to keep the percolation level of the SWNT network spatially and temporally stable, while protecting it from atmosphere exchanges. In particular, we succeeded in constructing advanced NOR gates CMOS logic circuit. High-performances were obtained, such as an on/off ratio of 10^5, an on-conductance of 20 μS, and a subthreshold swing of less than 165 mV/decade. In addition, our devices maintained their ambipolar operation characteristics under ambient air for more than two months, which is a fundamental achievement towards realizing operating-stable nanoelectronic devices.

SWNTs have been synthesized by using the developed plasma torch technology (detailed process can be found in our Ref. 18). This process exclusively produces SWNTs, where their growth takes place in the gas-phase. The as-grown soot like SWNTs were subsequently purified by an acidic treatment through refluxing in a 3M-HNO_3 (Sigma Aldrich) solution.[19] The plasma-grown carbon nanotubes were characterized by the bright field transmission electron microscopy (TEM) using a Jeol JEM-2100 F FEG- TEM (200 kV) microscope. Figure 1(a) shows a representative TEM micrograph of the purified SWNT deposit, where bundles of a few SWNTs (the diameter of the individual tubes is about 1.2 nm) are clearly seen. These bundles have diameters in the 2–10 nm range and lengths of the order of few μm, leading thereby to aspect ratios over three orders of magnitudes. Figure 1(b) shows a typical Raman spectrum (Ar^+ laser radiation (2.41 eV). Renishaw Imaging Microscope

FIG. 1. (a) Representative TEM images of the purified SWNT. Inset is a close up view of a SWNTs bundle showing individual nanotube having a 1.2 nm-diam. (b) The corresponding microRaman spectrum. (c) Typical AFM image of the n-SiC surface, and (d) schematic of the hybrid n-SiC/p-SWNT back-gated TFT assembly.

Wire^{TM}) indicating a clear scattering radial breathing mode (RBM) peaks centered at 185 cm^{-1} and attributed to the strong presence of SWNTs having a mean diameter of 1.2 nm,[20] in total agreement with TEM observations. All the devices were fabricated on the epitaxial layer (p$^+$ ion implantation was used with concentrations of 5×10^{20} cm^{-3}) deposited on the (0001) Si-face of 4H-SiC wafers, purchased from Cree, Inc. Detailed processing steps can be found elsewhere.[21,22] To induce the electrical activation of the impurities and to crystallize the film, the implanted samples were annealed in a high vacuum furnace (10^{-6} mbar) at 1200 °C during 2 h. Samples were then oxidized for 13 h in dry O_2 at 1150 °C, yielding a gate dielectric oxide of about 110 nm. They were subsequently annealed in NO at 1175 °C for 4 h. Prior to SWNT deposition, the SiO_2 was first chemically etched from one side (hydrofluoric acid 13% with an etching rate of ∼4.43 nm/min). Figure 1(c) shows the contact-mode atomic force microscopy images (NanoScope III, Digital Instrument) of the SiC surface after SiO_2 removing. The purified SWNTs were first ultrasonicated in dimethylformamide (1 mg/ml) solution for 5 h to dissolve the SWNT bundles. The solution was then centrifuged at 12300 rpm for 15 min to select well-dispersed, narrow bundles of the SWNTs. The centrifuged solution was then drop (10 µl) casted on the top of n-4H-SiC surface (held at 60 °C for solvent evaporation). The density of deposited SWNTs was controlled through the number of drops cast on the substrate.[23] Ti/Au (20/180 nm) drain, source, and back-gated electrodes were then deposited by means of PLD (pulsed laser deposition, using ArF excimer laser, 193 nm) in a TFT scheme (Fig. 1(d)). Finally, a thin film of PMMA (Miller-Stephenson Chemical Co., Inc.) was directly deposited (by drop coating) onto the nanotubes network, to spatially maintain the SWNTs' percolation distribution and to protect the TFT active channel from long term oxidation.[24] Electrical transport properties of our hybrid TFTs were measured using a semiconductor parameter analyzer HP4155C, Agilent Technologies.

The channel length and width were initially designed to be 5 and 50 µm, respectively. To remove the metallic-SWNTs, we introduced an electrical breakdown (more details on the process are available in Ref. 25). Hereafter, we discuss the device characteristics achieved after the breakdown procedure. The on/off transistor switching ratios undergo significant improvement but are inevitably accompanied by a significant degradation of the on-current. Nevertheless, the electrical breakdown is time consuming, and thus one still needs to develop better ways to scale up the removal of metallic nanotubes.

We carried out systematic studies of the electrical performance of the devices. Figure 2(a) shows the TFT transfer

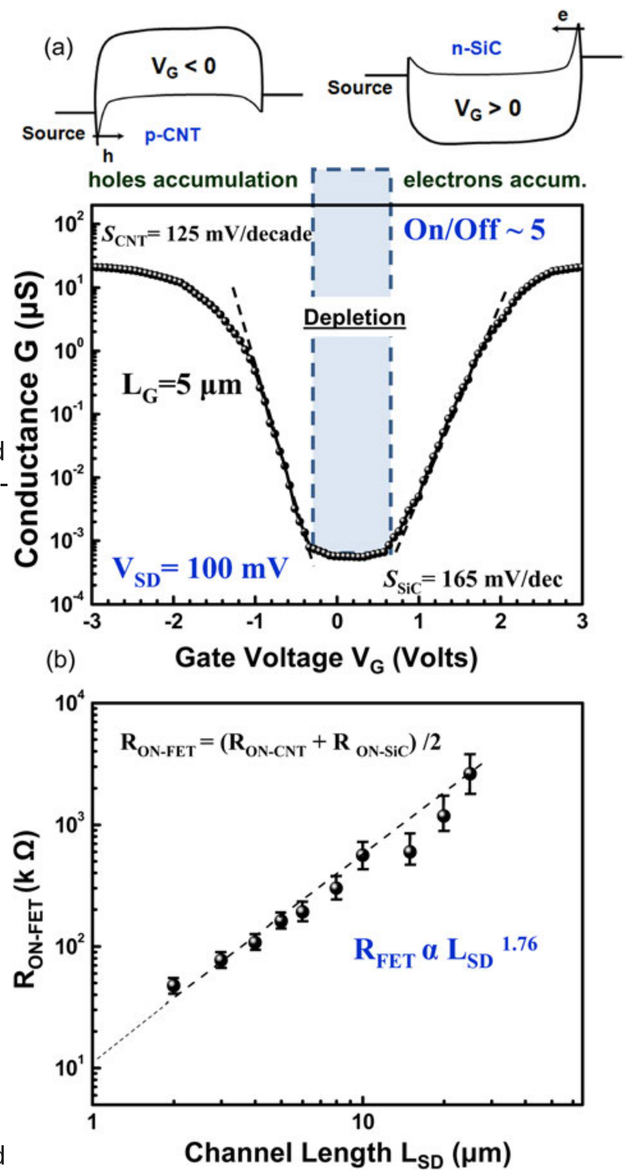

FIG. 2. (a) Electrical resistance measurements on devices with a channel width of 50 µm and channel lengths ranging from 2 to 30 µm. (b) Transfer characteristics (conductance G versus gate voltage V_G) of the hybrid TFT having a L_{SD} of 5 µm.

characteristics (conductance G as a function of gate voltage V_G) at 100 mV drain voltages (V_{DS}) measured in air (for a TFT channel length of 5 μm). All devices exhibit clear ambipolar characteristics, showing that one branch (p-type) of I_{DS} (or G) results from hole injection from the source, while the other branch (n-type) is due to electron injection from the drain. For the sake of discussion, we denote that the TFTs exhibit low off-conductance ($G_{OFF} < 1$ nS) measured at off-state and high on-conductance ($G_{ON} > 20$ μS) measured at the on-states for both the p- and n-regions. The corresponding on/off switching ratio was found to be as high as 10^5, with an excellent subthreshold swing S of 165 and 125 mV/dec, for the n and p TFT-regions, respectively. Our hybrid TFTs exhibit very promising characteristics rarely observed simultaneously.

At the On-states TFTs, we measured the average on-resistances of the devices (expressed as the average of the on-resistances of both the p- and n-regions, respectively) as a function of the transistor channel lengths. Such devices were made with channel widths W of 50 μm and channel lengths L_{SD} varying from 2 to 30 μm. The geometric scaling of the device resistance is shown in Fig. 2(b) which plots the log of the source to drain resistance versus log(L_{SD}) of the devices. The resistance data scale nonlinearly with channel length, and a least squares power law fit to the data yields $R \propto L^{1.76}$. This nonlinear scaling is most probably due to the nanotubes network and is an indication that the network approaches the percolation threshold where nonlinear effects are expected.[26] The extracted contact resistance of our devices was thereby found to be as low as 11.18 kΩ. Therefore, channel properties such as network density, which is crucial for long-channel devices, are not examined in the present work. It is worth noting at this level that all the measured transistor characteristics were found to achieve long-term stability operation under ambient conditions (i.e., within a maximum fluctuation of less than 4% after more than 2 months duration time). These performances are summarised in the Table I.

Finally, a sophisticated logic circuit based on the hybrid TFTs have also been demonstrated. An important outcome of this work is the addictiveness in integrating CMOS-like logic gates using ambipolar hybrid TFTs.

Figure 3 shows the output characteristics of the NOR gate. The logic block employs a 100 kΩ resistive load in the pull-down network, while four ambipolar hybrid TFTs were connected using external Au-wires to serve as the pull-up network. The value of the resistive load is chosen so that it is between the On-state resistance and the Off-state resistance of the transistors. The NOR circuit is operated with a V_{DD} of 3 V. 3 and −3 V applying on gates A and B are treated as logics "1" and "0," respectively. For the NOR gate, the output is "0" when either one of the two inputs is "1." These output characteristics confirm that our circuits realize the logic function correctly. Based on such hybrid TFT transistors, the construction of truly integrated circuits is currently in progress.

FIG. 3. Output characteristics of a NOR gate with resistive load using four hybrid ambipolar TFT. The supply voltage for the circuit $V_{SD} = 3$ V. Input voltages of 3 and −3 V are treated as logics "1" and "0," respectively.

In conclusion, we fabricated hybrid and air stable TFT ambipolar devices based on silicon carbide and carbon nanotubes materials, and we systematically studied their electronic properties. Combining the simultaneously p-type and n-type states into the hybrid devices, we demonstrated CMOS-NOR gates with appropriate resistive load. Although ambipolar behavior has been considered undesirable in next-generation devices, there is mounting evidence that the ability to control ambipolarity presents a design opportunities, and this work strongly argues for further investigation of its applicability.

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TABLE I. Data summarizing the main transistor performances measured under ambient conditions with respect to the time over 2 months-duration.

	Day 1	Day 17	Day 33	Day 49	Day 65	% Fluctuation
G_{on} (n-Sic) (μS)	19.6	19.8	20.2	20.1	20	3%
G_{on} (p-SWNT) (μS)	19.4	19.4	20	19.9	19.9	3%
On/off switching ratios	1.21×10^5	1.17×10^5	1.18×10^5	1.3×10^5	1.11×10^5	1%
S_{SWNT} (mV/decade)	121	126	122	123	125	4%
S_{SiC} (mV/decade)	163	164	166	167	165	3%
$R_{ON\text{-}FET}$ (kΩ)	11.18	11.63	11.19	11.16	11.37	4%

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